Programmable Logic Data Book 1994/1995

How To Use This Book

Overall Organization

This book has been organized by product type, beginning with Product Information. The products are next, starting with Small PLDs, then CPLDs, FPGAs, and Software. A section containing Quality and Reliability is next, followed by a Package Diagrams section. Within each section, data sheets are arranged in order of part number.

Recommended Search Paths

To search by:	Use:
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Size	The Product Selector Guide in section 1.
Numeric part number	Numeric Device Index. The book is also arranged in order of part number.
Other manufacturer's part number	The Cross Reference Guide in section 1.
Military part number	The Military Selector Guide in section 1.

Key to Waveform Diagrams

 = Rising edge of signal will occur during this time.

 = Falling edge of signal will occur during this time.

 = Signal may transition during this time (don't care condition).

 = Signal changes from high-impedance state to valid logic level during this time.

 = Signal changes from valid logic level to high-impedance state during this time.

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General Information 1

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General Product Information

Cypress Semiconductor Background

Cypress Semiconductor was founded in April 1983 with the stated goal of serving the high-performance semiconductor market. This market is served by producing the highest-performance integrated circuits using state-of-the-art processes and circuit design. Cypress is a complete semiconductor manufacturer, performing its own process development, circuit design, wafer fabrication, assembly, and test. The company went public in May 1986 and has been listed on the New York Stock Exchange since October 1988.

The initial semiconductor process, a CMOS process employing 1.2-micron geometries, was introduced in March 1984. This process is used in the manufacturing of Static RAMs and Logic circuits. In the third quarter of 1984, a 1.2-micron CMOS EPROM process was introduced for the production of programmable products. At the time of introduction, these processes were the most advanced production processes in the industry. Following the 1.2-micron processes, a 0.8-micron CMOS SRAM process was implemented in the first quarter of 1986, and a 0.8-micron EPROM process in the third quarter of 1987.

In keeping with the strategy of serving the high-performance markets with state-of-the-art integrated circuits, Cypress introduced two new processes in 1989. These were a bipolar submicron process, targeted for ECL circuits, and a BiCMOS process to be used for most types of TTL and ECL circuits.

The circuit design technology used by Cypress is also state of the art. This design technology, along with advanced process technology, allows Cypress to introduce the fastest, highest-performance circuits in the industry. Cypress's offers products in four divisions: the Static Memory Division, the Programmable Products Division, the Computation Products Division, and the Data Communications Division.

Static Memories Division

Cypress is a market-leading supplier of SRAMs, providing a wide range of SRAM memories for leading companies worldwide. SRAMs are used in high-performance personal computers, workstations, telecommunications systems, industrial systems, instrumentation devices, and networking products. Cypress's lower production cost structure allows the company to compete effectively in the high-volume personal computer and workstation market for SRAMs, including providing cache RAMs to support today's high-performance microprocessors, such as Pentium™, and PowerPC™. This business, combined with upcoming low-voltage products for the cellular communications, portable instrument, and laptop/notebook PC markets, positions Cypress for future success in this key product area.

Multichip modules is a fast-growing market segment that consists of multiple semiconductor chips mounted in packages that can be inserted in a computer circuit board. Cache modules for personal computers are the mainstay of this product line, and Cypress has announced major design wins for these products in IBM's PS/ValuePoint™ line of PCs, and in Apple Computer's highest performing Power Macintosh™ products.

Programmable Products Division

With increasing pressure on system designers to bring products to market more quickly, programmable logic devices (PLDs) are becoming extremely popular. PLDs are logic control devices that can be easily programmed by engineers in the field, and later erased and reprogrammed. This allows the designers to make key changes to their systems very late in the development cycle to ensure competitive advantage. Used extensively in an wide range of applications, PLDs constitute a large and growing market. Cypress's UltraLogic™ product line addresses the high-density programmable logic market. UltraLogic includes the pASIC380 family of field-programmable gate arrays (FPGAs), the industry's fastest. It also includes the highest performance complex PLDs, the FLASH370 family. Both of these product families are supported by Cypress's VHDL (Very high-speed integrated circuit Hardware Description Language) based *Warp3*™, the industry's most advanced software design tool. Cypress pioneered the use of VHDL for PLD programming, and *Warp* software is a key factor in the company's overall success in the PLD market.

Cypress is a leading provider of the industry-standard 22V10 PLD with a wide range of offerings including a BiCMOS 22V10 at 5 ns. Cypress is committed to competing in all ranges of the PLD market, with small devices, the MAX™ CY7C340 EPLD line, and the UltraLogic products. To support these products, Cypress offers one of the industry's broadest range of programming tools and software for the programming of its PLDs.

Cypress provides one of the industry's broadest ranges of CMOS EPROMs and PROMs. Cypress owns a large share of the high-speed CMOS PROM market, and with its new cost structure, is effectively penetrating the mainstream EPROM market with a popular 256 Kbit EPROM and the introduction of the world's fastest 1 Megabit EPROM at 25 ns.

FCT Logic products are used in bus interface and data buffering applications in almost all digital systems. With the addition of the FCT logic product line, Cypress now offers over 46 standard logic and bus interface functions. The products are offered in the second generation FCT-T format, which is pin-compatible with the older FCT devices, but adds TTL (transistor-to-transistor logic) outputs for significantly lower ground bounce and improved system noise immunity. Cypress also offers the most popular devices with on-chip 25-ohm termination resistors (FCT2-T) to further lower ground bounce with no speed loss. Included in the new product family is the CYBUS3384, a bus switch that enables bidirectional data transfer between multiple bus systems or between 5 volt and 3.3 volt devices. This broad product offering is produced on Cypress's high-volume, CMOS manufacturing lines.

Data Communications Division

This is an especially significant area for Cypress since it represents a more market-driven orientation for the company in a fast-growing market segment. As part of the new company strategy, Cypress has dedicated this product line to serve the high-speed data communications market with a range of products from the physical connection layer to system-level solutions. HOTLink™, high-speed, point-to-point serial communications chips have been well received. HOTLink, along with the recently announced SONET/SDS Serial Transceiver (SST™), address the fast-growing market segments of Asynchronous Transfer Mode (ATM) and Fibre Channel communications. The data communications division encompasses related products including RoboClock, a programmable skew clock buffer that adjusts complex timing control signals for a broad range of systems. The division also offers a broad range of First-In, First-Out (FIFO) memories, used to communicate data between systems operating at different frequencies, and Dual-Port Memories, used to distribute data to two different systems simultaneously.

Computation Products Division

This division focuses on the high-volume, high-growth market surrounding the desktop computer. It is the second of Cypress's market-oriented divisions. The division includes timing technology products offered through Cypress's IC Designs Subsidiary in Kirkland, Washington, and a new line of PC chipsets. IC Designs products are used widely in personal computers and disk drives, and the product line provides Cypress with major inroads into these growing markets. IC Designs clock oscillators control the intricate timing of all aspects of a computer system, including signals for the computer's central processing unit (CPU), keyboard, disk drives, system bus, serial port, and real-time clock. They replace all of the metal can oscillators used in the system. This product line includes QuiXTAL™ – – a programmable metal can oscillator that replaces individual oscillators used to control timing signals in virtually every type of electronics equipment. Cypress's chipset offerings include products for 486-based personal computers, as well as PCI local bus controllers for graphics and multimedia desktop applications. Cypress has announced plans to introduce a low-power, 3.3 volt chipset for the Pentium P54C, as well as P54C bus controller.

Cypress Facilities

Situated in California's Silicon Valley (San Jose), Round Rock (Austin), Texas, and Bloomington, Minnesota, Cypress houses R&D, design, wafer fabrication, and administration. There are additional Cypress Design Centers in Starkville, Mississippi, Colorado Springs, Colorado, and the United Kingdom, and a PLD software design group in Beaverton, Oregon. The facilities are designed to the most demanding technical and environmental specifications in the industry. At the Texas and Minnesota facilities, the entire wafer fabrication area is specified to be a Class 1 environment. This means that the ambient air has less than 1 particle of greater than 0.2 microns in diameter per cubic foot of air. Other environmental considerations are carefully insured: temperature is controlled to a ±0.1 degree Fahrenheit tolerance; filtered air is completely exchanged more than 10 times each minute throughout the fab; and critical equipment is situated on isolated slabs to minimize vibration.

Attention to assembly is equally critical. Cypress manufactures 100 percent of our wafers in the United States, at our front-end fabrication sites in California (San Jose), Minnesota (Bloomington), and Texas (Round Rock). Cypress Texas, our largest fab, and Cypress Minnesota, our newest fab, are both Class 1 facilities.

To improve our global competitiveness, we chose to move most of our back-end assembly, test, and mark operations to a facility in Thailand. Be assured that Cypress's total quality commitment extends to the new site—Cypress Bangkok.

The move to Bangkok consummated an intense search by Cypress for a world-class, environmentally sophisticated facility that we could bring on line quickly. The Cypress search team scrutinized fifteen manufacturing facilities in five countries and chose a site managed by Alphatec Electronics Co., Ltd., a privately owned, entrepreneurial company promoted by the Thailand Board of Investment. Cypress Bangkok occupies almost 25,000 square feet—a significant portion of the manufacturing floor space available within the facility. The full facility at Bangkok occupies more than 85,000 square feet on a site that encompasses 25 acres—sufficient room for expansion to a number of buildings in a campus-like setting.

Manufacturing at the site since 1990 with a charter to specialize in IC packaging, the Alphatec facility has almost a century of person-years experience working for U.S. semiconductor suppliers. Thoroughly modern, MIL 883-certified, and with fully developed administrative, logistic, and manufacturing systems in place, the facility has earned an exceptional reputation for hermetic assembly and out-going quality.

Cypress San Jose maintains complete management control of Cypress Bangkok's assembly, test, mark, and ship operations within the facility, thus assuring complete continuity of San Jose's back-end operations and quality.

Cypress has added Tape Automated Bonding (TAB) to its package offering. TAB, a surface-mount packaging technology, provides the densest lead and package footprint available for fully tested die.

From Cypress's facility in Minnesota, a VME Bus Interface Products group has been in operation since the acquisition of VTC's fab in 1990. Cypress manufactures VIC and VAC VME devices on the 0.8 micron CMOS process.

The Cypress motto has always been "only the best—the best facilities, the best equipment, the best employees . . . all striving to make the best CMOS, BiCMOS, and bipolar products."

Cypress Process Technology

In the last decade, there has been a tremendous need for high-performance semiconductor products manufactured with a balance of SPEED, RELIABILITY, and POWER. Cypress Semiconductor overcame the classically held perceptions that CMOS was a moderate-performance technology.

Cypress initially introduced a 1.2-micron "N" well technology with double-layer poly and a single-layer metal. The process employed lightly doped extensions of the heavily doped source and drain regions for both "N" and "P" channel transistors for significant improvement in gate delays. Further improvements in performance, through the use of substrate bias techniques, have added the benefit of eliminating the input and output latch-up characteristics associated with older CMOS technologies.

Cypress pushed process development to new limits in the areas of PROMs (Programmable Read Only Memory) and EPLDs (Erasable Programmable Logic Devices). Both PROMs and EPLDs have existed since the early 1970s in a bipolar process that employed various fuse technologies and was the only viable high-speed nonvolatile process available. Cypress PROMs and EPLDs use EPROM technology, which has been in use in MOS (Metal Oxide Silicon) since the early 1970s. EPROM technology has traditionally emphasized density while forsaking performance. Through improved technology, Cypress produced the first high-performance CMOS PROMs and EPLDs, replacing their bipolar counterparts.

To maintain our leadership position in CMOS technology, Cypress introduced a sub-micron technology in 1987. This 0.8 micron breakthrough made Cypress's CMOS one of the most advanced production processes in the world. The drive to maintain leadership in process technology has not stopped with the 0.8-micron devices. Cypress introduced a 0.65-micron process in 1991. A 0.5-micron process is currently in production.

Although not a requirement in the high-performance arena, CMOS technology substantially reduces the power consumption for any device. This improves reliability by allowing the device to operate at a lower die temperature. Now higher levels of integration are possible without trading performance for power. For in-

stance, devices may now be delivered in plastic packages without any impact on reliability.

While addressing the performance issues of CMOS technology, Cypress has not ignored the quality and reliability aspects of technology development. Rather, the traditional failure mechanisms of electrostatic discharge (ESD) and latch-up have been addressed and solved through process and design technology innovation.

ESD-induced failure has been a generic problem for many high-performance MOS and bipolar products. Although in its earliest years, MOS technology experienced oxide reliability failures, this problem has largely been eliminated through improved oxide growth techniques and a better understanding of the ESD problem. The effort to adequately protect against ESD failures is perturbed by circuit delays associated with ESD protection circuits. Focusing on these constraints, Cypress has developed ESD protection circuitry specific to 1.2-, 0.8-, 0.65-, and 0.5-micron CMOS process technology. Cypress products are designed to withstand voltage and energy levels in excess of 2001 volts and 0.4 milli-joules.

Latch-up, a traditional problem with CMOS technologies, has been eliminated through the use of substrate bias generation techniques, the elimination of the "P" MOS pull-ups in the output drivers, the use of guardring structures and care in the physical layout of the products.

Cypress has also developed additional process innovations and enhancements: multilayer metal interconnections, advanced metal deposition techniques, silicides, exclusive use of plasma for etching, and 100-percent stepper technology with the world's most advanced equipment.

Cypress has developed a BiCMOS technology to augment the capabilities of the Cypress CMOS processes. The new BiCMOS technology is based on the Cypress 0.8-micron CMOS process for enhanced manufacturability. Like CMOS, the process is scalable, to take advantage of finer line lithography. Where speed is critical, Cypress BiCMOS allows increased transistor performance. It also allows reduced power in the non-speed critical sections of the design to optimize the speed/power balance. The BiCMOS process makes memories and logic operating up to 400 MHz possible.

Cypress technologies have been carefully designed, creating products that are "only the best" in high-speed, excellent reliability, and low power.

Ordering Information

In general, the valid ordering codes for all products follow the format below; e.g., CY7C128–45DMB, PALC16R8L–35PC

PAL & PLD

PREFIX	DEVICE	SUFFIX	FAMILY
PAL C	16R8	–25 L M B	PAL 20
PAL C	16R8	L–35 P C	LOW POWER PAL 20
PAL C	22V10	–25 W C	PAL 24 VARIABLE PRODUCT TERMS
PAL CE	16V8	–25 P C	FLASH-ERASABLE PAL20
PLD C	20G10	–25 W C	GENERIC PLD 24
CY	7C330	–33 P C	PLD SYNCHRONOUS STATE MACHINE

PROCESSING

B = MIL-STD-883C FOR MILITARY PRODUCT
= LEVEL 2 PROCESSING FOR COMMERCIAL PRODUCT
T = SURFACE-MOUNTED DEVICES TO BE TAPE AND REELED
R = LEVEL 2 PROCESSING ON TAPE AND REELED DEVICES

TEMPERATURE RANGE

C = COMMERCIAL (0°C TO +70°C)
I = INDUSTRIAL (–40°C TO +85°C)
M = MILITARY (–55°C TO +125°C)

PACKAGE

B =PLASTIC PIN GRID ARRAY (PPGA)
D =CERAMIC DUAL IN-LINE PACKAGE (CERDIP)/BRAZED DIP
E =TAPE AUTOMATED BONDING (TAB)
F =FLATPACK (SOLDER-SEALED FLAT PACKAGE)
G =PIN GRID ARRAY (PGA)
H =WINDOWED LEADED CHIP CARRIER
J =PLASTIC LEADED CHIP CARRIER (PLCC)
K =CERPACK (GLASS-SEALED FLAT PACKAGE)
L =LEADLESS CHIP CARRIER (LCC)
N =PLASTIC QUAD FLATPACK (PQFP)
P =PLASTIC DUAL IN-LINE (PDIP)
Q =WINDOWED LEADLESS CHIP CARRIER (LCC)
R =WINDOWED PIN GRID ARRAY (PGA)
S =SOIC (GULL WING)
T =WINDOWED CERPACK
U =CERAMIC QUAD FLATPACK (CQFP)
V =SOJ
W =WINDOWED CERAMIC DUAL IN-LINE PACKAGE (CERDIP)
X =DICE (WAFFLE PACK)
Y =CERAMIC LEADED CHIP CARRIER
Z =TSOP
HD =HERMETIC DIP (MODULE)
HV =HERMETIC VERTICAL DIP
PF =PLASTIC FLAT SIP
PS =PLASTIC SIP
PZ =PLASTIC ZIP
BG =BALL GRID ARRAY

SPEED (ns or MHz)

L = LOW-POWER OPTION
A, B, C, D, G, CF = REVISION LEVEL

Cypress FSCM #65786

Cypress Semiconductor Bulletin Board System (BBS) Announcement

Cypress Semiconductor supports a 24-hour electronic Bulletin Board System (BBS) that allows Cypress Applications to better serve our customers by allowing them to transfer files to and from the BBS.

The BBS is set up to serve in multiple ways. One of its purposes is to allow customers to receive the most recent versions of programming software. Another is to allow the customers to send PLD programming files that they are having trouble with to the BBS. Cypress Applications can then find the errors in the files, correct them, and place them back on the BBS for the customer to download. The customer may also ask questions in our open forum message area. The sysop (system operator) will forward these questions to the appropriate applications engineer for an answer. The answers then get posted back into the forum. The BBS also allows the customer to communicate with their local FAE electronically, and to download both application notes and the latest versions of selected datasheets.

Communications Set-Up

The BBS uses a USRobotics HST Dual Standard modems capable of 14.4-Kbaud rates without compression and rates upwards of 19.2-Kbaud with compression. It is compatible with CCITT V.32 bis, V.32, V.22 (2400-baud), Bell 212A (1200-baud), CCITT V.42, and CCITT V.42 bis. It also handles MNP levels 2, 3, 4, and 5.

To call the BBS, set your communication package parameters as follows:

Baud Rate:	1200 baud to 19.2 Kbaud. Max. is determined by your modem.
	Data Bits: 8
	Parity: None (N)
	Stop Bits: 1

In the U.S. the phone number for the BBS is (408) 943−2954. In Japan the BBS number is 81−423−69−8220. In Europe the BBS number is 49−810−62−2675. These numbers are for transmitting data only.

If the line is busy, please retry at a later time. When you access the BBS, an initial screen with the following statement will appear:

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Rybbs Bulletin Board
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After you choose the graphics format you want to use, the system will ask for your first and last name. If you are a first-time user, you will be asked a few questions for the purposes of registration. Otherwise you will be asked for your password, and then you will be logged onto the BBS, which is completely menu driven.

Downloading Application Notes and Datasheets

A complete listing of files that may be downloaded is included on the BBS. Application notes and selected datasheets are available for downloading in two formats, PCL and Postscript. An "hp" in front of the file name indicates it is a PCL file and can be downloaded to Hewlett-Packard LaserJets and compatible printers. Files without the hp preceding them are in Postscript and can be downloaded to any Postscript printer.

If you have any problems or questions regarding the BBS, please contact Cypress Applications at (408) 943−2821 (voice).

Contact a Cypress representative or use the Cypress Bulletin Board System to get copies of the application notes listed here.

ABEL 4.0/4.1 and the CY7C330, CY7C331, and CY7C332
Bus-Oriented Maskable Interrupt Controller
CMOS PAL Basics
CY7C330 as a Multi-Channel Mbus Arbiter
CY7C331 Asynchronous Self-Timed VMEbus Requestor
CY7C344 as a Second-Level Cache Controller for the 80486
Design Tips for Advanced Max Users
Designing a Multiprocessor Interrupt Distribution Unit with MAX
DMA Control Using the CY7C342 MAX EPLD
FDDI Physical Connection Management Using the CY7C330
FIFO RAM Controller with Programmable Flags
Interfacing PROMs and RAMs to DSP Using Cypress MAX Products
Introduction to Programmable Logic
PAL Design Example: A GCR Encoder/Decoder
pASIC380 Power vs. Operating Frequency
PLD-Based Data Path For SCSI-2
State Machine Design Considerations and Methodologies
T2 Framing Circuitry
Understanding the CY7C330 Synchronous EPLD
Using ABEL to Program the Cypress 22V10
Using ABEL to Program the CY7C330
Using ABEL 3.2 to Program the CY7C331
Using CUPL with Cypress PLDs
Using Log/IC to Program the CY7C330
Using One-Hot-State Coding to Accelerate a MAX State Machine
Using the CY7C330 in Closed-Loop Servo Control
Using the CY7C331 as a Waveform Generator
Using the CY7C344 with the PLD ToolKit
Are Your PLDs Metastable?
State Machine Design Considerations and Methodologies
Designing with the CY7C335 and *Warp2* VHDL Compiler
The FLASH370 Family Of CPLDs and Designing with *Warp2*
Implementing a Reframe Controller for the CY7B933 HOTLink Receiver in a CY7C371 CPLD
Architectures and Technologies for FPGAs
Designing with FPGAs
An Introduction to Cypress's 380 Family of FPGAs and the *Warp3* Design Tool
CY7C380 Family Quick Power Calculator
Using Scan Mode on pASIC380 For In-Circuit Testing
Getting Started Converting .ABL Files to VHDL
Top-Down Design Methodology With VHDL (Designing an Interrupt Controller)
Abel–HDL vs. IEEE–1076 VHDL
VHDL Techniques for Optimal Design Fitting
Describing State Machines with *Warp2* VHDL
Using Hierarchical VHDL Design

Glossary '93
Glossary '94

PLDs

Size	Organization	Pins	Part Number	Speed (ns)	I_{CC}/I_{SB} (mA @ ns)	Packages	Availability
PAL20	16L8	20	PAL16L8	t_{PD} = 4.5/5/7	180	D, J, P	Now
PAL20	16R8	20	PAL16R8	$t_{S/CO}$ = 2.5/4.5, 2.5/5, 3.5/6	180	D, J, P	Now
PAL20	16R6	20	PAL16R6	$t_{PD/S/CO}$ = 4.5/2.5/4.5, 5/2.5/5, 7/3.5/6	180	D, J, P	Now
PAL20	16R4	20	PAL16R4	$t_{PD/S/CO}$ = 4.5/2.5/4.5, 5/2.5/5, 7/3.5/6	180	D, J, P	Now
PAL20	16L8	20	PALC16L8/L	t_{PD} = 20	70, 45	D, L, P, Q, V, W	Now
PAL20	16R8	20	PALC16R8/L	$t_{S/CO}$ = 15/12	70, 45	D, L, P, Q, V, W	Now
PAL20	16R6	20	PALC16R6/L	$t_{PD/S/CO}$ = 20/20/15	70, 45	D, L, P, Q, V, W	Now
PAL20	16R4	20	PALC16R4/L	$t_{PD/S/CO}$ = 20/20/15	70, 45	D, L, P, Q, V, W	Now
PALCE20	16V8—Macrocell	20S	PALCE16V8	$t_{PD/S/CO}$ = 7.5/5/5, 10/6/7, 15/10/8	115/90/55	D, J, L, P	Now
PALCE24	20V8—Macrocell	24	PALCE20V8	$t_{PD/S/CO}$ = 7.5/5/5, 10/6/7, 15/10/8	115/90/55	D, J, L, P	Q494
PAL24	22V10—Macrocell	24S	PALC22V10/L	$t_{PD/S/CO}$ = 25/15/15	90, 55	D, J, K, L, P, Q, W	Now
PAL24	22V10—Macrocell	24S	PALC22V10B	$t_{PD/S/CO}$ = 15/10/10	90	D, H, J, K, L, P, Q, W	Now
PAL24	22V10—Macrocell	24S	PAL22V10C	$t_{PD/S/CO}$ = 6/3/5.5, 7.5/3/6, 10/3.6/7.5	190	D, J, L, P	Now
PAL24	22VP10—Macrocell	24S	PAL22VP10C	$t_{PD/S/CO}$ = 6/3/5.5, 7.5/3/6, 10/3.6/7.5	190	D, J, L, P	Now
PALCE24	22V10—Macrocell	24	PALC22V10D	$t_{PD/S/CO}$ = 7.5/5/5, 10/6/7, 15/10/8	130/90/90	D, J, L, P	Now
PAL24	22V10—Macrocell	24	PAL22V10G	$t_{PD/S/CO}$ = 5/2.5/4, 6/3/5.5	190	D, J, L	Now
PAL24	22VP10—Macrocell	24	PAL22VP10G	$t_{PD/S/CO}$ = 5/2.5/4, 6/3/5.5	190	D, J, L	Now
PLD24	20G10—Generic	24S	PLDC20G10	$t_{PD/S/CO}$ = 25/15/15	55	D, J, L, P, Q, W	Now
PLD24	20G10—Generic	24S	PLDC20G10B	$t_{PD/S/CO}$ = 15/12/10	70	D, H, J, L, P, Q, W	Now
PLD24	20G10—Generic	24S	PLD20G10C	$t_{PD/S/CO}$ = 7.5/3/6.5, 10/3.6/7.5	190	D, J, L, P	Now
PLD24	20RA10—Asynchronous	24S	PLD20RA10	$t_{PD/S/CO}$ = 15/10/15	80	D, H, J, L, P, Q, W	Now
PLD28	7C330—State Machine	28S	CY7C330	f_{MAX}, t_{IS}, t_{CO} = 66 MHz/3ns/12ns	130 @ 50 MHz	D, H, J, L, P, Q, W	Now
PLD28	7C331—Asynchronous, Registered	28S	CY7C331	$t_{PD/S/CO}$ = 20/12/20	120@25 ns	D, H, J, L, P, Q, W	Now
PLD28	7C335—Universal Synchronous	28S	CY7C335	f_{MAX}/t_{IS} = 100 MHz/2ns, 83 MHz/2ns	140	D, H, J, L, P, Q, W	Now

CPLDs

Size	Organization	Pins	Part Number	Speed (ns)	I_{CC}/I_{SB} (mA)	Packages	Availability
MAX28	7C344—32 Macrocell	28S	CY7C344/B	$t_{PD/S/CO}$ = 15/9/10, 10/6/5	200/150	D, H, J, P, W	Now
MAX44	7C343—64 Macrocell	44	CY7C343/B	$t_{PD/S/CO}$ = 20/12/12, 12/8/6	135/125	H, J, R	Now
MAX68	7C342—128 Macrocell	68	CY7C342/B	$t_{PD/S/CO}$ = 25/15/14, 12/8/6	250/225	H, J, R	Now
MAX84	7C341—192 Macrocell	84	CY7C341/B	$t_{PD/S/CO}$ = 25/20/16, 15/10/7	380/360	H, J, R	Now
MAX100	7C346—128 Macrocell	84, 100	CY7C346/B	$t_{PD/S/CO}$ = 25/15/14, 15/10/7	250/225	H, J, N, R	Now
FLASH370-44	7C371—32-Macrocell Flash CPLD	44	CY7C371	$f_{MAX}/t_S/t_{CO}$ = 143MHz/6.5 ns/6.5 ns	150/TBD	J, Y	Now
FLASH370-44	7C372—64-Macrocell Flash CPLD	44	CY7C372	$f_{MAX}/t_S/t_{CO}$ = 100 MHz/6.5 ns/6.5 ns	180/TBD	J, Y	Q494
FLASH370-84	7C373—64-Macrocell Flash CPLD	84, 100	CY7C373	$f_{MAX}/t_S/t_{CO}$ = 100 MHz/6.5 ns/ 6.5 ns	180/TBD	A, J, G, Y	Q494
FLASH370-84	7C374—128-Macrocell Flash CPLD	84, 100	CY7C374	$f_{MAX}/t_S/t_{CO}$ = 100 MHz/6.5 ns/ 6.5 ns	300/TBD	A, J, G, Y	Now
FLASH370-160	7C375—128-Macrocell Flash CPLD	160	CY7C375	$f_{MAX}/t_S/t_{CO}$ = 100 MHz/6.5 ns/ 6.5 ns	300/TBD	A, G, U	Now
FLASH370-160	7C376—192-Macrocell Flash CPLD	160	CY7C376	$f_{MAX}/t_S/t_{CO}$ = 83 MHz/10 ns/10 ns	300/TBD	A, G	Q495
FLASH370-240	7C377—192-Macrocell Flash CPLD	240	CY7C377	$f_{MAX}/t_S/t_{CO}$ = 83 MHz/10 ns/10 ns	300/TBD	BGA, N, G	Q495
FLASH370-160	7C378—256-Macrocell Flash CPLD	160	CY7C378	$f_{MAX}/t_S/t_{CO}$ = 83 MHz/10 ns/10 ns	300/TBD	A, G	Q295
FLASH370-240	7C379—256-Macrocell Flash CPLD	240	CY7C379	$f_{MAX}/t_S/t_{CO}$ = 83 MHz/10 ns/10 ns	300/TBD	BGA, N, G	Q295

FPGAs

Size	Organization	Pins	Part Number	Speed Grade	I_{CC}/I_{SB} (mA)	Packages	Availability
pASIC380–1K	CMOS 8x12, 1K Gates FPGA	44	CY7C381A	–0, –1, –2	I_{SB} = 10	J	Now
pASIC380–1K	CMOS 8x12, 1K Gates FPGA	68, 100	CY7C382A	–0, –1, –2	I_{SB} = 10	A, G, J	Now
pASIC380–1K 3.3V	3.3V CMOS 8x12, 1K Gates FPGA	44	CY7C3381A	–0, –1, –2	I_{SB} = 2	J	Q394
pASIC380–1K 3.3V	3.3V CMOS 8x12, 1K Gates FPGA	68, 100	CY7C3382A	–0, –1, –2	I_{SB} = 2	A, G, J	Q394
pASIC380–2K	CMOS 12x16, 2K Gates FPGA	68	CY7C383A	–0, –1, –2	I_{SB} = 10	J	Now
pASIC380–2K	CMOS 12x16, 2K Gates FPGA	84, 100	CY7C384A	–0, –1, –2	I_{SB} = 10	A, G, J	Now
pASIC380–4K	CMOS 16x24, 4K Gates FPGA	84, 100	CY7C385A	–0, –1, –2	I_{SB} = 10	A, J	Now
pASIC380–4K	CMOS 16x24, 4K Gates FPGA	144 160	CY7C386A	–0, –1, –2	I_{SB} = 10	A, G, U	Now
pASIC380–8K	CMOS 24x32, 8K Gates FPGA	144	CY7C387A	–0, –1, –2	I_{SB} = 10	A, G	Q195
pASIC380–8K	CMOS 24x32, 8K Gates FPGA	208	CY7C388A	–0, –1, –2	I_{SB} = 10	N, G	Q195
pASIC380–12K	CMOS 32x36, 12K Gates FPGA	208	CY7C389A	–0, –1, –2	I_{SB} = 10	N	Q495

Design and Programming Tools

Part Name	Type	Part Number
Warp2 for PC	VHDL Design Tool	CY3120
Warp2 for Sun	VHDL Design Tool	CY3125
Warp3 for PC	VHDL/CAE Design Tool	CY3130
Warp3 for Sun	VHDL/CAE Design Tool	CY3135
Impulse3	Programmer	CY3500

Notes:

The above specifications are for the commercial temperature range of 0°C to 70°C. Military temperature range (–55°C to +125°C) product processed to MIL-STD-883 Revision C is also available for most products. Speed and power selections may vary from those above. Contact your local sales office for more information.

Commercial grade product is available in plastic, CERDIP, or LCC. Military grade product is available in CERDIP, LCC, or PGA. F, K, and T packages are special order only.

All power supplies are V_{CC} = 5V ± 10%.

22S, 24S, 28S stands for 300 mil. 22-pin, 24-pin, 28-pin, respectively. 28.4 stands for 28-pin 400 mil, 24.4 stands for 24-pin 400 mil.

PLCC, SOJ, and SOIC packages are available on some products.

F, K, and T packages are special order only.

Package Code:

B = PLASTIC PIN GRID ARRAY
D = CERDIP
E = TAPE AUTOMATED BOND (TAB)
F = FLATPACK
G = PIN GRID ARRAY (PGA)
H = WINDOWED HERMETIC LCC
J = PLCC
K = CERPACK
L = LEADLESS CHIP CARRIER (LCC)
N = PLASTIC QUAD FLATPACK
P = PLASTIC
Q = WINDOWED LCC
R = WINDOWED PGA
S = SOIC
T = WINDOWED CERPACK
U = CERAMIC QUAD FLATPACK
V = SOJ
W = WINDOWED CERDIP
X = DICE
Y = CERAMIC LCC
Z = TSOP
HD = HERMETIC DIP (Module)
HV = HERMETIC VERTICAL DIP
PF = PLASTIC FLAT SIP
PS = PLASTIC SIP
PZ = PLASTIC ZIP
BG = BALL GRID ARRAY

CYPRESS	CYPRESS
PALC16L8-25C	PALC16L8L-25C
PALC16L8-30M	PALC16L8-20M
PALC16L8-35C	PALC16L8-25C
PALC16L8-40M	PALC16L8-30M
PALC16L8L-35C	PALC16L8L-25C
PALC16R4-25C	PALC16R4L-25C
PALC16R4-30M	PALC16R4-20M
PALC16R4-35C	PALC16R4-25C
PALC16R4-40M	PALC16R4-30M
PALC16R4L-35C	PALC16R4L-25C
PALC16R6-25C	PALC16R6L-25C
PALC16R6-30M	PALC16R6-20M
PALC16R6-35C	PALC16R6-25C
PALC16R6-40M	PALC16R6-30M
PALC16R6L-35C	PALC16R6L-25C
PALC16R8-25C	PALC16R8L-25C
PALC16R8-30M	PALC16R8-20M
PALC16R8-35C	PALC16R8-25C
PALC16R8-40M	PALC16R8-30M
PALC16R8L-35C	PALC16R8L-25C
PALC22V10-35C	PALC22V10-25C
PALC22V10-40M	PALC22V10-30M
PALC22V10L-25C	PALC22V10-25C
PALC22V10L-35C	PALC22V10L-25C
PLDC20G10-35C	PLDC20G10-25C
PLDC20G10-40M	PLDC20G10-30M

ALTERA	CYPRESS
PREFIX:EPM	PREFIX:CY
5032DC	7C344-25WC
5032DC-2	7C344-20WC
5032DC-15	7C344-15WC
5032DC-17	Call Factory
5032DC-20	7C344-20WC
5032DC-25	7C344-25WC
5032DM	7C344-25WMB
5032DM-25	7C344-25WMB
5032JC	7C344-25HC
5032JC-2	7C344-20HC
5032JC-15	7C344-15HC
5032JC-17	Call Factory
5032JC-20	7C344-20HC
5032JC-25	7C344-25HC
5032JI-20	7C344-20HI
5032JM	7C344-25HMB
5032JM-25	7C344-25HMB
5032LC	7C344-25JC
5032LC-2	7C344-20JC
5032LC-15	7C344-15JC
5032LC-17	Call Factory
5032LC-20	7C344-20JC
5032LC-25	7C344-25JC
5032PC	7C344-25PC
5032PC-2	7C344-20PC
5032PC-15	7C344-15PC
5032PC-17	Call Factory
5032PC-20	7C344-20PC
5032PC-25	7C344-25PC
5064JC	7C343-35HC
5064JC-1	7C343-25HC
5064JC-2	7C343-30HC
5064JI	7C343-35HI

ALTERA	CYPRESS
5064JM	7C343-35HMB
5064LC	7C343-35JC
5064LC-1	7C343-25JC
5064LC-2	7C343-30JC
5128AGC-1	7C342B-12RC
5128AGC-2	7C342B-15RC
5128AGC-3	7C342B-20RC
5128AJC-1	7C342B-12HC
5128AJC-2	7C342B-15HC
5128AJC-3	7C342B-20HC
5128ALC-1	7C342B-12JC
5128ALC-2	7C342B-15JC
5128ALC-3	7C342B-20JC
5128GC	7C342-35RC
5128GC-1	7C342-25RC
5128GC-2	7C342-30RC
5128GM	7C342-35RMB
5128JC	7C342-35HC
5128JC-1	7C342-25HC
5128JC-2	7C342-30HC
5128JI	7C342-35HI
5128JI-2	7C342-30HI
5128JM	7C342-35HMB
5128LC	7C342-35JC
5128LC-1	7C342-25JC
5128LC-2	7C342-30JC
5128LI	7C342-35JI
5128LI-2	7C342-30HI
5130GC	7C346-35RC
5130GC-1	7C346-25RC
5130GC-2	7C346-30RC
5130GM	7C346-35RM
5130JC	7C346-35HC
5130JC-1	7C346-25HC
5130JC-2	7C346-30HC
5130JM	7C346-35HM
5130LC	7C346-35JC
5130LC-1	7C346-25JC
5130LC-2	7C346-30JC
5130LI	7C346-35JI
5130LI-2	7C346-30JI
5130QC	7C346-35NC
5130QC-1	7C346-25NC
5130QC-2	7C346-30NC
5130QI	7C346-35NI
5192AGC-1	7C341B-15RC
5192AGC-2	7C341B-20RC
5192AJC-1	7C341B-15HC
5192AJC-2	7C341B-20HC
5192ALC-1	7C341B-15JC
5192ALC-2	7C431B-20JC
5192GC	7C341-35RC
5192GC-1	7C341-25RC
5192GC-2	7C341-30RC
5192JC	7C341-35HC
5192JC-1	7C341-25HC
5192JC-2	7C341-30HC
5192JI	7C341-35HI
5192LC	7C341-35JC
5192LC-1	7C341-25JC
5192LC-2	7C341-30JC

AMD	CYPRESS
SMD PN	SMD PN
5962-85155 01RX	5962-88713 09RX
5962-85155 012X	5962-88713 09XX
5962-85155 02RX	5962-88713 10RX
5962-85155 022X	5962-88713 10XX
5962-85155 03RX	5962-88713 11RX
5962-85155 032X	5962-88713 11XX
5962-85155 04RX	5962-88713 12RX
5962-85155 042X	5962-88713 12XX
5962-85155 05RX	5962-88713 09RX
5962-85155 052X	5962-88713 09XX
5962-85155 06RX	5962-88713 10RX
5962-85155 062X	5962-88713 10XX
5962-85155 07RX	5962-88713 11RX
5962-85155 072X	5962-88713 11XX
5962-85155 08RX	5962-88713 12RX
5962-85155 082X	5962-88713 12XX
5962-85155 09RX	5962-92338 01MRX
5962-85155 092X	5962-92338 01MXX
5962-85155 10RX	5962-92338 01MRX
5962-85155 102X	5962-92338 02MXX
5962-85155 11RX	5962-92338 03MRX
5962-85155 112X	5962-92338 03MXX
5962-85155 12RX	5962-92338 04MRX
5962-85155 122X	5962-92338 04MXX
5962-85155 13RX	5962-92338 01MRX
5962-85155 14RX	5962-92338 02MRX
5962-85155 15RX	5962-92338 03MRX
5962-85155 16RX	5962-92338 04MRX
5962-85155 17RX	5962-92338 01MRX
5962-85155 18RX	5962-92338 02MRX
5962-85155 19RX	5962-92338 03MRX
5962-85155 20RX	5962-92338 04MRX
5962-86053 01LA	5962-89841 01LX
5962-86053 013A	5962-89841 013X
5962-86053 01KA	5962-89841 01KX
5962-86053 02LA	5962-89841 01LX
5962-86053 023A	5962-89841 013X
5962-86053 02KA	5962-89841 01KX
5962-86053 04LA	5962-89841 02LX
5962-86053 043A	5962-89841 023X
5962-86053 04KA	5962-89841 02KX
5962-86053 053A	5962-89841 063X
5962-86053 05KA	5962-89841 06KX
5962-86053 05LA	5962-89841 06LX
5962-88515 01RX	5962-88713 09RX
5962-88515 012X	5962-88713 09XX
5962-88515 02RX	5962-88713 10RX
5962-88515 022X	5962-88713 10XX
5962-88515 03RX	5962-88713 11RX
5962-88515 032X	5962-88713 11XX
5962-88515 04RX	5962-88713 12RX
5962-88515 042X	5962-88713 12XX
PREFIX:Am	PREFIX:CY
PREFIX:SN	PREFIX:CY
SUFFIX:B	SUFFIX:B
SUFFIX:D	SUFFIX:D OR W
SUFFIX:F	SUFFIX:F
SUFFIX:L	SUFFIX:L
SUFFIX:P	SUFFIX:P
MACH110-12JC	7C371-83JC
MACH110-15JC	7C371-66JC

Product Line Cross Reference

AMD	CYPRESS
MACH110-20JC	7C371-66JC
MACH110-20/BXA	7C371-66YMB
MACH130-15JC	7C373-83JC
MACH130-20JC	7C373-66JC
MACH130-20/BXA	7C373-66YMB
MACH210-12JC	7C372-100JC
MACH210-15JC	7C372-83JC
MACH210-20JC	7C372-66JC
MACH210-20/BXA	7C372-66YMB
MACH210A-10JC	7C372-125JC
MACH210A-12JC	7C372-100JC
MACH230-15JC	7C374-83JC
MACH230-20JC	7C374-66JC
MACH435-15JC	7C374-83JC
MACH435-20JC	7C374-66JC
PAL16L8-4C	PAL16L8-4C
PAL16L8-5C	PAL16L8-5C
PAL16L8-7C	PAL16L8-7C
PAL16L8-10/B	PAL16L8-10M
PAL16L8-12/B	PAL16L8-10M
PAL16L8-D/2	PAL16L8-7C
PAL16L8A-4C	PALC16L8L-35C
PAL16L8A-4M	PALC16L8-40M
PAL16L8AC	PALC16L8-25C
PAL16L8ALC	PALC16L8-25C
PAL16L8ALM	PALC16L8-30M
PAL16L8AM	PALC16L8-30M
PAL16L8BM	PALC16L8-20M
PAL16L8C	PALC16L8-35C
PAL16L8LC	PALC16L8-35C
PAL16L8LM	PALC16L8-40M
PAL16L8M	PALC16L8-40M
PAL16L8QC	PALC16L8L-35C
PAL16L8QM	PALC16L8-40M
PAL16R4-4C	PAL16R4-4C
PAL16R4-5C	PAL16R4-5C
PAL16R4-7C	PAL16R4-7C
PAL16R4-10/B	PAL16R4-10M
PAL16R4-12/B	PAL16R4-10M
PAL16R4-D/2	PAL16R4-7C
PAL16R4A-4C	PALC16R4L-35C
PAL16R4A-4M	PALC16R4-40M
PAL16R4ALC	PALC16R4-25C
PAL16R4ALM	PALC16R4-30M
PAL16R4AM	PALC16R4-30M
PAL16R4BM	PALC16R4-20M
PAL16R4C	PALC16R4-35C
PAL16R4LC	PALC16R4-35C
PAL16R4LM	PALC16R4-40M
PAL16R4M	PALC16R4-40M
PAL16R4QC	PALC16R4L-35C
PAL16R4QM	PALC16R4-40M
PAL16R6-4C	PAL16R6-4C
PAL16R6-5C	PAL16R6-5C
PAL16R6-7C	PAL16R6-7C
PAL16R6-10/B	PAL16R6-10M
PAL16R6-12/B	PAL16R6-10M
PAL16R6-D/2	PAL16R6-7C
PAL16R6A-4C	PALC16R6L-35C
PAL16R6A-4M	PALC16R6-40M
PAL16R6AC	PALC16R6-25C
PAL16R6ALC	PALC16R6-25C

AMD	CYPRESS
PAL16R6ALM	PALC16R6-30M
PAL16R6AM	PALC16R6-30M
PAL16R6BM	PALC16R6-20M
PAL16R6C	PALC16R6-35C
PAL16R6LC	PALC16R6-35C
PAL16R6LM	PALC16R6-40M
PAL16R6M	PALC16R6-40M
PAL16R6QC	PALC16R6L-35C
PAL16R6QM	PALC16R6-40M
PAL16R8-4C	PAL16R8-4C
PAL16R8-5C	PAL16R8-5C
PAL16R8-7C	PAL16R8-7C
PAL16R8-10/B	PAL16R8-10M
PAL16R8-12/B	PAL16R8-10M
PAL16R8-D/2	PAL16R8-7C
PAL16R8A-4C	PALC16R8L-35
PAL16R8A-4M	PALC16R8-40M
PAL16R8AC	PALC16R8-25C
PAL16R8ALC	PALC16R8-25C
PAL16R8ALM	PALC16R8-30M
PAL16R8AM	PALC16R8-30M
PAL16R8BM	PALC16R8-20M
PAL16R8C	PALC16R8-35C
PAL16R8LC	PALC16R8-35C
PAL16R8LM	PALC16R8-40M
PAL16R8M	PALC16R8-40M
PAL16R8QC	PALC16R8L-35
PAL16R8QM	PALC16R8-40M
PAL22V10-7JC	PALC22V10D-7JC
PAL22V10-7PC	PALC22V10D-7PC
PAL22V10-10DC	PALC22V10D-10DC
PAL22V10-10JC	PALC22V10D-10JC
PAL22V10-10PC	PALC22V10D-10PC
PAL22V10-12/B3A	PALC22V10B-10LMB
PAL22V10-12/BLA	PALC22V10B-10DMB
PAL22V10-15DC	PALC22V10B-15DC
PAL22V10-15JC	PALC22V10B-15JC
PAL22V10-15PC	PALC22V10B-15PC
PAL22V10-20/B3A	PALC22V10B-20LMB
PAL22V10-20/BLA	PALC22V10B-20DMB
PAL22V10/B3A	PALC22V10-35LMB
PAL22V10/BLA	PALC22V10-35DMB
PAL22V10A/B3A	PALC22V10-25LMB
PAL22V10A/BLA	PALC22V10-25DMB
PAL22V10ADC	PALC22V10-25DC
PAL22V10AJC	PALC22V10-25JC
PAL22V10APC	PALC22V10-25PC
PAL22V10DC	PALC22V10-35DC
PAL22V10JC	PALC22V10-35JC
PAL22V10PC	PALC22V10-35PC
PALCE16V8H-7JC/4	PALCE16V8-7JC
PALCE16V8H-7PC/4	PALCE16V8-7PC
PALCE16V8H-10JC/4	PALCE16V8-10JC
PALCE16V8H-10PC/4	PALCE16V8-10PC
PALCE16V8H-15JC/4	PALCE16V8-15JC
PALCE16V8H-15PC/4	PALCE16V8-15PC
PALCE16V8H-25JC/4	PALCE16V8-25JC
PALCE16V8H-25PC/4	PALCE16V8-25PC
PALCE16V8Q-15JC/4	PALCE16V8L-15JC
PALCE16V8Q-15PC/4	PALCE16V8L-15PC
PALCE16V8Q-25JC/4	PALCE16V8L-25JC
PALCE16V8Q-25PC/4	PALCE16V8L-25PC

AMD	CYPRESS
PALCE22V10H-7JC	PALC22V10D-10JC
PALCE22V10H-10PC	PALC22V10D-7PC
PALCE22V10H-10JC	PALC22V10D-10JC
PALCE22V10H-10PC	PALC22V10D-10PC
PALCE22V10H -15/B3A	PALC22V10D -15LMB
PALCE22V10H -15/BLA	PALC22V10D -15DMB
PALCE22V10H-15JC	PALC22V10D-15JC
PALCE22V10H-15PC	PALC22V10D-15PC
PALCE22V10H -20/B3A	PALC22V10D -20LMB
PALCE22V10H -20/BLA	PALC22V10D -20DMB
PALCE22V10H -25/B3A	PALC22V10D -25LMB
PALCE22V10H -25/BLA	PALC22V10D -25DMB
PALCE22V10H-25JC	PALC22V10D-25JC
PALCE22V10H-25PC	PALC22V10D-25PC
PALCE22V10H -30/B3A	PALC22V10D -25LMB
PALCE22V10H -30/BLA	PALC22V10D -25DMB

ATMEL	CYPRESS
PREFIX:AT	PREFIX:CY
22V10	PALC22V10
22V10-15	PALC22V10B

HARRIS	CYPRESS
PREFIX:HM	PREFIX:CY
PREFIX:HPL	PREFIX:CY
SUFFIX:8	SUFFIX:B
PREFIX:1	SUFFIX:D
PREFIX:9	SUFFIX:F
PREFIX:4	SUFFIX:L
PREFIX:3	SUFFIX:P
16LC8-5	PALC16L8L-35C
16LC8-8	PALC16L8-40M
16LC8-9	PALC16L8-40M
16RC4-5	PALC16R4L-35C
16RC4-8	PALC16R4-40M
16RC4-9	PALC16R4-40M
16RC6-5	PALC16R6L-35C
16RC6-8	PALC16R6-40M
16RC6-9	PALC16R6-40M
16RC8-5	PALC16R8L-35C
16RC8-8	PALC16R8-40M
16RC8-9	PALC16R8-40M

INTEL	CYPRESS
PREFIX:85C	PREFIX:CY
PREFIX:85C	PREFIX:PLD
PREFIX:D	SUFFIX:D
PREFIX:L	SUFFIX:L
PREFIX:P	SUFFIX:P
SUFFIX:/B	SUFFIX:B
22V10-10C	PALC22V10D-7C
22V10-10C	PALC22V10D-10C
22V10-10C	PAL22V10C-7C+
22V10-10C	PAL22V10C-10C+
22V10-15C	PALC22V10B-15C
22V10-15C	PALC22V10D-15C

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB}

+ = meets all performance specs but may not meet I_{CC} or I_{SB}

* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB}

− = functionally equivalent

† = SOIC only

Product Line Cross Reference

LATTICE	CYPRESS
PREFIX:EE	PREFIX:CY
PREFIX:GAL	PREFIX:PALCE
PREFIX:ST	PREFIX:CY
SUFFIX:B	SUFFIX:B
SUFFIX:D	SUFFIX:D
SUFFIX:L	SUFFIX:L
SUFFIX:P	SUFFIX:P
GAL16V8A-10LJ	PALCE16V8-10JC
GAL16V8A-10LP	PALCE16V8-10PC
GAL16V8A-15LJ	PALCE16V8-15JC
GAL16V8A-15LP	PALCE16V8-15PC
GAL16V8A-15QJ	PALCE16V8L-15JC
GAL16V8A-15QP	PALCE16V8L-15PC
GAL16V8A-L5LJ	PALCE16V8-25JC
GAL16V8A-25LP	PALCE16V8-25PC
GAL16V8A-25QJ	PALCE16V8L-25JC
GAL16V8A-25QP	PALCE16V8L-25PC
GAL16V8B-7LJ	PALCE16V8-7JC
GAL16V8B-7LP	PALCE16V8-7PC
GAL16V8B-10LJ	PALCE16V8-10JC
GAL16V8B-10LJI	PALCE16V8-10JI
GAL16V8B-10LP	PALCE16V8-10PC
GAL16V8B-10LPI	PALCE16V8-10PI
GAL16V8B-15LJI	PALCE16V8-15JI
GAL16V8B-15LPI	PALCE16V8-15PI
GAL16V8B-25LJI	PALCE16V8-25JI
GAL16V8B-25LPI	PALCE16V8-25PI
GAL20V8A	PALCE20V8
GAL20V8B	PALCE20V8
GAL22V10B-7LJ	PALC22V10D-7JC
GAL22V10B-7LP	PALC22V10D-7PC
GAL22V10B-10LJ	PALC22V10D-10JC
GAL22V10B-10LP	PALC22V10D-10PC
GAL22V10B-15LD /883	PALC22V10D-15DMB
GAL22V10B-15LJ	PALC22V10D-15JC
GAL22V10B-15LJI	PALC22V10D-15JI
GAL22V10B-15LP	PALC22V10D-15PC
GAL22V10B-15LPI	PALC22V10D-15PI
GAL22V10B-15LR /883	PALC22V10D-15LMB
GAL22V10B-20LJI	PALC22V10D-15JI
GAL22V10B-20LD /883	PALC22V10D-15DMB
GAL22V10B-20LPI	PALC22V10D-15PI
GAL22V10B-20LR /883	PALC22V10D-15LMB
GAL22V10B-25LD /883	PALC22V10D-25DMB
GAL22V10B-25LJ	PALC22V10D-25JC
GAL22V10B-25LJI	PALC22V10D-25JI
GAL22V10B-25LP	PALC22V10D-25PC
GAL22V10B-25LPI	PALC22V10D-25PI
GAL22V10B-25LR /883	PALC22V10D-25LMB
GAL22V10B-30LD /883	PALC22V10D-25DMB
GAL22V10B-30LR /883	PALC22V10D-25LMB
GAL22V10C-5LJ	PAL22V10G-5JC
GAL22V10C-7LJ	PAL22V10D-7JC
GAL22V10C-7PC	PAL22V10D-7PC

MMI/AMD	CYPRESS
SUFFIX:883B	SUFFIX:B
SUFFIX:F	SUFFIX:F
SUFFIX:J	SUFFIX:D
SUFFIX:L	SUFFIX:L
SUFFIX:N	SUFFIX:P
SUFFIX:SHRP	SUFFIX:B
PAL12L10C	PLDC20G10-35C
PAL12L10M	PLDC20G10-40M
PAL14L8C	PLDC20G10-35C
PAL14L8M	PLD20G10-40M
PAL16L6C	PLD20G10-35C
PAL16L6M	PLDC20G10-40M
PAL16L8A-2C	PALC16L8-35C
PAL16L8A-2M	PALC16L8-40M
PAL16L8A-4C	PALC16L8L-35C
PAL16L8A-4M	PALC16L8-40M
PAL16L8AC	PALC16L8-25C
PAL16L8AM	PALC16L8-30M
PAL16L8B-2C	PALC16L8-35C
PAL16L8B-2M	PALC16L8-30M
PAL16L8B-4C	PALC16L8L-35C
PAL16L8B-4M	PALC16L8-40M
PAL16L8BM	PALC16L8-20M
PAL16L8C	PALC16L8-35C
PAL16L8D-4C	PALC16L8L-25C
PAL16L8D-4M	PALC16L8-30M
PAL16L8M	PALC16L8-40M
PAL16R4A-2C	PALC16R4-35C
PAL16R4A-2M	PALC16R4-40M
PAL16R4A-4C	PALC16R4L-35C
PAL16R4A-4M	PALC16R4-40M
PAL16R4AC	PALC16R4-25C
PAL16R4AM	PALC16R4-30M
PAL16R4B-2C	PALC16R4-25C
PAL16R4B-2M	PALC16R4-30M
PAL16R4B-4C	PALC16R4L-35C
PAL16R4B-4M	PALC16R4-40M
PAL16R4BM	PALC16R4-20M
PAL16R4C	PALC16R4-35C
PAL16R4D-4C	PALC16R4L-25C
PAL16R4M	PALC16R4-40M
PAL16R6A-2C	PALC16R6-35C
PAL16R6A-2M	PALC16R6-40M
PAL16R6A-4C	PALC16R6L-35C
PAL16R6A-4M	PALC16R6-40M
PAL16R6AC	PALC16R6-25C
PAL16R6AM	PALC16R6-30M
PAL16R6B-2C	PALC16R6-25C
PAL16R6B-2M	PALC16R6-30M
PAL16R6B-4C	PALC16R6L-35C
PAL16R6B-4M	PALC16R6-40M
PAL16R6BM	PALC16R6-20M
PAL16R6C	PALC16R6-35C
PAL16R6D-4C	PALC16R6L-25C
PAL16R6M	PALC16R6-40M
PAL16R8A-2C	PALC16R8-35C
PAL16R8A-2M	PALC16R8-40M
PAL16R8A-4C	PALC16R8L-35C
PAL16R8A-4M	PALC16R8-40M
PAL16R8AC	PALC16R8-25C
PAL16R8AM	PALC16R8-30M
PAL16R8B-2C	PALC16R8-25C

MMI/AMD	CYPRESS
PAL16R8B-2M	PALC16R8-30M
PAL16R8B-4C	PALC16R8L-35C
PAL16R8B-4M	PALC16R8-40M
PAL16R8BM	PALC16R8-20M
PAL16R8C	PALC16R8-35C
PAL16R8D-4C	PALC1648L-25C
PAL16R8M	PALC16R8-40M
PAL18L4C	PLDC20G10-35C
PAL18L4M	PLDC20G10-40M
PAL20L10AC	PLDC20G10-35C
PAL20L10AM	PLDC20G10-30M
PAL20L10C	PLDC20G10-35C
PAL20L10M	PLDC20G10-40M
PAL20L2C	PLDC20G10-35C
PAL20L2M	PLDC20G10-40M
PAL20L8A-2C	PLDC20G10-35C
PAL20L8A-2M	PLDC20G10-40M
PAL20L8AC	PLDC20G10-25C
PAL20L8AM	PLDC20G10-30M
PAL20L8C	PLDC20G10-35C
PAL20L8M	PLDC20G10-40M
PAL20R4A-2C	PLDC20G10-35C
PAL20R4A-2M	PLDC20G10-40M
PAL20R4AC	PLDC20G10-25C
PAL20R4AM	PLDC20G10-30M
PAL20R4C	PLDC20G10-35C
PAL20R4M	PLDC20G10-40M
PAL20R6A-2C	PLDC20G10-35C
PAL20R6A-2M	PLDC20G10-40M
PAL20R6AC	PLDC20G10-25C
PAL20R6AM	PLDC20G10-30M
PAL20R6C	PLDC20G10-35C
PAL20R6M	PLDC20G10-40M
PAL20R8A-2C	PLDC20G10-35C
PAL20R8A-2M	PLDC20G10-40M
PAL20R8AC	PLDC20G10-25C
PAL20R8AM	PLDC20G10-30M
PAL20R8C	PLDC20G10-35C
PAL20R8M	PLDC20G10-40M
PALC22V10/A	PALC22V10-35C

NATIONAL	CYPRESS
PREFIX:DM	PREFIX:CY
PREFIX:GAL	PREFIX:None
PREIFX:IDM	PREFIX:CY
PREFIX:NM	PREFIX:CY
PREFIX:NMC	PREFIX:CY
SUFFIX:J	SUFFIX:D
SUFFIX:N	SUFFIX:P
18L4C	PLDC20G10-35C
18L4M	PLDC20G10-40M
20L2M	PLDC20G10-40M
GAL22V10-15C	PALC22V10D-15C
GAL22V10-20I	PALC22V10D-15I
GAL22V10-20M	PALC22V10D-15M
GAL22V10-25C	PALC22V10D-25C
GAL22V10-30I	PALC22V10D-25I
GAL22V10-30M	PALC22V10D-25M
PAL164A2M	PALC16R4-40M
PAL16L8A2C	PALC16L8-35C
PAL16L8A2M	PALC16L8-40M
PAL16L8AC	PALC16L8-25C

Product Line Cross Reference

NATIONAL	CYPRESS
PAL16L8AM	PALC16L8-30M
PAL16L8B2C	PALC16L8-25C
PAL16L8B2M	PALC16L8-30M
PAL16L8B4C	PALC16L8L-35C
PAL16L8B4M	PALC16L8-40M
PAL16L8BM	PALC16L8-20M
PAL16L8C	PALC16L8-35C
PAL16L8M	PALC16L8-40M
PAL16R4A2C	PALC16R4-35C
PAL16R4AC	PALC16R4-25C
PAL16R4AM	PALC16R4-30M
PAL16R4B2C	PALC16R4-25C
PAL16R4B2M	PALC16R4-30M
PAL16R4B4C	PALC16R4L-35C
PAL16R4B4M	PALC16R4-40M
PAL16R4BM	PALC16R4-20M
PAL16R4C	PALC16R4-35C
PAL16R4M	PALC16R4-40M
PAL16R6A2C	PALC16R6-35C
PAL16R6A2M	PALC16R6-40M
PAL16R6AC	PALC16R6-25C
PAL16R6AM	PALC16R6-30M
PAL16R6B2C	PALC16R6-25C
PAL16R6B2M	PALC16R6-30M
PAL16R6B4C	PALC16R6L-35C
PAL16R6B4M	PALC16R6-40M
PAL16R6BM	PALC16R6-20M
PAL16R6C	PALC16R6-35C
PAL16R6M	PALC16R6-40M
PAL16R8A2C	PALC16R8-35C
PAL16R8A2M	PALC16R8-40M
PAL16R8AC	PALC16R8-25C
PAL16R8AM	PALC16R8-30M
PAL16R8B2C	PALC16R8-25C
PAL16R8B2M	PALC16R8-30M
PAL16R8B4C	PALC16R8L-35C
PAL16R8B4M	PALC16R8-40M
PAL16R8BM	PALC16R8-20M
PAL16R8C	PALC16R8-35C
PAL16R8M	PALC16R8-40M
PAL20L2C	PLDC20G10-35C
PAL20L8AC	PLDC20G10-25C
PAL20L8AM	PLDC20G10-30M
PAL20L8BC	PLDC20G10-25C
PAL20L8BM	PLDC20G10-30M
PAL20L8C	PLDC20G10-35C
PAL20L8M	PLDC20G10-40M
PAL20L10B2C	PLDC20G10-25C
PAL20L10B2M	PLDC20G10-30M
PAL20L10C	PLDC20G10-35C
PAL20L10M	PLDC20G10-40M
PAL20R4AC	PLDC20G10-25C
PAL20R4AM	PLDC20G10-30M
PAL20R4BC	PLDC20G10-25C
PAL20R4BM	PLDC20G10-30M
PAL20R4C	PLDC20G10-35C
PAL20R4M	PLDC20G10-40M
PAL20R6AC	PLDC20G10-25C
PAL20R6AM	PLDC20G10-30M
PAL20R6BC	PLDC20G10-25C
PAL20R6BM	PLDC20G10-30M
PAL20R6C	PLDC20G10-35C

NATIONAL	CYPRESS
PAL20R6M	PLDC20G10-40M
PAL20R8AC	PLDC20G10-25C
PAL20R8AM	PLDC20G10-30M
PAL20R8BC	PLDC20G10-25C
PAL20R8BM	PLDC20G10-30M
PAL20R8C	PLDC20G10-35C
PAL20R8M	PLDC20G10-40M

QUICKLOGIC	CYPRESS
PREFIX:QL	PREFIX:CY
8X12B-*CG68C	7C382A-*GC
8X12B-*CG68I	7C382A-*GI
8X12B-*CG68M	7C382A-*GMB
8X12B-*PF100C	7C382A-*AC
8X12B-*PF100I	7C382A-*AI
8X12B-*PL44C	7C381A-*JC
8X12B-*PL44I	7C381A-*JI
8X12B-*PL68C	7C382A-*JC
8X12B-*PL68I	7C382A-*JI
12X16B-*CG84C	7C384A-*GC
12X16B-*CG84I	7C384A-*GI
12X16B-*CG84M	7C384A-*GMB
12X16B-*PF100C	7C384A-*AC
12X16B-*PF100I	7C384A-*AI
12X16B-*PL68C	7C383A-*JC
12X16B-*PL68I	7C383A-*JI
12X16B-*PL84C	7C384A-*JC
12X16B-*PL84I	7C384A-*JI
16X24B-*GC144C	7C386A-*GC
16X24B-*GC144I	7C386A-*GI
16X24B-*GC144M	7C386A-*GMB
16X24B-*PF100C	7C385A-*AC
16X24B-*PF100I	7C385A-*AI
16X24B-*PF144C	7C386A-*AC
16X24B-*PF144I	7C386A-*AI
16X24B-*PL84C	7C385A-*JC
16X24B-*PL84I	7C385A-*JI
24X32B-*GC44C	7C387A-*GC
24X32B-*GC144I	7C387A-*GI
24X32B-*GC144MB	7C387A-*GMB
24X32B-*GC208C	7C388A-*GC
24X32B-*GC208I	7C388A-*GI
24X32B-*GC208M	7C388A-*GMB
24X32B-*PF144C	7C387A-*AC
24X32B-*PF144I	7C387A-*AI
24X32B-*PF208C	7C388A-*AC
24X32B-*PF208I	7C388A-*AI

TI	CYPRESS
PREFIX:JBP	PREFIX:CY
PREFIX:PAL	SUFFIX:P
PREFIX:SM	PREFIX:CY
PREFIX:SMJ	PREFIX:CY
PREFIX:SN	PREFIX:CY
PREFIX:TBP	PREFIX:CY
PREFIX:TIB	PREFIX:CY
PREFIX:TMS	PREFIX:CY
SUFFIX:F	SUFFIX:F
SUFFIX:J	SUFFIX:L
SUFFIX:N	SUFFIX:D
22V10AC	PALC22V10-25C
22V10AM	PALC22V10-30M
PAL16L8-5C	PAL16L8-5C

TI	CYPRESS
PAL16L8-7C	PAL16L8-7C
PAL16L8-7M	PAL16L8-7M
PAL16L8-10C	PAL16L8-7C
PAL16L8-10M	PAL16L8-10M
PAL16L8-12M	PAL16L8-10M
PAL16L8-15C	PAL16L8-7C
PAL16L8-15M	PAL16L8-10M
PAL16L8-20M	PALC16L8-20M
PAL16L8-25C	PALC16L8-25C
PAL16L8-30M	PALC16L8-30M
PAL16L8A-2C	PALC16L8-35C
PAL16L8A-2M	PALC16L8-40M
PAL16L8AC	PALC16L8-25C
PAL16L8AM	PALC16L8-30M
PAL16R4-5C	PAL16R4-5C
PAL16R4-7C	PAL16R4-7C
PAL16R4-7M	PAL16R4-7M
PAL16R4-10C	PAL16R4-7C
PAL16R4-10M	PAL16R4-10M
PAL16R4-12M	PAL16R4-10M
PAL16R4-15C	PAL16R4-7C
PAL16R4-15M	PAL16R4-10M
PAL16R4-20M	PALC16R4-20M
PAL16R4-25C	PALC16R4-25C
PAL16R4-30M	PALC16R4-30M
PAL16R4A-2C	PALC16R4-25C
PAL16R4A-2M	PALC16R4-40M
PAL16R4AC	PALC16R4-25C
PAL16R4AM	PALC16R4-30M
PAL16R6-5C	PAL16R6-5C
PAL16R6-7C	PAL16R6-7C
PAL16R6-7M	PAL16R6-7M
PAL16R6-10C	PAL16R6-7C
PAL16R6-10M	PAL16R6-10M
PAL16R6-12M	PAL16R6-10M
PAL16R6-15C	PAL16R6-7C
PAL16R6-15M	PAL16R6-10M
PAL16R6-20M	PALC16R6-20M
PAL16R6-25C	PALC16R6-25C
PAL16R6-30M	PALC16R6-30M
PAL16R6A-2C	PALC16R6-25C
PAL16R6A-2M	PALC16R6-40M
PAL16R6AC	PALC16R6-25C
PAL16R6AM	PALC16R6-30M
PAL16R8-5C	PAL16R8-5C
PAL16R8-7C	PAL16R8-7C
PAL16R8-7M	PAL16R8-7M
PAL16R8-10C	PAL16R8-7C
PAL16R8-10M	PAL16R8-10M
PAL16R8-12M	PAL16R8-10M
PAL16R8-15C	PAL16R8-7C
PAL16R8-15M	PAL16R8-10M
PAL16R8-20M	PALC16R8-20M
PAL16R8-25C	PALC16R8-25C
PAL16R8-30M	PALC16R8-30M
PAL16R8A-2C	PALC16R8-25C
PAL16R8A-2M	PALC16R8-40M
PAL16R8AC	PALC16R8-25C
PAL16R8AM	PALC16R8-30M
PAL20L8A-2C	PLDC20G10-25C
PAL20L8A-2M	PLDC20G10-30M
PAL20L8AC	PLDC20G10-25C

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB}

+ = meets all performance specs but may not meet I_{CC} or I_{SB}

* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB}

– = functionally equivalent

† = SOIC only

TI	CYPRESS
PAL20L8AM	PLDC20G10–30M
PAL20L10A–2C	PLDC20G10–25C
PAL20L10A–2M	PLDC20G10–30M
PAL20L10AC	PLDC20G10–35C
PAL20L10AM	PLDC20G10–30M
PAL20R4A–2C	PLDC20G10–25C
PAL20R4A–2M	PLDC20G10–30M
PAL20R4AC	PLDC20G10–25C
PAL20R4AM	PLDC20G10–30M
PAL20R6A–2C	PLDC20G10–25C
PAL20R6A–2M	PLDC20G10–30M
PAL20R6AC	PLDC20G10–25C
PAL20R6AM	PLDC20G10–30M
PAL20R8A–2C	PLDC20G10–25C
PAL20R8A–2M	PLDC20G10–30M
PAL20R8AC	PLDC20G10–25C
PAL20R8AM	PLDC20G10–30M
PAL22V10–7C	PALC22V10D–7C
PAL22V10–7C	PAL22V10C–7C
PAL22V10–15C	PALC22V10B–15C
PAL22V10–20M	PALC22V10B–20M
PAL22V10AC	PALC22V10–25C
PAL22V10AC	PALC22V10L–25C
PAL22V10AM	PALC22V10–25MB
PAL22V10AM	PALC22V10–30MB
PAL22V10C	PALC22V10–35C
PAL22V10C	PALC22V10L–35C

Military Overview

Features

Cypress products are designed using our state-of-the-art CMOS and BiCMOS processes, and they must meet the full – 55 to +125 degrees Celsius operational criteria for military use. The commitment continues with the 1986 DESC certification of our automated U.S. facility in San Jose, California. Cypress meets the stringent quality and reliability requirements of MIL-STD-883D and MIL-I-38535B and participates in each of the military processing programs: MIL-STD-883D compliant, SMD (Standardized Military Drawing), and QML.

Product Design

Every Cypress product is designed to meet or exceed the full temperature and functional requirements of military product. This means that Cypress builds military product as a matter of course, rather than as an accidental benefit of favorable test yield. Designs are being carried out in our industry-leading 0.65-micron CMOS and BiCMOS processes. Cypress is able to offer a family of products that are industry leaders in density, low operating and standby current, and high speed. In addition, our technology results in products with very small manufacturable die sizes that will fit into the LCCs and flatpacks so often used in military programs.

DESC-Certified Facility

On May 8, 1986, the Cypress facility at 3901 North First Street in San Jose, California was certified by DESC for the production of JAN Class B CMOS Microcircuits. And, most recently, on February 16, 1994, Cypress received QML (Qualified Manufacturers List) transitional certification from DESC to the requirements of MIL-I-38535B. This certification allows Cypress to continue to produce JAN products as well as manufacture devices listed on the QML. QML certification attests to Cypress' commitment to quality and reliability through the use of statistical process control and total quality management. Our wafer fabrication facilities are Class 10 (San Jose) and Class 1 (Round Rock, TX and Bloomington, MN) manufacturing environments and our assembly facility is also a clean room.

Datasheet Documentation

Every Cypress final data sheet is a corporate document with a revision history. The document number and revision appears on each final data sheet. Cypress maintains a listing of all data sheet documentation and a copy is available to customers upon request. This gives a customer the ability to verify the current status of any data sheet and it also gives that customer the ability to obtain updated specifications as required.

Every final data sheet also contains detailed Group A subgroup testing information. All of the specified parameters that are tested at Group A are listed in a table at the end of each final data sheet, with a notation as to which specific Group A test subgroups apply.

Assembly Traceability Code™

Cypress Semiconductor places an assembly traceability code on every military package that is large enough to contain the code. The ATC automatically provides traceability for that product to the individual wafer lot. This unique code provides Cypress with the ability to determine which operators and equipment were used in the manufacture of that product from start to finish.

Quality and Reliability

MIL-STD-883D and MIL-I-38535B spell out the toughest of quality and reliability standards for military products. Cypress products meet all of these requirements and more. Our in-house quality and reliability programs are being updated regularly with tighter and tighter objectives. Please refer to the chapter on Quality, Reliability, and Process Flows for further details.

Military Product Offerings

Cypress offers three levels of processing for military product.

First, all Cypress products are available with processing in full compliance with MIL-STD-883, Revision D.

Second, selected products are available to the SMD (Standardized Military Drawing) program administered by DESC. These products are not only fully MIL-STD-883D compliant, but are also screened to the electrical requirements of the applicable military drawing.

Third, selected products are available as JAN devices. These products are processed in full accordance with MIL-I-38535B and they are screened to the electrical requirements of the applicable JAN slash sheet.

Product Packaging

All packages for military product are hermetic. A look at the package appendix in the back of this data book will give the reader an appreciation of the variety of packages offered. Included are cerDIPs, windowed CerDIPs, leadless chip carriers (LCCs), windowed leadless chip carriers, cerpaks, windowed cerpaks, quad cerpaks, windowed quad cerpaks, bottom-brazed flatpacks, and pin grid arrays.

Summary

Cypress Semiconductor is committed to the support of the military marketplace. Our commitment is demonstrated by our product designs, our DESC-certified facility, our documentation and traceability, our quality and reliability programs, our support of all levels of military processing, and by our leadership in special packaging.

PLDs

	Organization	Pins	Part Number	JAN/SMD Number[1]*	Speed (ns/MHz)	I_{CC} (mA @ ns/MHz)	883 Availability
PAL20	16L8, 16R8, 16R6, 16R4	20	PAL16XX	5962-92338(O)	t_{PD} = 7, 10	180 @ 7	Now
PALC20	16L8, 16R8, 16R6, 16R4	20	PALC16XX	5962-88678(W)	t_{PD} = 20, 30	70 @ 20	Now
PALC20	16L8, 16R8, 16R6, 16R4	20	PALC16XX	5962-88713(O)	t_{PD} = 20, 30	70 @ 20	Now
PLD24	22V10C—Macrocell	24S	PAL22V10C	5962-91760(O)	$t_{PD/S/CO}$ = 10/3.6/7.5	190 @ 10	Now
PLD24	22V10C—Macrocell	24S	PAL22VP10C	5962-91760(O)	$t_{PD/S/CO}$ = 10/3.6/7.5	190 @ 10	Now
PLDC24	22V10—Macrocell	24S	PALC22V10	5962-87539(W)	$t_{PD/S/CO}$ = 25/18/15	100 @ 25	Now
PLD24	22V10—Macrocell	24S	PALC22V10B	5962-87539(W)	$t_{PD/S/CO}$ = 20/17/15	100 @ 20	Now
PLDC24	22V10—Macrocell	24S	PALC22V10	5962-88670(O)	$t_{PD/S/CO}$ = 25/18/15	100 @ 25	Now
PLD24	22V10—Macrocell	24S	PALC22V10B	5962-88670(O)	$t_{PD/S/CO}$ = 15/12/10	120 @ 15	Now
PLDC24	22V10—Macrocell	24S	PALC22V10B	M38510/507(W)	$t_{PD/S/CO}$ = 15/12/10	120 @ 15	Now
PLDC24	22V10—Macrocell	24S	PALC22V10B	M38510/508(O)	$t_{PD/S/CO}$ = 15/12/10	120 @ 15	Now
PLDC24	22V10D—Macrocell	24S	PALC22V10D	5962-89841(O)	$t_{PD/S/CO}$ = 10/6/7	130@10	Now
PLDC24	20G10—Generic	24S	PLDC20G10	5962-88637(O)	$t_{PD/S/CO}$ = 20/17/15	80 @ 30	Now
PLDC24	20RA10—Asynchronous	24S	PLD20RA10	5962-90555(O)	$t_{PD/SU/CO}$ = 20/10/20	100 @ 25	Now
PLDC28	7C330—State Machine	28S	CY7C330	5962-89546(W)	50, 40, 28 MHz	180 @ 40 MHz	Now
PLDC28	7C330—State Machine	28S	CY7C330	5926-90802(O)	50, 40, 28 MHz	180 @ 40 MHz	Now
PLDC28	7C331—Asynchronous	28S	CY7C331	5962-90754(W)	t_{PD} = 25, 30, 40	200 @ 20 MHz	Now
PLDC28	7C331—Asynchronous	28S	CY7C331	5962-89855(O)	t_{PD} = 25, 30, 40	200 @ 20 MHz	Now
PLDC28	7C332—Combinatorial	28S	CY7C332	5962-91584(W)	t_{PD} = 20, 25, 30	200 @ 24 MHz	Now
PLD28	7C335—Synchronous	28S	CY7C335	5862-94510(W)	f_{MAX5} = 66.6, 50, 83	160 @ 66.6 MHz	Now

CPLDs

	Organization	Pins	Part Number	JAN/SMD Number[1]*	Speed (ns/MHz)	I_{CC} (mA @ ns/MHz)	883 Availability
MAX28	7C344—32 Macrocell	28S	CY7C344	5962-90611(W)	t_{PD} = 25, 35	220@25	Now
MAX40	7C343—64 Macrocell	40/44	CY7C343	5962-92158(W)	t_{PD} = 25, 30, 35	225@25	Now
MAX68	7C342—128 Macrocell	68	CY7C342	5962-89468(W)	t_{PD} = 30, 35, 40	320@30	Now
MAX84	7C341—192 Macrocell	84	CY7C341	5962-92062(W)	t_{PD} = 30, 35, 40	480@30	Now
MAX100	7C346—128 Macrocell	84/100	CY7C346	5962-91344(W)	t_{PD} = 30, 35	320@35	Now
PLDC28	7C361—State Machine	28S	CY7C361		100, 83, 66 MHz	150 @ 100 MHz	Now
FLASH370 −44	7C371—32 Macrocell	44	CY7C371	5962-94684(O)	$f_{MAX}/t_S/t_{CO}$=83MHz/ 10/10	260@83	Now
FLASH370 −44	7C372—64 Macrocell	44	CY7C372		$f_{MAX}/t_S/t_{CO}$=83MHz/ 8/8	300@83	3Q94
FLASH370 −84	7C373—64 Macrocell	84	CY7C373		$f_{MAX}/t_S/t_{CO}$=83MHz/ 8/8	300@83	3Q94
FLASH370 −84	7C374—128 Macrocell	84	CY7C374		$f_{MAX}/t_S/t_{CO}$=83MHz/ 8/8	370@83	Now
FLASH370 −160	7C375—128 Macrocell	160	CY7C375		$f_{MAX}/t_S/t_{CO}$=83MHz/ 8/8	370@83	Now
FLASH370 −160	7C376—192 Macrocell	160	CY7C376		$f_{MAX}/t_S/t_{CO}$=83MHz/ 12/12	300/TBD	4Q95
FLASH370 −240	7C377—192 Macrocell	240	CY7C377		$f_{MAX}/t_S/t_{CO}$=83MHz/ 12/12	300/TBD	4Q95
FLASH370 −160	7C378—256 Macrocell	160	CY7C378		$f_{MAX}/t_S/t_{CO}$=83MHz/ 12/12	300/TBD	2Q95
FLASH370 −240	7C379—256 Macrocell	240	CY7C379		$f_{MAX}/t_S/t_{CO}$=83MHz/ 12/12	300/TBD	2Q95

FPGAs

	Organization	Pins	Part Number	JAN/SMD Number[1]*	Speed (ns/MHz)	I_{CC} (mA @ ns/MHz)	883 Availability
1K FPGA	CMOS 8 x 12	68	CY7C382A		−0, −1	20	3Q94
2K FPGA	CMOS 12 x 16	84	CY7C384A		−0, −1	20	4Q94
4K FPGA	CMOS 16 x 24	145/ 160	CY7C386A		−0, −1	20	Now
8K FPGA	CMOS 24 x 32	145/ 160/ 208	CY7C387A/8A		−0, −1	20	1Q95

Notes:

The Cypress facility at 3901 North First Street in San Jose, CA is DESC-certified for JAN class B production.

All of the above products are available with processing to MIL-STD-883D at a minimum. Many of these products are also available either to SMD (Standardized Military Drawings) or to JAN slash sheets.

The speed and power specifications listed above cover the full military temperature range.

22S stands for 22-pin 300-mil DIP.
24S stands for 24-pin 300-mil DIP.
28S stands for 28-pin 300-mil DIP.
32S stands for 32-pin 300-mil DIP.

Military Ordering Information

Cypress Semiconductor fully supports the DESC standardized Military Drawing Program for devices that are compliant to the Class B requirements of MIL-STD-883D.

Listed below are the SMDs for which Cypress is an approved source of supply. Please contact your local Cypress representative for the latest SMD update.

DESC SMD (Standardized Military Drawing) Approvals[1]

SMD Number	Cypress[2] Part Number	Package[3] Description	Package[3] Type	Product Description
5962-87539 01LX	PALC22V10-25WMB	24.3 DIP	W14	24-Pin CMOS UV EPLD
5962-87539 013X	PALC22V10-25QMB	28 S LCC	Q64	24-Pin CMOS UV EPLD
5962-87539 02LX	PALC22V10-30WMB	24.3 DIP	W14	24-Pin CMOS UV EPLD
5962-87539 023X	PALC22V10-30QMB	28 S LCC	Q64	24-Pin CMOS UV EPLD
5962-87539 03LX	PALC22V10-40WMB	24.3 DIP	W14	24-Pin CMOS UV EPLD
5962-87539 04LX	PALC22V10B-20WMB	24.3 DIP	W14	24-Pin CMOS UV EPLD
5962-87539 043X	PALC22V10B-20QMB	28 S LCC	Q64	24-Pin CMOS UV EPLD
5962-88637 01KX	PLDC20G10-40KMB	24 CP	K73	Generic CMOS PLD
5962-88637 01LX	PLDC20G10-40DMB	24.3 DIP	D14	Generic CMOS PLD
5962-88637 02KX	PLDC20G10-30KMB	24 CP	K73	Generic CMOS PLD
5962-88637 02LX	PLDC20G10-30DMB	24.3 DIP	D14	Generic CMOS PLD
5962-88637 023X	PLDC20G10-30LMB	28 S LCC	L64	Generic CMOS PLD
5962-88670 01KX	PALC22V10-25KMB	24 CP	K73	24-Pin CMOS PLD
5962-88670 01LX	PALC22V10-25DMB	24.3 DIP	D14	24-Pin CMOS PLD
5962-88670 013X	PALC22V10-25LMB	28 S LCC	L64	24-Pin CMOS PLD
5962-88670 02KX	PALC22V10-30KMB	24 CP	K73	24-Pin CMOS PLD
5962-88670 02LX	PALC22V10-30DMB	24.3 DIP	D14	24-Pin CMOS PLD
5962-88670 023X	PALC22V10-30LMB	28 S LCC	L64	24-Pin CMOS PLD
5962-88670 03KX	PALC22V10-40KMB	24 CP	K73	24-Pin CMOS PLD
5962-88670 03LX	PALC22V10-40DMB	24.3 DIP	D14	24-Pin CMOS PLD
5962-88670 04KX	PALC22V10B-20KMB	24 CP	K73	24-Pin CMOS PLD
5962-88670 04LX	PALC22V10B-20DMB	24.3 DIP	D14	24-Pin CMOS PLD
5962-88670 043X	PALC22V10B-20LMB	28 S LCC	L64	24-Pin CMOS PLD
5962-88670 05KX	PALC22V10B-15KMB	24 CP	K73	24-Pin CMOS PLD
5962-88670 05LX	PALC22V10B-15DMB	24.3 DIP	D14	24-Pin CMOS PLD
5962-88670 053X	PALC22V10B-15LMB	28 S LCC	L64	24-Pin CMOS PLD
5962-88678 01XX	PALC16L8-40QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962-88678 02XX	PALC16R8-40QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962-88678 03RX	PALC16R6-40WMB	20.3 DIP	W6	20-Pin CMOS UV EPLD
5962-88678 03XX	PALC16R6-40QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962-88678 04RX	PALC16R4-40WMB	20.3 DIP	W6	20-Pin CMOS UV EPLD
5962-88678 04XX	PALC16R4-40QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962-88678 07XX	PALC16R6-30QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962-88678 09RX	PALC16L8-20WMB	20.3 DIP	W6	20-Pin CMOS UV EPLD
5962-88678 09XX	PALC16L8-20QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962-88678 10RX	PALC16R8-20WMB	20.3 DIP	W6	20-Pin CMOS UV EPLD
5962-88678 10XX	PALC16R8-20QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962-88678 11RX	PALC16R6-20WMB	20.3 DIP	W6	20-Pin CMOS UV EPLD
5962-88678 11XX	PALC16R6-20QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962-88678 12RX	PALC16R4-20WMB	20.3 DIP	W6	20-Pin CMOS UV EPLD
5962-88678 12XX	PALC16R4-20QMB	20 S LCC	Q61	20-Pin CMOS UV EPLD
5962-88713 01RX	PALC16L8-40DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 05RX	PALC16L8-30DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 05XX	PALC16L8-30LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 06RX	PALC16R8-30DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 07RX	PALC16R6-30DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 07XX	PALC16R6-30LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 08RX	PALC16R4-30DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 08XX	PALC16R4-30LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 09RX	PALC16L8-20DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 09XX	PALC16L8-20LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 10RX	PALC16R8-20DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 10XX	PALC16R8-20LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 11RX	PALC16R6-20DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 11XX	PALC16R6-20LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 12RX	PALC16R4-20DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 12XX	PALC16R4-20LMB	20 S LCC	L61	20-Pin CMOS PLD

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
5962-89468 01XX	CY7C342-35RMB	68 PGA	H81	128-Macrocell UV EPLD
5962-89468 01YX	CY7C342-35HMB	68 SOJ	R68	128-Macrocell UV EPLD
5962-89468 01ZX	CY7C342-35TMB	68 QFP	T91	128-Macrocell UV EPLD
5962-89546 01XX	CY7C330-28WMB	28.3 DIP	W22	PLD State Machine
5962-89546 02XX	CY7C330-40WMB	28.3 DIP	W22	PLD State Machine
5962-89546 02YX	CY7C330-40TMB	28 CP	T74	PLD State Machine
5962-89546 023X	CY7C330-40QMB	28 S LCC	Q64	PLD State Machine
5962-89546 03XX	CY7C330-50WMB	28.3 DIP	W22	PLD State Machine
5962-89546 03YX	CY7C330-50TMB	28 CP	T74	PLD State Machine
5962-89546 033X	CY7C330-50QMB	28 S LCC	Q64	PLD State Machine
5962-89841 01KX	PALC22V10D-30KMB	24 CP	K73	CMOS EE PLD
5962-89841 01LX	PALC22V10D-30DMB	24.3 DIP	D14	CMOS EE PLD
5962-89841 013X	PALC22V10D-30LMB	28 S LCC	L64	CMOS EE PLD
5962-89841 02KX	PALC22V10D-20KMB	24 CP	K73	CMOS EE PLD
5962-89841 02LX	PALC22V10D-20DMB	24.3 DIP	D14	CMOS EE PLD
5962-89841 023X	PALC22V10D-20LMB	28 S LCC	L64	CMOS EE PLD
5962-89841 03KX	PALC22V10D-15KMB	24 CP	K73	CMOS EE PLD
5962-89841 03LX	PALC22V10D-15DMB	24.3 DIP	D14	CMOS EE PLD
5962-89841 033X	PALC22V10D-15LMB	28 S LCC	L64	CMOS EE PLD
5962-89841 04KX	PALC22V10D-25KMB	24 CP	K73	CMOS EE PLD
5962-89841 04LX	PALC22V10D-25DMB	24.3 DIP	D14	CMOS EE PLD
5962-89841 043X	PALC22V10D-25LMB	28 S LCC	L64	CMOS EE PLD
5962-89841 05KX	PALC22V10D-15KMB	24 CP	K73	CMOS EE PLD
5962-89841 05LX	PALC22V10D-15DMB	24.3 DIP	D14	CMOS EE PLD
5962-89841 053X	PALC22V10D-15LMB	28 S LCC	L64	CMOS EE PLD
5962-89841 06KX	PALC22V10D-10KMB	24 CP	K73	CMOS EE PLD
5962-89841 06LX	PALC22V10D-10DMB	24.3 DIP	D14	CMOS EE PLD
5962-89841 063X	PALC22V10D-10LMB	28 S LCC	L64	CMOS EE PLD
5962-89855 01MYX	CY7C331-40KMB	28 CP	K74	Asynchronous PLD
5962-89855 01MZX	CY7C331-40YMB	28 S JCQ	Y64	Asynchronous PLD
5962-89855 01M3X	CY7C331-40LMB	28 S LCC	L64	Asynchronous PLD
5962-89855 02MXX	CY7C331-30DMB	28.3 DIP	D22	Asynchronous PLD
5962-89855 02MYX	CY7C331-30KMB	28 CP	K74	Asynchronous PLD
5962-89855 02MZX	CY7C331-30YMB	28 S JCQ	Y64	Asynchronous PLD
5962-89855 03MXX	CY7C331-25DMB	28.3 DIP	D22	Asynchronous PLD
5962-89855 03MYX	CY7C331-25KMB	28 CP	K74	Asynchronous PLD
5962-89855 03MZX	CY7C331-25YMB	28 S JCQ	Y64	Asynchronous PLD
5962-89855 03M3X	CY7C331-25LMB	28 S LCC	L64	Asynchronous PLD
5962-90555 01LX	PLDC20RA10-35DMB	24.3 DIP	D14	Asynchronous CMOS OTP PLD
5962-90555 02KX	PLDC20RA10-25KMB	24 CP	K73	Asynchronous CMOS OTP PLD
5962-90555 02LX	PLDC20RA10-25DMB	24.3 DIP	D14	Asynchronous CMOS OTP PLD
5962-90555 023X	PLDC20RA10-25LMB	28 S LCC	L64	Asynchronous CMOS OTP PLD
5962-90555 03KX	PLDC20RA10-20KMB	24 CP	K73	Asynchronous CMOS OTP PLD
5962-90555 03LX	PLDC20RA10-20DMB	24.3 DIP	D14	Asynchronous CMOS OTP PLD
5962-90754 01MYX	CY7C331-40TMB	28 CP	T74	Asynchronous UV PLD
5962-90754 01MZX	CY7C331-40HMB	28 S JCQ	H64	Asynchronous UV PLD
5962-90754 02MYX	CY7C331-30TMB	28 CP	T74	Asynchronous UV PLD
5962-90754 02MZX	CY7C331-30HMB	28 S JCQ	H64	Asynchronous UV PLD
5962-90754 02M3X	CY7C331-30QMB	28 S LCC	Q64	Asynchronous UV PLD
5962-90754 03MXX	CY7C331-25WMB	28.3 DIP	W22	Asynchronous UV PLD
5962-90754 03MYX	CY7C331-25TMB	28 CP	T74	Asynchronous UV PLD
5962-90754 03MZX	CY7C331-25HMB	28 S JCQ	H64	Asynchronous UV PLD
5962-90754 03M3X	CY7C331-25QMB	28 S LCC	Q64	Asynchronous UV PLD
5962-91584 01MYX	CY7C332-25TMB	28 CP	T74	Registered Combinatorial UV EPLD
5962-91584 01MZX	CY7C332-25HMB	28 S JCQ	H64	Registered Combinatorial UV EPLD
5962-91584 02MYX	CY7C332-20TMB	28 CP	T74	Registered Combinatorial UV EPLD
5962-91584 02MZX	CY7C332-20HMB	28 S JCQ	H64	Registered Combinatorial UV EPLD
5962-91584 02M3X	CY7C332-20QMB	28 S LCC	Q64	Registered Combinatorial UV EPLD

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
5962-91760 01M3X	PAL22V10C-15LMB	28 S LCC	L64	BiCMOS OTP PLD
5962-91760 02M3X	PAL22V10C-12LMB	28 S LCC	L64	BiCMOS OTP PLD
5962-91760 03M3X	PAL22V10C-10LMB	28 S LCC	L64	BiCMOS OTP PLD
5962-91760 04M3X	PAL22VP10C-15LMB	28 S LCC	L64	BiCMOS OTP PLD
5962-91760 05M3X	PAL22VP10C-12LMB	28 S LCC	L64	BiCMOS OTP PLD
5962-91760 06M3X	PAL22VP10C-10LMB	28 S LCC	L64	BiCMOS OTP PLD
5962-92062 01MXX	CY7C341-40HMB	84 S JCQ	H84	192-Macrocell UV EPLD
5962-92062 01MYX	CY7C341-40RMB	84 PGA	R84	192-Macrocell UV EPLD
5962-92062 02MXX	CY7C341-30HMB	84 S JCQ	H84	192-Macrocell UV EPLD
5962-92062 02MYX	CY7C341-30RMB	84 PGA	R84	192-Macrocell UV EPLD
5962-92158 02MXX	CY7C343-30HMB	44 S JCQ	H67	64-Macrocell UV EPLD
5962-92338 01MRX	PAL16L8-10DMB	20.3 DIP	D6	20-Pin BiCMOS PLD
5962-92338 01MSX	PAL16L8-10KMB	20 CP	K71	20-Pin BiCMOS PLD
5962-92338 01MXX	PAL16L8-10LMB	20 S LCC	L61	20-Pin BiCMOS PLD
5962-92338 02MRX	PAL16R8-10DMB	20.3 DIP	D6	20-Pin BiCMOS PLD
5962-92338 02MSX	PAL16R8-10KMB	20 CP	K71	20-Pin BiCMOS PLD
5962-92338 02MXX	PAL16R8-10LMB	20 S LCC	L61	20-Pin BiCMOS PLD
5962-92338 03MRX	PAL16R6-10DMB	20.3 DIP	D6	20-Pin BiCMOS PLD
5962-92338 03MSX	PAL16R6-10KMB	20 CP	K71	20-Pin BiCMOS PLD
5962-92338 03MXX	PAL16R6-10LMB	20 S LCC	L61	20-Pin BiCMOS PLD
5962-92338 04MRX	PAL16R4-10DMB	20.3 DIP	D6	20-Pin BiCMOS PLD
5962-92338 04MSX	PAL16R4-10KMB	20 CP	K71	20-Pin BiCMOS PLD
5962-92338 04MXX	PAL16R4-10LMB	20 S LCC	L61	20-Pin BiCMOS PLD
5962-92338 05MRX	PAL16L8-7DMB	20.3 DIP	D6	20-Pin BiCMOS PLD
5962-92338 05MSX	PAL16L8-7KMB	20 CP	K71	20-Pin BiCMOS PLD
5962-92338 05MXX	PAL16L8-7LMB	20 S LCC	L61	20-Pin BiCMOS PLD
5962-92338 06MRX	PAL16R8-7DMB	20.3 DIP	D6	20-Pin BiCMOS PLD
5962-92338 06MSX	PAL16R8-7KMB	20 CP	K71	20-Pin BiCMOS PLD
5962-92338 06MXX	PAL16R8-7LMB	20 S LCC	L61	20-Pin BiCMOS PLD
5962-92338 07MRX	PAL16R6-7DMB	20.3 DIP	D6	20-Pin BiCMOS PLD
5962-92338 07MSX	PAL16R6-7KMB	20 CP	K71	20-Pin BiCMOS PLD
5962-92338 07MXX	PAL16R6-7LMB	20 S LCC	L61	20-Pin BiCMOS PLD
5962-92338 08MRX	PAL16R4-7DMB	20.3 DIP	D6	20-Pin BiCMOS PLD
5962-92338 08MSX	PAL16R4-7KMB	20 CP	K71	20-Pin BiCMOS PLD
5962-92338 08MXX	PAL16R4-7LMB	20 S LCC	L61	20-Pin BiCMOS PLD
5962-93144 01MZX	CY7C346-35RMB	100 PGA	R100	128-Macrocell UV EPLD
5962-93144 01MUX	CY7C346-35HMB	84 S JCQ	H84	128-Macrocell UV EPLD
5962-93144 02MZX	CY7C346-30RMB	100 PGA	R100	128-Macrocell UV EPLD
5962-93144 02MUX	CY7C346-30HMB	84 S JCQ	H84	128-Macrocell UV EPLD

Notes:

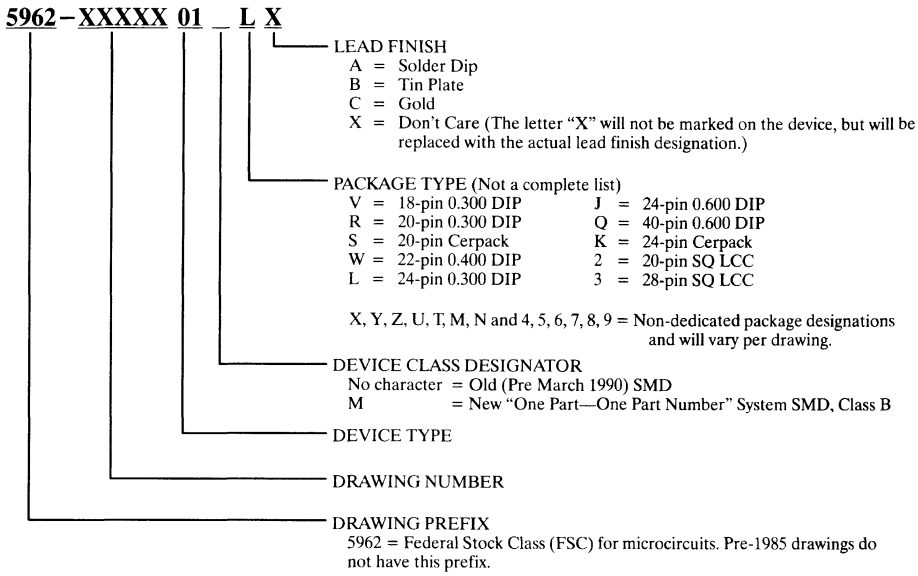
1. Devices listed have been approved by DESC for the SMD indicated as of the date of publication. Contact your local Cypress representative, or the Cypress SMD Hotline at 408/943-2716, for the latest update.
2. Use the SMD part number as the ordering code.
3. Package: 24.3 DIP = 24-pin 0.300″ DIP;
   24.6 DIP = 24-pin 0.600″ DIP;
   28 R LCC = 28 terminal rectangular LCC,
   S = Square LCC, TLCC = Thin LCC
   24 CP = 24-pin ceramic flatpack (Configuration 1);
   FP = brazed flatpack;
   PGA = Pin Grid Array.

SMD Hotline: 408/943-2716

JAN M38510 Qualifications

JAN Number	Cypress[2] Part Number	Package[3]		Product Description	Qualification Status
		Description	Type		
JM 38510/50701BLA	PALC22V10B-30WMB	24.3 DIP	W14	CMOS UV PLD	Qualified
JM 38510/50701B3A	PALC22V10B-30QMB	28 S LCC	Q64	CMOS UV PLD	Qualified
JM 38510/50702BLA	PALC22V10B-25WMB	24.3 DIP	W14	CMOS UV PLD	Qualified
JM 38510/50702B3A	PALC22V10B-25QMB	28 S LCC	Q64	CMOS UV PLD	Qualified
JM 38510/50703BLA	PALC22V10B-20WMB	24.3 DIP	W14	CMOS UV PLD	Qualified
JM 38510/50703B3A	PALC22V10B-20QMB	28 S LCC	Q64	CMOS UV PLD	Qualified
JM 38510/50704BLA	PALC22V10B-15WMB	24.3 DIP	W14	CMOS UV PLD	Qualified
JM 38510/50704B3A	PALC22V10B-15QMB	28 S LCC	Q64	CMOS UV PLD	Qualified
JM 38510/50801BLA	PALC22V10B-30DMB	24.3 DIP	D14	CMOS PLD	Qualified
JM 38510/50801BKA	PALC22V10B-30KMB	24 CP	K73	CMOS PLD	Qualified
JM 38510/50801B3A	PALC22V10B-30LMB	28 S LCC	L64	CMOS PLD	Qualified
JM 38510/50802BLA	PALC22V10B-25DMB	24.3 DIP	D14	CMOS PLD	Qualified
JM 38510/50802BKA	PALC22V10B-25KMB	24 CP	K73	CMOS PLD	Qualified
JM 38510/50802B3A	PALC22V10B-25LMB	28 S LCC	L64	CMOS PLD	Qualified
JM 38510/50803BLA	PALC22V10B-20DMB	24.3 DIP	D14	CMOS PLD	Qualified
JM 38510/50803BKA	PALC22V10B-20KMB	24 CP	K73	CMOS PLD	Qualified
JM 38510/50803B3A	PALC22V10B-20LMB	28 S LCC	L64	CMOS PLD	Qualified
JM 38510/50804BLA	PALC22V10B-15DMB	24.3 DIP	D14	CMOS PLD	Qualified
JM 38510/50804BKA	PALC22V10B-15KMB	24 CP	K73	CMOS PLD	Qualified
JM 38510/50804B3A	PALC22V10B-15LMB	28 S LCC	L64	CMOS PLD	Qualified

SMD Ordering Information



Cypress Military Marking Information

Manufacturer's identification:

Cypress Logo, CYPRESS, CYP, and CY are trademarks of Cypress Semiconductor Corporation.

Manufacturer's designating symbol or CAGE CODE:

Designating symbol = CETK or ETK

CAGE CODE/FSCM Number = 65786

Country of origin:

USA = United States of America

THA = Thailand

In general, the codes for all products (except modules) follow the format below.

PAL & PLD

PREFIX	DEVICE	SUFFIX	FAMILY
PAL C	16R8	-20 DMB	PAL 20
PAL C	22V10	-15 WMB	PAL 24 VARIABLE PRODUCT TERMS
PLD C	20G10	-20 WMB	GENERIC PLD 24
CY	7C330	-50 DMB	PLD SYNCHRONOUS STATE MACHINE
PALCE	16V8	-25 DMB	FLASH-ERASABLE PAL20

e.g., PALC16R8-20DMB

Cypress FSCM #65786

Small PLDs 2

Section Contents

Small PLDs (Programmable Logic Devices)

Introduction to Cypress PLDs

Cypress PLD Family Features

Cypress Semiconductor's PLD family offers the user a wide range of programmable logic solutions that incorporate leading-edge circuit design techniques as well as diverse process technology capabilities. This allows Cypress PLD users to select PLDs that best suit the needs of their particular high-performance system, regardless of whether speed, power consumption, density, or device flexibility are the critical requirements imposed by the system.

Cypress offers enhanced-performance industry-standard 20- and 24-pin device architectures as well as proprietary 28-pin application-tailored architectures. The range of technologies offered includes leading-edge 0.8-micron CMOS EPROM for high speed, low power, and high density, 0.65-micron FLASH technology for high speed, low power and electrical alterability, and 0.5-micron BiCMOS for high-speed, power-sensitive applications.

The reprogrammable memory cells used by Cypress serve the same purpose as the fuse used in most bipolar PLD devices. Before programming, the AND gates or product terms are connected via the reprogrammable memory cell to both the true and complement inputs. When the reprogrammable memory cell is programmed, the inputs from a gate or product term are disconnected. Programming alters the transistor threshold of each cell so that no conduction can occur, which is equivalent to disconnecting the input from the gate or product term. This is similar to "blowing" the fuses of BiCMOS or bipolar fusible devices, which disconnects the input gate from the product term. Selective programming of each of these reprogrammable memory cells enables the specific logic function to be implemented by the user.

The programmability of Cypress's PLDs allows the users to customize every device in a number of ways to implement their unique logic requirements. Using PLDs in place of SSI or MSI components results in more effective utilization of board space, reduced cost and increased reliability. The flexibility afforded by these PLDs allows the designer to quickly and effectively implement a number of logic functions ranging from random logic gate replacement to complex combinatorial logic functions.

The PLD family implements the familiar "sum of products" logic by using a programmable AND array whose output terms feed a fixed OR array. The sum of these can be expressed in a Boolean transfer function and is limited only by the number of product terms available in the AND-OR array. A variety of different sizes and architectures are available. This allows for more efficient logic optimization by matching input, output, and product terms to the desired application.

PLD Notation

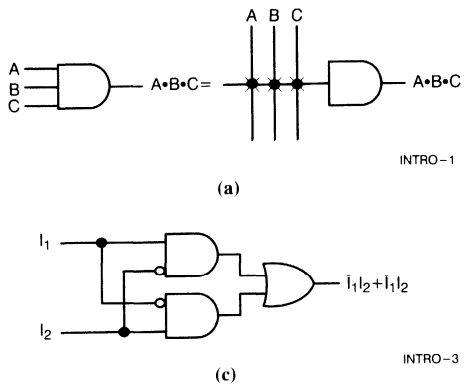
To reduce confusion and to have an orderly way of representing the complex logic networks, logic diagrams are provided for the various part types. In order to be useful, Cypress logic diagrams employ a common logic convention that is easy to use. *Figure 1* shows the adopted convention. In part (a), an "×" represents an unprogrammed EPROM cell or intact fuse link that is used to perform the logical AND operation upon the input terms. The convention adopted does not imply that the input terms are connected on the common line that is indicated. A further extension of this convention is shown in part (b), which shows the implementation of a simple transfer function. The normal logic representation of the transfer function logic convention is shown in part (c).

PLD Circuit Configurations

Cypress PLDs have several different output configurations that cover a wide spectrum of applications. The available output configurations offer the user the benefits of both lower package counts and reduced costs when used. This approach allows designers to select PLDs that best fit their applications. An example of some of the configurations that are available are listed below.

Programmable I/O

Figure 2 illustrates the programmable I/O offered in the Cypress PLD family that allows product terms to directly control the outputs of the device. One product term is used to directly control the three-state output buffer, which then gates the summation of the remaining terms to the output pin. The output of this summation can be fed back into the PLD as an input to the array. This programmable I/O feature allows the PLD to drive the output pin when the three-state output is enabled or, when the three-state output is disabled, the I/O pin can be used as an input to the array.



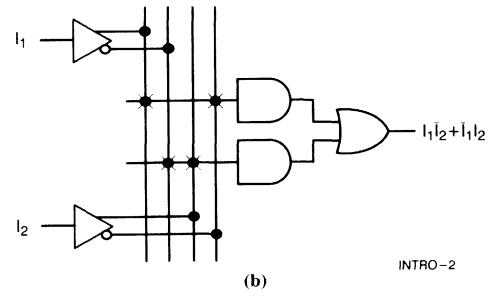


Figure 1. Logic Diagram Conventions

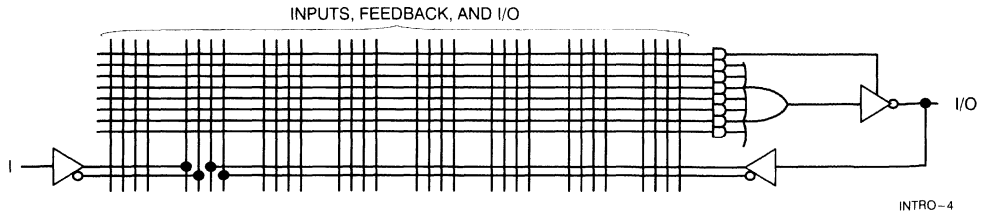


Figure 2. Programmable I/O

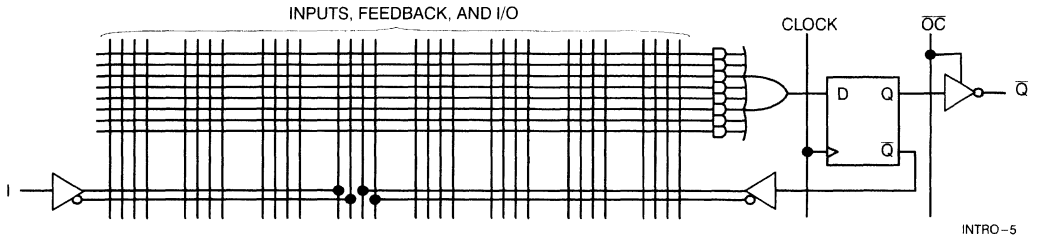


Figure 3. Registered Outputs with Feedback

Registered Outputs with Feedback

Figure 3 illustrates the registered outputs offered on a number of the Cypress PLDs which allow any of these circuits to function as a state sequencer. The summation of the product terms is stored in the D-type output flip-flop on the rising edge of the system clock. The Q output of the flip-flop can then be gated to the output pin by enabling the three-state output buffer. The output of the flip-flop can also be fed back into the array as an input term. The output feedback feature allows the PLD to remember and then alter its function based upon that state. This circuit can be used to execute such functions as counting, skip, shift, and branch.

Programmable Macrocell

The programmable macrocell, illustrated in *Figure 4*, provides the capability of defining the architecture of each output individually. Each of the potential outputs may be specified to be "registered" or "combinatorial." Polarity of each output may also be individually selected allowing complete flexibility of output configuration. Further configurability is provided through "array" configurable "output enable" for each potential output. This feature allows the outputs to be reconfigured as inputs on an individual basis or alternately used as a bidirectional I/O controlled by the programmable array (see *Figure 5*).

Buried Register Feedback

The CY7C331 and CY7C335 PLDs provide registers that may be "buried" or "hidden" by electing feedback of the register output. These buried registers, which are useful in state machines, may be implemented without sacrificing the use of the associated device pin as an input. In previous PLDs, when the feedback path was activated, the input pin-path to the logic array was blocked. The proprietary CY7C335 reprogrammable synchronous state machine macrocell illustrates the shared input multiplexer, which provides an alternative input path for the I/O pin associated with a buried macrocell register (*Figure 6*). Each pair of macrocells shares an input multiplexer, and as long as alternate macrocells are buried, up to six of the twelve output registers can be buried without the loss of any I/O pins as inputs. The CY7C335 also contains four dedicated hidden macrocells with no external output that are used as additional state registers for creating high-performance state machines (*Figure 7*).

Asynchronous Register Control

Cypress also offers PLDs that may be used in asynchronous systems in which register clock, set, and reset are controlled by the outputs of the product term array. The clock signal is created by the processing of external inputs and/or internal feedback by the logic of the product term array, which is then routed to the register clock. The register set and reset are similarly controlled by product term outputs and can be triggered at any time independent of the register clock in response to external and/or feedback inputs processed by the logic array. The proprietary CY7C331 Asynchronous Registered PLD, for which the I/O macrocell is illustrated in *Figure 8*, is an example of such a device. The register clock, set, and reset functions of the CY7C331 are all controlled by product terms and are dependent only on input signal timing and combinatorial delay through the device logic array to enable their respective functions.

Input Register Cell

Other Cypress PLDs provide input register cells to capture short duration inputs that would not otherwise be present at the inputs long enough to allow the device to respond. The proprietary CY7C335 Reprogrammable Synchronous State Machine provides these input register cells (*Figure 9*). The clock for the input register may be provided from one of two external clock input pins selectable by a configuration bit, C4, dedicated for this purpose for each input register. This choice of input register clock allows signals to be captured and processed from two independent system sources, each controlled by its own independent clock. These input register cells are provided within I/O macrocells, as well as for dedicated input pins.

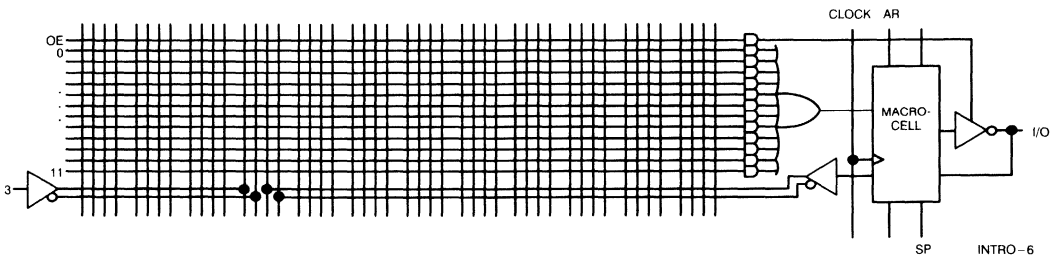


Figure 4. Programmable Macrocell

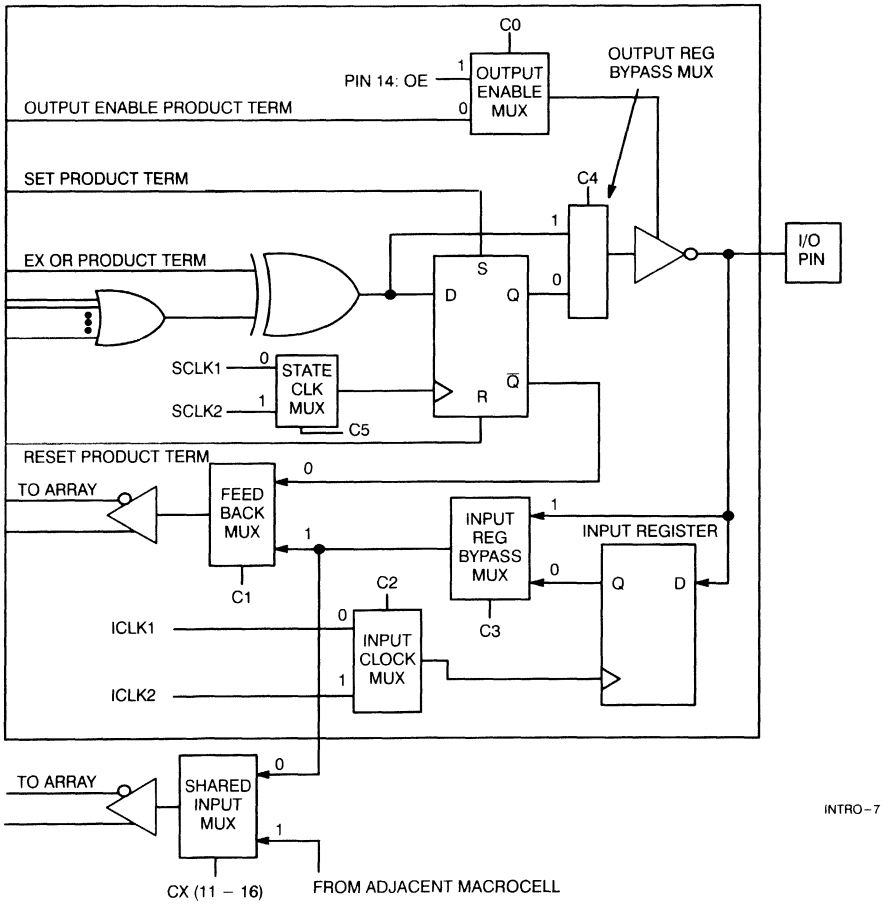


Figure 5. CY7C335 I/O Macrocell

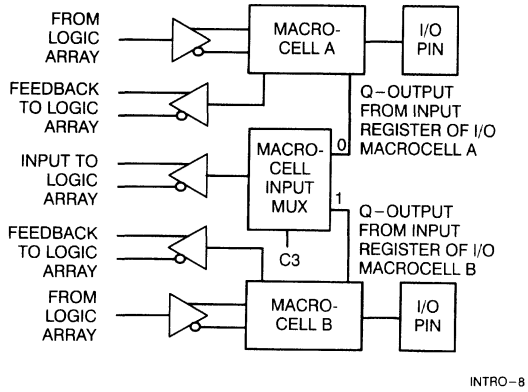


Figure 6. CY7C335 I/O Macrocell Pair Shared Input MUX

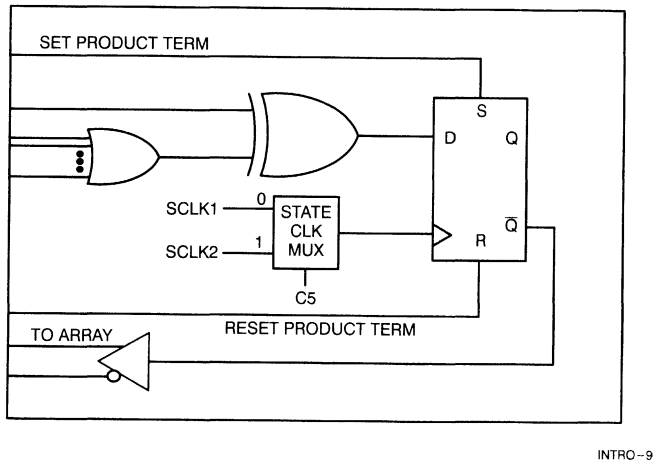


Figure 7. CY7C335 Hidden Macrocell

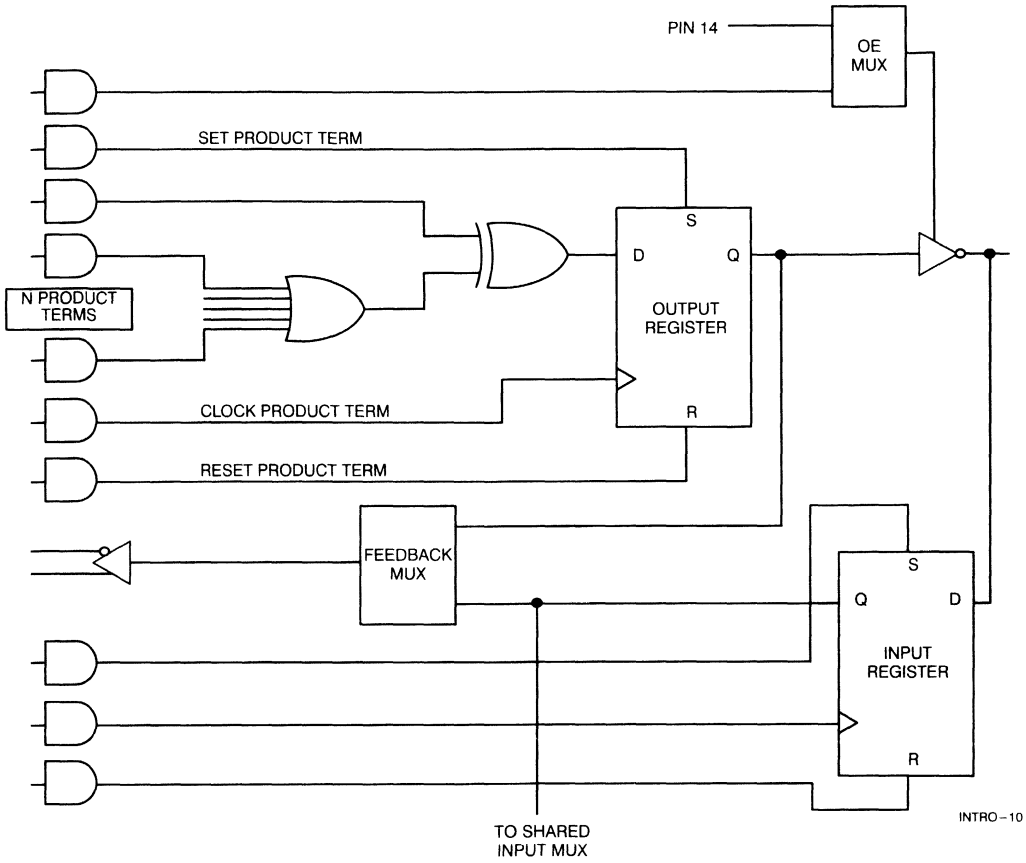


Figure 8. CY7C331 Registered Asynchronous Macrocell

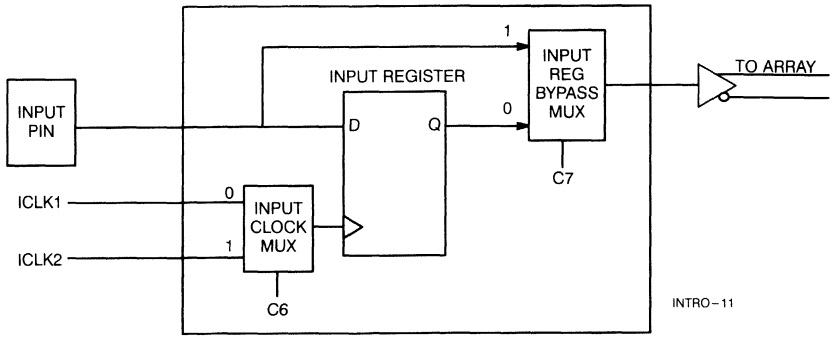


Figure 9. CY7C335 Input Macrocell

Document #: 38-00165-B

PAL®20 Series
16L8/16R8
16R6/16R4

4.5-ns, Industry-Standard PLDs

Features

- **Ultra high speed supports today's and tomorrow's fastest microprocessors**
  - **— t_{PD} = 4.5 ns**
  - **— t_S = 2.5 ns**
  - **— f_{MAX} = 142.9 MHz (external)**
- **Popular industry standard architectures**
- **Power-up RESET**
- **High reliability**
  - **— Proven Ti-W fuses**
  - **— AC and DC tested at the factory**
- **Security fuse**

Functional Description

Cypress PAL20 Series devices consist of the PAL16L8, PAL16R8, PAL16R6, and PAL16R4. Using BiCMOS process and Ti-W fuses, these devices implement the familiar sum-of-products (AND-OR) logic structure.

The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms while the OR array sums selected terms at the outputs.

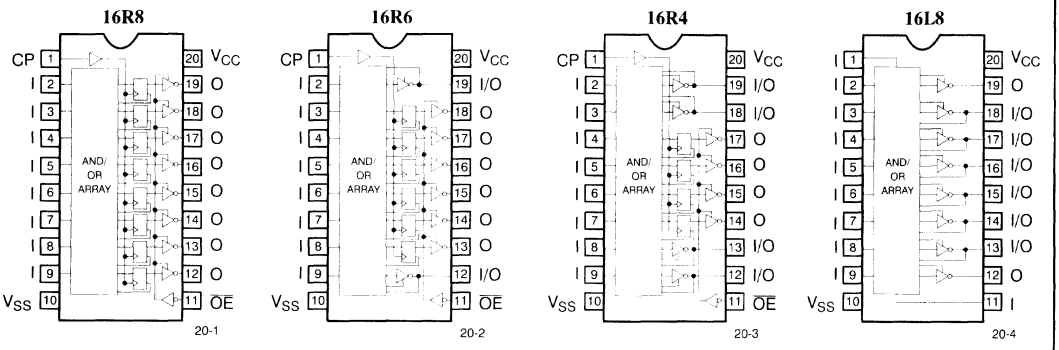
The product selector guide details all the different options available. All the registered devices feature power-up RESET. The register Q output is set to a logic LOW when power is applied to the devices.

A security fuse is provided on all the devices to prevent copying of the device fuse pattern.

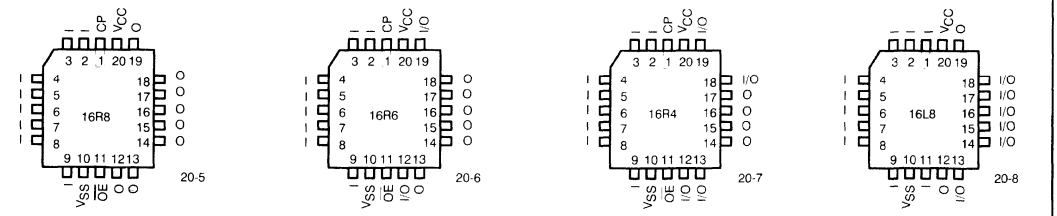
Programming

The PAL20 Series devices can be programmed using the *Impulse* programmer available from Cypress Semiconductor. See third party information in thirdparty tool section for further programmer information.

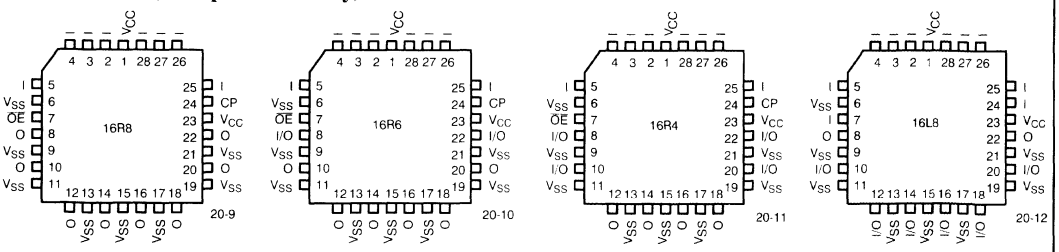
Logic Symbols and DIP Pinouts



20-Pin PLCC/LCC Pinouts



28-Pin PLCC (−4 Speed Bin Only) Pinouts



PAL is a registered trademark of Monolithic Memories Inc.

CYPRESS

Function Selection Guide

Device	Dedicated Inputs	Outputs	Product Terms/Outputs	Feedback	Enable
PAL16L8	10	6 comb. 2 comb.	7 7	I/O —	prog. prog.
PAL16R8	8	8 reg.	8	reg.	pin
PAL16R6	8	6 reg. 2 comb.	8 7	reg. I/O	pin prog.
PAL16R4	8	4 reg. 4 comb.	8 7	reg. I/O	pin prog.

Speed Selection Guide (Commercial −4/−5/−7, Military −7/−10)

Speed Bin	t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	f_{MAX} (MHz)	I_{CC} (mA)
−4	4.5	2.5	4.5	142.9	180
−5	5	2.5	5	133.3	180
−7	7	3.5	6	105.3	180
−10	10	4.5	7	87.0	180

2

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to V_{CC} + 0.5V

DC Input Voltage ..... −1.2V to V_{CC} + 0.5V

DC Input Current (except during programming) ..... −30 mA to +5 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±5%
Military[1]	−55°C to +125°C	5V ±10%

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	Commercial	2.4		V
			I_{OH} = −2 mA	Military			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA	Commercial		0.5	V
			I_{OL} = 12 mA	Military			
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs[2]			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs[2]				0.8	V
I_{IX}	Input Leakage Current	0.4V ≤ V_{IN} ≤ 2.7V, V_{CC} = Max.[3]			−250	50	µA
I_I	Maximum Input Current	V_{IN} = 5.5V, V_{CC} = Max.				1	mA
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{SS} ≤ V_{OUT} ≤ V_{CC}[3]			−100	+100	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[4]			−30	−130	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = GND, Outputs Open				180	mA

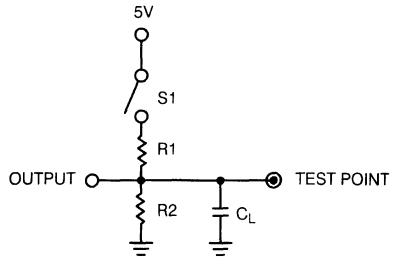
Notes:

1. T_A is the "instant on" case temperature.
2. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
3. I/O pin leakage is the worse case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

Capacitance[5]

Parameter	Description		Test Conditions	Typical	Unit
C_{IN}	Input Capacitance	CP, $\overline{OE}$	T_A = 25°C, f = 1 MHz, V_{IN} = 0, V_{CC} = 5.0V	8	pF
		$I_1 - I_8$		5	pF
C_{OUT}	Output Capacitance			8	pF

AC Test Loads and Waveforms



Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	200Ω	390Ω	390Ω	750Ω	1.5V
t_{PZX}, t_{EA}	Z ⧫ H: Open Z ⧫ L: Closed						1.5V
t_{PXZ}, t_{ER}	H ⧫ Z: Open L ⧫ Z: Closed	5 pF					H ⧫ Z: V_{OH} − 0.5V L ⧫ Z: V_{OL} + 0.5V

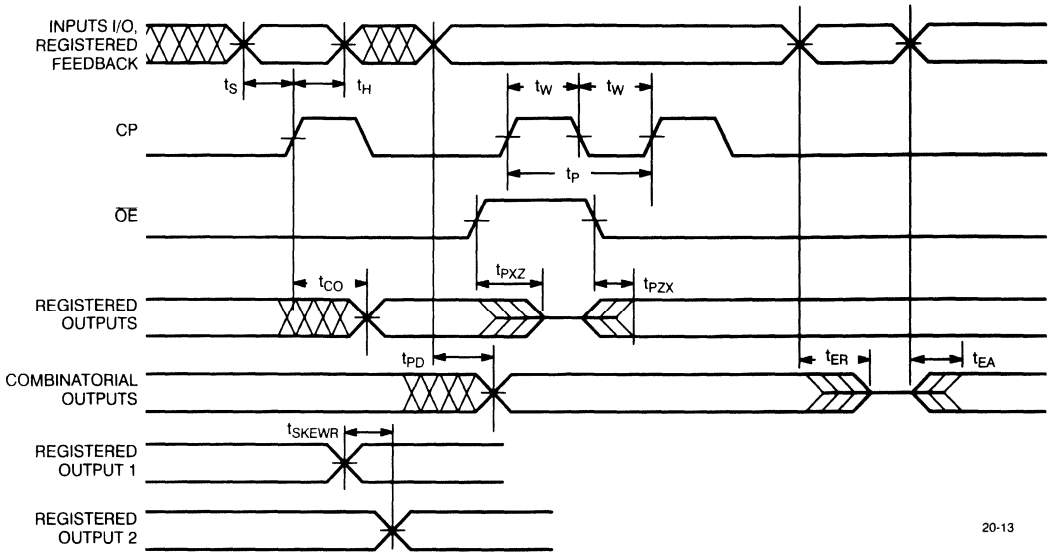
Switching Characteristics Over the Operating Range[6]

Parameter	Description		−4		−5		−7		−10		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Non-Registered Output 16L8, 16R6, 16R4		1	4.5	1	5	2	7	2	10	ns
t_{EA}	Input to Output Enable 16L8, 16R6, 16R4		2	6.5	2	6.5	2	7	2	10	ns
t_{ER}	Input to Output Disable Delay 16L8, 16R6, 16R4		2	5.5	2	5.5	2	7	2	10	ns
t_{PZX}	Pin 11 to Output Enable 16R8, 16R6, 16R4		1	6	1	6	2	7	2	10	ns
t_{PXZ}	Pin 11 to Output Disable 16R8, 16R6, 16R4		1	5	1	5	2	7	2	10	ns
t_{CO}	Clock to Output 16R8, 16R6, 16R4		1	4.5	1	5	2	6	2	7	ns
t_{SKEWR}	Skew Between Registered Outputs 16R8, 16R6, 16R4[5]			0.75		1		1		1	ns
t_S	Input or Feedback Set-Up Time 16R8, 16R6, 16R4		2.5		2.5		3.5		4.5		ns
t_H	Hold Time 16R8, 16R6, 16R4		0		0		0		0		ns
t_P	Clock Period (t_{CO} + t_S)		7		7.5		9.5		11.5		ns
t_W	Clock Width		3		3		3.5		5		ns
f_{MAX}	Maximum Frequency	External Feedback (1/tp)[7]		142.9		133.3		105.3		87	MHz
		Internal Feedback[5, 8]		175		175		150		133	

Notes:

5. Tested initially and after any design or process changes that may affect these parameters.
6. See the last page of this specification for Group A subgroup testing information.
7. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
8. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal-only feedback can operate.

Switching Waveforms[9]



Note:
9. Input rise and fall time is 2-ns typical.

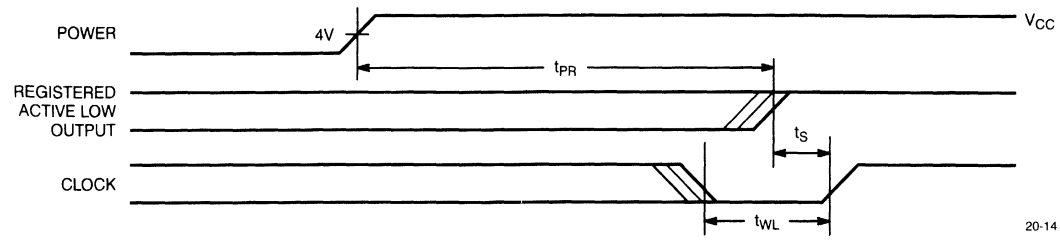
Power-Up Reset

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will be HIGH due to the inverting output buffer. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

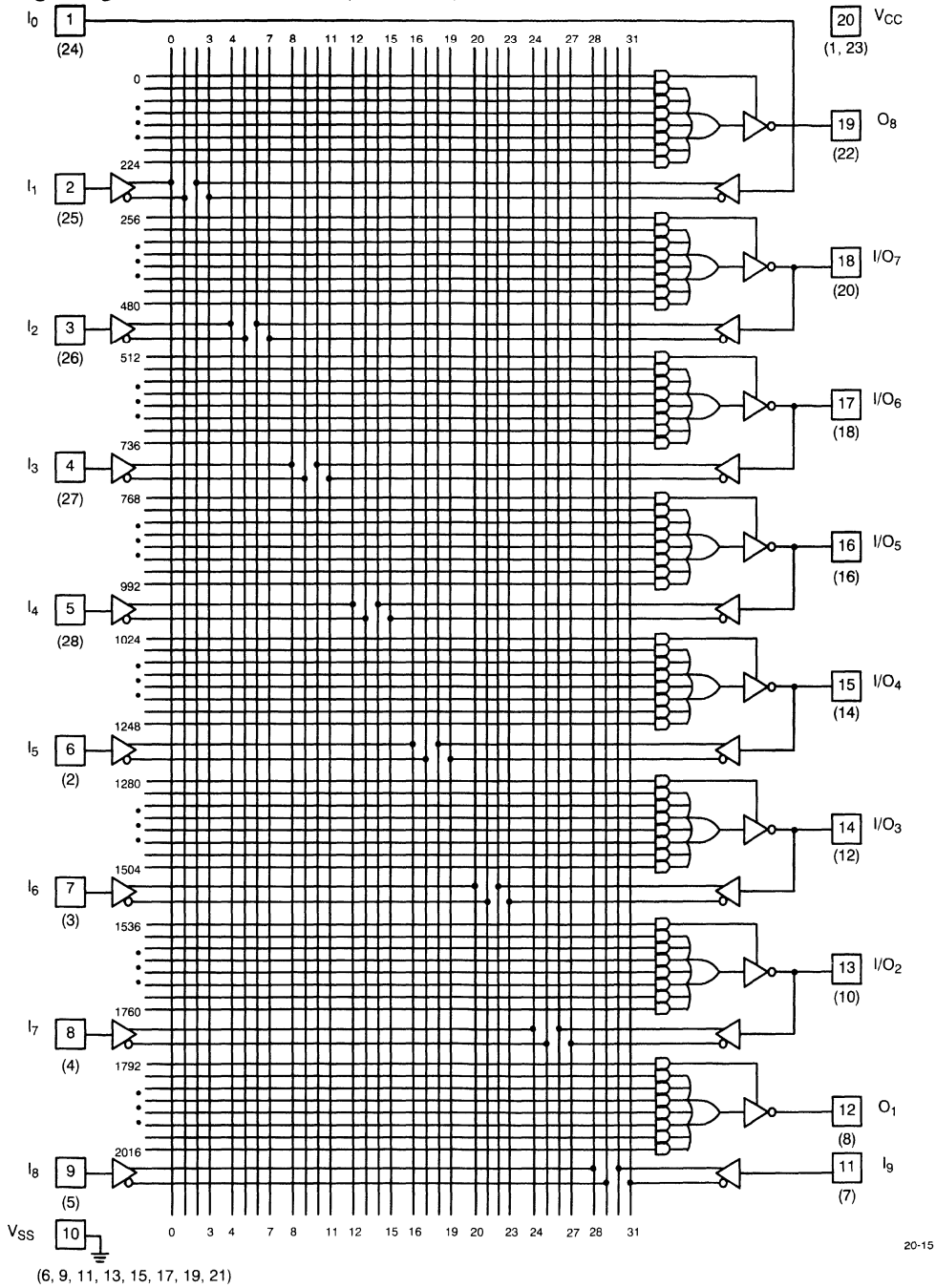
1. The V_{CC} must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback set-up times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-Up Reset Time	1000	ns
t_S	Input or Feedback Set-Up Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		

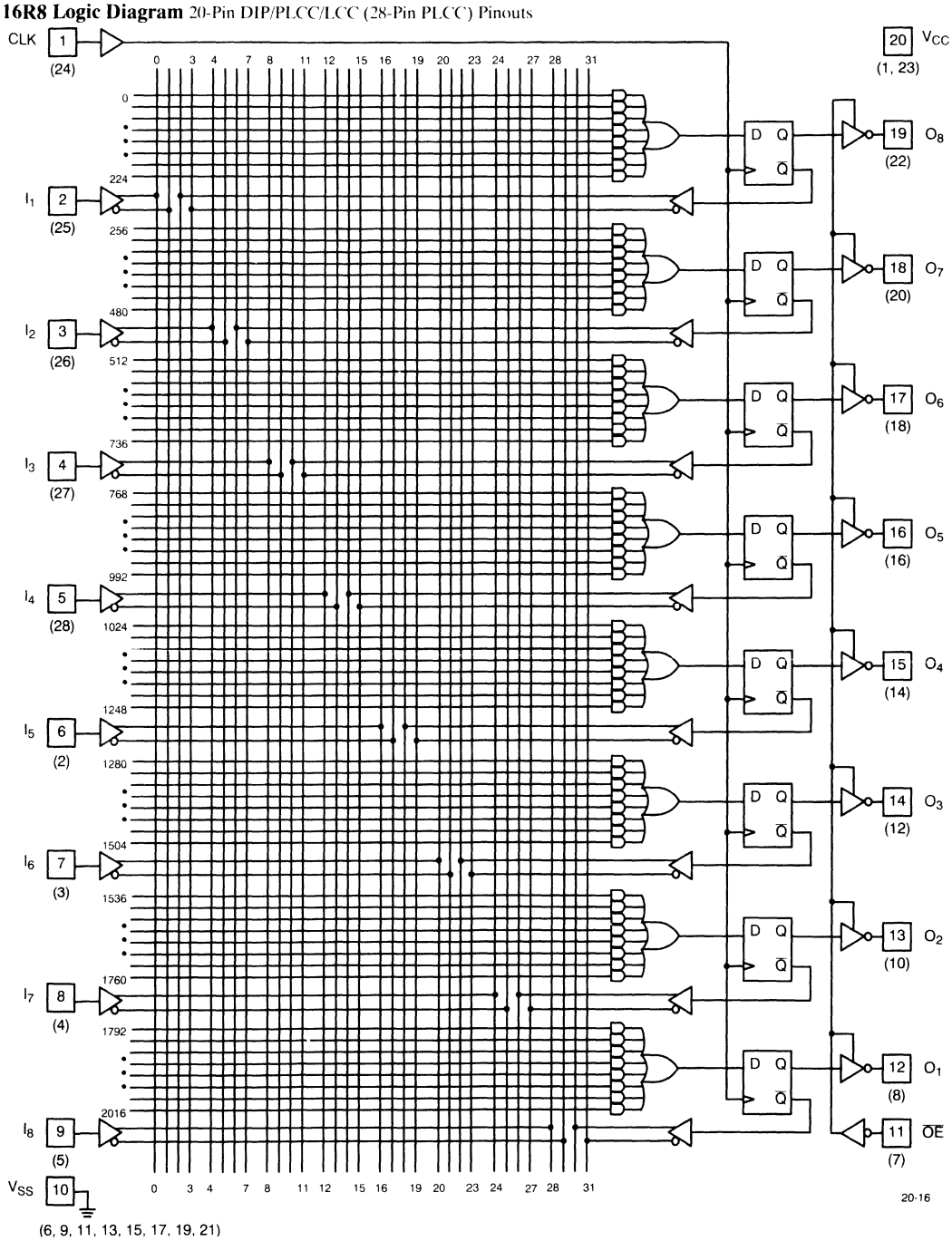
Power-Up Reset Waveform



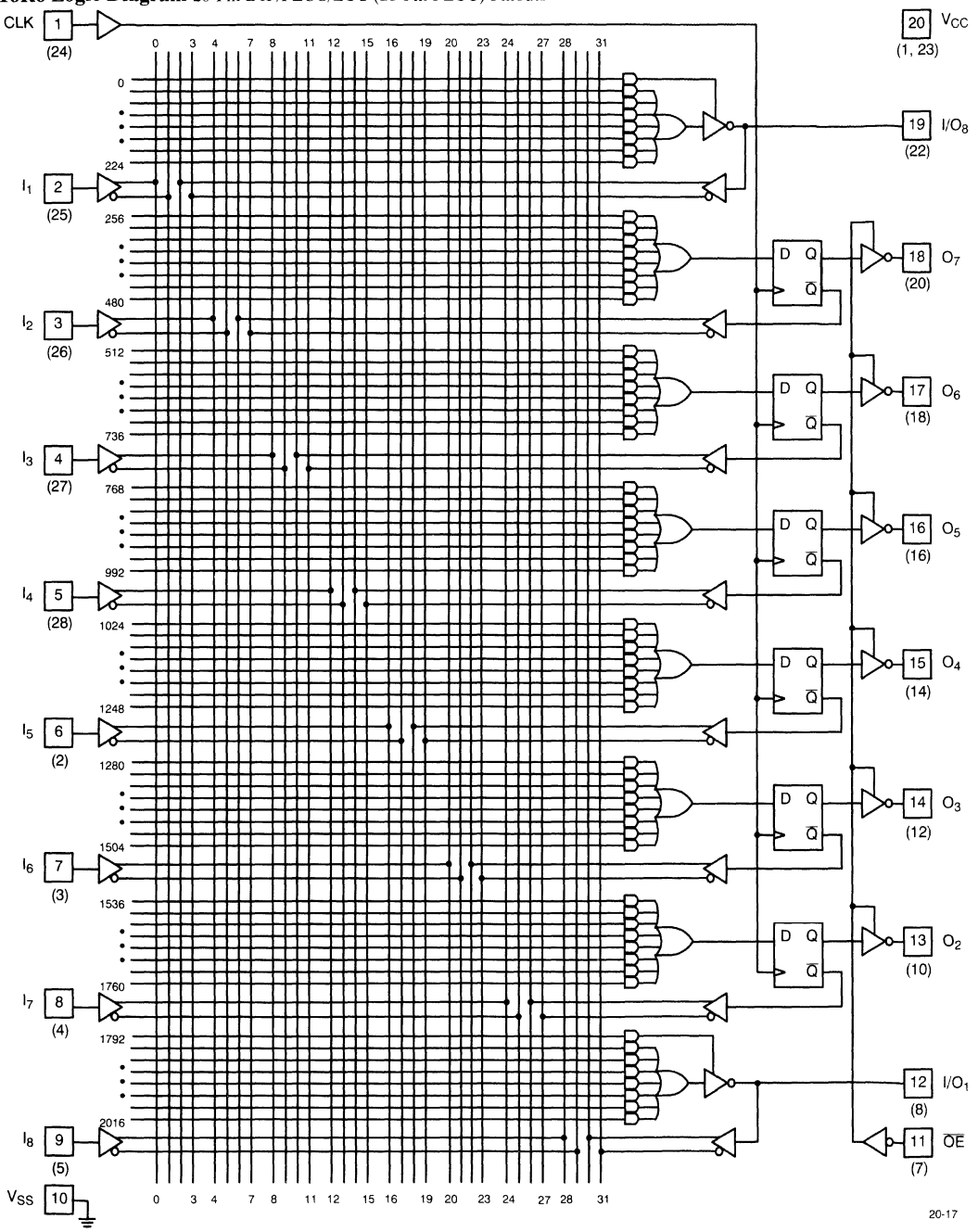
16L8 Logic Diagram 20-Pin DIP/PLCC/LCC (28-Pin PLCC) Pinouts



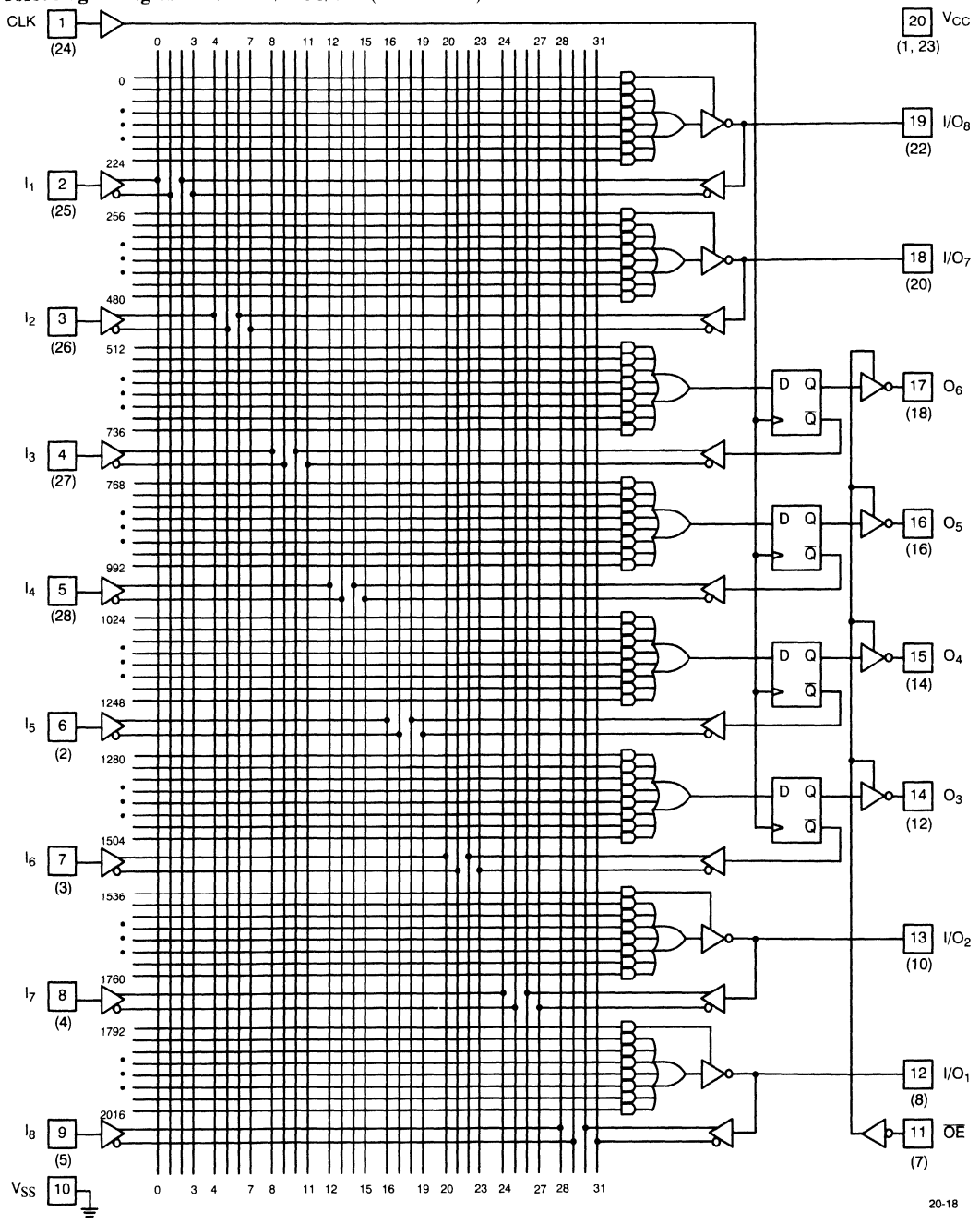
16R8 Logic Diagram 20-Pin DIP/PLCC/LCC (28-Pin PLCC) Pinouts



16R6 Logic Diagram 20-Pin DIP/PLCC/LCC (28-Pin PLCC) Pinouts



16R4 Logic Diagram 20-Pin DIP/PLCC/LCC (28-Pin PLCC) Pinouts



Ordering Information

I_{CC} (mA)	t_{PD} (ns)	Ordering Code	Package Name	Package Type	Operating Range
180	4.5	PAL16L8–4JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	5	PAL16L8–5DC	D6	20-Lead (300-Mil) CerDIP	
		PAL16L8–5JC	J61	20-Lead Plastic Leaded Chip Carrier	
		PAL16L8–5PC	P5	20-Lead (300-Mil) Molded DIP	
	7	PAL16L8–7DC	D6	20-Lead (300-Mil) CerDIP	
		PAL16L8–7JC	J61	20-Lead Plastic Leaded Chip Carrier	
		PAL16L8–7PC	P5	20-Lead (300-Mil) Molded DIP	
		PAL16L8–7DMB	D6	20-Lead (300-Mil) CerDIP	Military
		PAL16L8–7LMB	L61	20-Pin Square Leadless Chip Carrier	
	10	PAL16L8–10DMB	D6	20-Lead (300-Mil) CerDIP	
		PAL16L8–10LMB	L61	20-Pin Square Leadless Chip Carrier	

I_{CC} (mA)	f_{MAX} (MHz)	Ordering Code	Package Name	Package Type	Operating Range
180	142.9	PAL16R8–4JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	133.3	PAL16R8–5DC	D6	20-Lead (300-Mil) CerDIP	
		PAL16R8–5JC	J61	20-Lead Plastic Leaded Chip Carrier	
		PAL16R8–5PC	P5	20-Lead (300-Mil) Molded DIP	
	105.3	PAL16R8–7DC	D6	20-Lead (300-Mil) CerDIP	
		PAL16R8–7JC	J61	20-Lead Plastic Leaded Chip Carrier	
		PAL16R8–7PC	P5	20-Lead (300-Mil) Molded DIP	
		PAL16R8–7DMB	D6	20-Lead (300-Mil) CerDIP	Military
		PAL16R8–7LMB	L61	20-Pin Square Leadless Chip Carrier	
	87	PAL16R8–10DMB	D6	20-Lead (300-Mil) CerDIP	
		PAL16R8–10LMB	L61	20-Pin Square Leadless Chip Carrier	

I_{CC} (mA)	t_{PD} (ns)	f_{MAX} (MHz)	Ordering Code	Package Name	Package Type	Operating Range
180	4.5	142.9	PAL16R6–4JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	5	133.3	PAL16R6–5DC	D6	20-Lead (300-Mil) CerDIP	
			PAL16R6–5JC	J61	20-Lead Plastic Leaded Chip Carrier	
			PAL16R6–5PC	P5	20-Lead (300-Mil) Molded DIP	
	7	105.3	PAL16R6–7DC	D6	20-Lead (300-Mil) CerDIP	
			PAL16R6–7JC	J61	20-Lead Plastic Leaded Chip Carrier	
			PAL16R6–7PC	P5	20-Lead (300-Mil) Molded DIP	
			PAL16R6–7DMB	D6	20-Lead (300-Mil) CerDIP	Military
			PAL16R6–7LMB	L61	20-Pin Square Leadless Chip Carrier	
	10	87	PAL16R6–10DMB	D6	20-Lead (300-Mil) CerDIP	
			PAL16R6–10LMB	L61	20-Pin Square Leadless Chip Carrier	

Ordering Information (continued)

I_{CC} (mA)	t_{PD} (ns)	f_{MAX} (MHz)	Ordering Code	Package Name	Package Type	Operating Range
180	4.5	142.9	PAL16R4-4JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	5	133.3	PAL16R4-5DC	D6	20-Lead (300-Mil) CerDIP	
			PAL16R4-5JC	J61	20-Lead Plastic Leaded Chip Carrier	
			PAL16R4-5PC	P5	20-Lead (300-Mil) Molded DIP	
	7	105.5	PAL16R4-7DC	D6	20-Lead (300-Mil) CerDIP	
			PAL16R4-7JC	J61	20-Lead Plastic Leaded Chip Carrier	
			PAL16R4-7PC	P5	20-Lead (300-Mil) Molded DIP	
			PAL16R4-7DMB	D6	20-Lead (300-Mil) CerDIP	Military
			PAL16R4-7LMB	L61	20-Pin Square Leadless Chip Carrier	
	10	87	PAL16R4-10DMB	D6	20-Lead (300-Mil) CerDIP	
			PAL16R4-10LMB	L61	20-Pin Square Leadless Chip Carrier	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
V_{PP}	1, 2, 3
I_{CC}	1, 2, 3
I_{OZ}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{PD}	9, 10, 11
t_{PZX}	9, 10, 11
t_{CO}	9, 10, 11
t_S	9, 10, 11
t_H	9, 10, 11

Document #: 38-A-00025-C

PAL®C20 Series

Reprogrammable CMOS PALC 16L8, 16R8, 16R6, 16R4

Features

- **CMOS EPROM technology for reprogrammability**
- **High performance at quarter power**
  - **t_{PD} = 25 ns**
  - **t_S = 20 ns**
  - **t_{CO} = 15 ns**
  - **I_{CC} = 45 mA**
- **High performance at military temperature**
  - **t_{PD} = 20 ns**
  - **t_S = 20 ns**
  - **t_{CO} = 15 ns**
  - **I_{CC} = 70 mA**
- **Commercial and military temperature range**
- **High reliability**
  - **Proven EPROM technology**
  - **>1500V input protection from electrostatic discharge**
  - **100% AC and DC tested**
  - **10% power supply tolerances**
  - **High noise immunity**
  - **Security feature prevents pattern duplication**
  - **100% programming and functional testing**

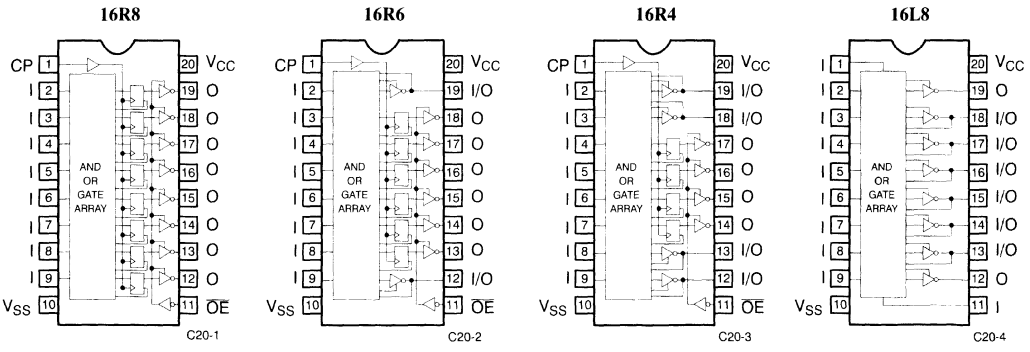
Functional Description

Cypress PALC20 Series devices are high-speed electrically programmable and UV-erasable logic devices produced in a proprietary N-well CMOS EPROM process. These devices utilize a sum-of-products (AND-OR) structure providing users with the ability to program custom logic functions serving unique requirements.

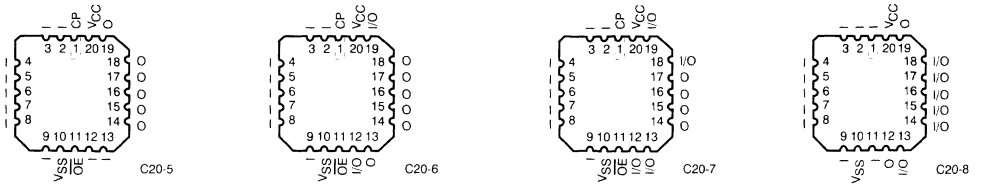
PALs are offered in 20-pin plastic and ceramic DIP, plastic SOJ, and ceramic LCC packages. The ceramic package can be equipped with an erasure window; when exposed to UV light, the PAL is erased and can then be reprogrammed.

Before programming, AND gates or product terms are connected via EPROM cells to both true and complement inputs. Programming an EPROM cell disconnects an input term from a product term. Selective programming of these cells allows a specific logic function to be implemented in a PALC device. PALC devices are supplied in four functional configurations designated 16R8, 16R6, 16R4, and 16L8. These 8 devices have potentially 16 inputs and 8 outputs configurable by the user. Output configurations of 8 registers, 8 combinatorial, 6 registers and 2 combinatorial as well as 4 registers and 4 combinatorial are provided by the 4 functional variations of the product family.

Logic Symbols and DIP and SOJ Pinouts



LCC Pinouts



PAL is a registered trademark of Advanced Micro Devices.

Functional Description (continued)

All combinatorial outputs on the 16R6 and 16R4 as well as 6 of the combinatorial outputs on the 16L8 may be used as optional inputs. All registered outputs have the $\overline{Q}$ bar side of the register fed back into the main array. The registers are automatically initialized upon power-up to Q output LOW and $\overline{Q}$ output HIGH. All unused inputs should be tied to ground.

All PALC devices feature a security function that provides the user with protection for the implementation of proprietary logic. When invoked, the contents of the normal array may no longer be accessed in the verify mode. Because EPROM technology is used as a storage mechanism, the content of the array is not visible under a microscope.

Cypress PALC products are produced in an advanced 1.2-micron N-well CMOS EPROM technology. The use of this proven EPROM technology is the basis for a superior product with inherent advantages in reliability, testability, programming, and functional yield. EPROM technology has the inherent advantage that all programmable elements may be programmed, tested, and erased during the manufacturing process. This also allows the device to be 100% functionally tested during manufacturing. An ability to preload the registers of registered devices during the testing operation makes the testing easier and more efficient. Combining these inherent and designed-in features provides an extremely high degree of functionality, programmability and assured AC performance, and testing becomes an easy task.

The register preload allows the user to initialize the registered devices to a known state prior to testing the device, significantly simplifying and shortening the testing procedure.

2

Commercial and Industrial Selection Guide

Generic Part Number	Logic	Output Enable	Outputs	I_{CC} (mA)		t_{PD} (ns)		t_S (ns)		t_{CO} (ns)	
				L	Com'l/Ind	-25	-35	-25	-35	-25	-35
16L8	(8) 7-wide AND-OR-Invert	Programmable	(6) Bidirectional (2) Dedicated	45	70	25	35	—	—	—	—
16R8	(8) 8-wide AND-OR	Dedicated	Registered Inverting	45	70	—	—	20	30	15	25
16R6	(6) 8-wide AND-OR	Dedicated	Registered Inverting	45	70	25	35	20	30	15	25
	(2) 7-wide AND-OR-Invert	Programmable	Bidirectional								
16R4	(4) 8-wide AND-OR	Dedicated	Registered Inverting	45	70	25	35	20	30	15	25
	(4) 7-wide AND-OR-Invert	Programmable	Bidirectional								

Military Selection Guide

Generic Part Number	Logic	Output Enable	Outputs	I_{CC} (mA)	t_{PD} (ns)			t_S (ns)			t_{CO} (ns)		
					-20	-30	-40	-20	-30	-40	-20	-30	-40
16L8	(8) 7-wide AND-OR-Invert	Programmable	(6) Bidirectional (2) Dedicated	70	20	30	40	—	—	—	—	—	—
16R8	(8) 8-wide AND-OR	Dedicated	Registered Inverting	70	—	—	—	20	25	35	15	20	25
16R6	(6) 8-wide AND-OR	Dedicated	Registered Inverting	70	20	30	40	20	25	35	15	20	25
	(2) 7-wide AND-OR-Invert	Programmable	Bidirectional										
16R4	(4) 8-wide AND-OR	Dedicated	Registered Inverting	70	20	30	40	20	25	35	15	20	25
	(4) 7-wide AND-OR-Invert	Programmable	Bidirectional										

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with Power Applied ..... −55°C to +125°C
Supply Voltage to Ground Potential (Pin 20 to Pin 10) ..... −0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V
DC Input Voltage ..... −3.0V to +7.0V
Output Current into Outputs (LOW) ..... 24 mA
DC Programming Voltage 14.0V
UV Exposure ..... 7258 Wsec/cm^2
Static Discharge Voltage ..... >1500V (per MIL-STD-883, Method 3015)
Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ±10%
Military[1]	−55°C to +125°C	5V ±10%
Industrial	−40°C to +85°C	

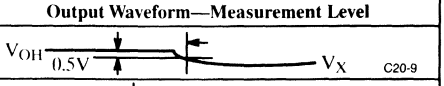
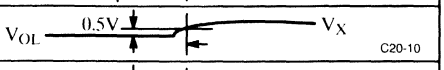
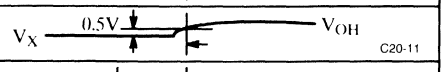
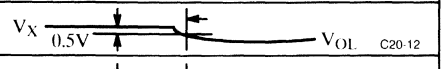
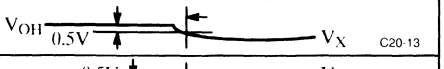
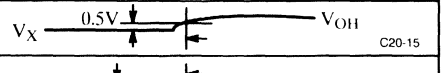
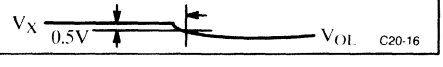
Electrical Characteristics Over the Operating Range (unless otherwise noted)[2]

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	Com'l/Ind	2.4		V
			I_{OH} = −2 mA	Military			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA	Com'l/Ind		0.4	V
			I_{OL} = 12 mA	Military			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH[3] Voltage for All Inputs			2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW[3] Voltage for All Inputs				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$			−10	10	µA
V_{PP}	Programming Voltage	I_{PP} = 50 mA Max.			13.0	14.0	V
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[4]				−300	mA
I_{CC}	Power Supply Current	All Inputs = GND, V_{CC} = Max., I_{OUT} = 0 mA[5]		"L"		45	mA
				Com'l/Ind		70	mA
				Military		70	mA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			−100	100	µA

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
5. $I_{CC(AC)}$ = (0.6 mA/MHz) × (Operating Frequency in MHz) + $I_{CC(DC)}$. $I_{CC(DC)}$ is measured with an unprogrammed device.

Electrical Characteristics Over the Operating Range (Unless Otherwise Noted)[2] (continued)

Parameter	V_X	Output Waveform—Measurement Level
t_{PXZ} (−)	1.5V	 C20-9
t_{PXZ} (+)	2.6V	 C20-10
t_{PZX} (+)	V_{thc}	 C20-11
t_{PZX} (−)	V_{thc}	 C20-12
t_{ER} (−)	1.5V	 C20-13
t_{ER} (+)	2.6V	 C20-14
t_{EA} (+)	V_{thc}	 C20-15
t_{EA} (−)	V_{thc}	 C20-16

Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	10	pF
C_{OUT}	Output Capacitance	V_{IN} = 0, V_{CC} = 5.0V	10	pF

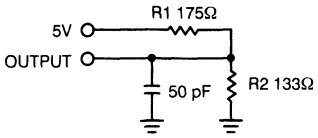
Switching Characteristics Over Operating Range[2, 7, 8]

		Commercial/Industrial				Military						
		−25		−35		−20		−30		−40		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PD}	Input or Feedback to Non-Registered Output 16L8, 16R6, 16R4		25		35		20		30		40	ns
t_{EA}	Input to Output Enable 16L8, 16R6, 16R4		25		35		20		30		40	ns
t_{ER}	Input to Output Disable Delay 16L8, 16R6, 16R4		25		35		20		30		40	ns
t_{PZX}	Pin 11 to Output Enable 16R8, 16R6, 16R4		20		25		20		25		25	ns
t_{PXZ}	Pin 11 to Output Disable 16R8, 16R6, 16R4		20		25		20		25		25	ns
t_{CO}	Clock to Output 16R8, 16R6, 16R4		15		25		15		20		25	ns
t_S	Input or Feedback Set-Up Time 16R8, 16R6, 16R4	20		30		20		25		35		ns
t_H	Hold Time 16R8, 16R6, 16R4	0		0		0		0		0		ns
t_P	Clock Period	35		55		35		45		60		ns
t_W	Clock Width	15		20		12		20		25		ns
f_{MAX}	Maximum Frequency		28.5		18		28.5		22		16.5	MHz

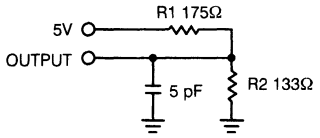
Notes:

6. Tested initially and after any design or process changes that may affect these parameters.
7. Part (a) (part (c) for military) of AC Test Loads and Waveforms is used for all parameters except t_{EA}, t_{ER}, t_{PZX} and t_{PXZ}. Part (b) (part (d) for military) of AC Test Loads and Waveforms is used for t_{EA}, t_{ER}, t_{PZX} and t_{PXZ}.
8. The parameters t_{ER} and t_{PXZ} are measured as the delay from the input disable logic threshold transition to V_{OH} − 0.5V for an enabled HIGH output or V_{OL} + 0.5V for an enabled LOW output. Please see Electrical Characteristics for waveforms and measurement reference levels.

AC Test Loads and Waveforms

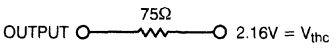


(a) Commercial

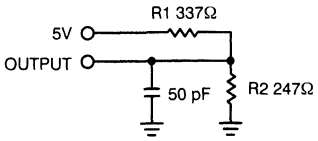


(b) Commercial C20-17

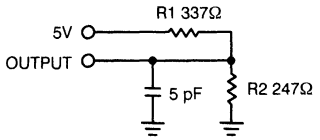
Equivalent to:
THÉVENIN EQUIVALENT COMMERCIAL



C20-18

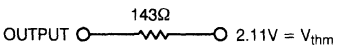


(c) Military

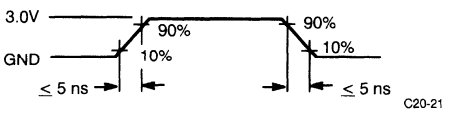


(d) Military C20-20

Equivalent to:
THÉVENIN EQUIVALENT MILITARY



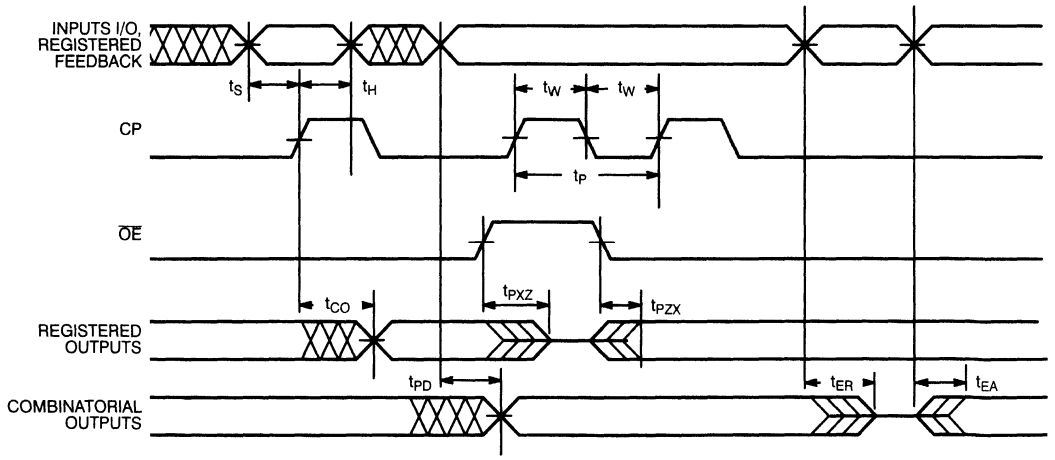
C20-19



C20-21

(e)

Switching Waveforms



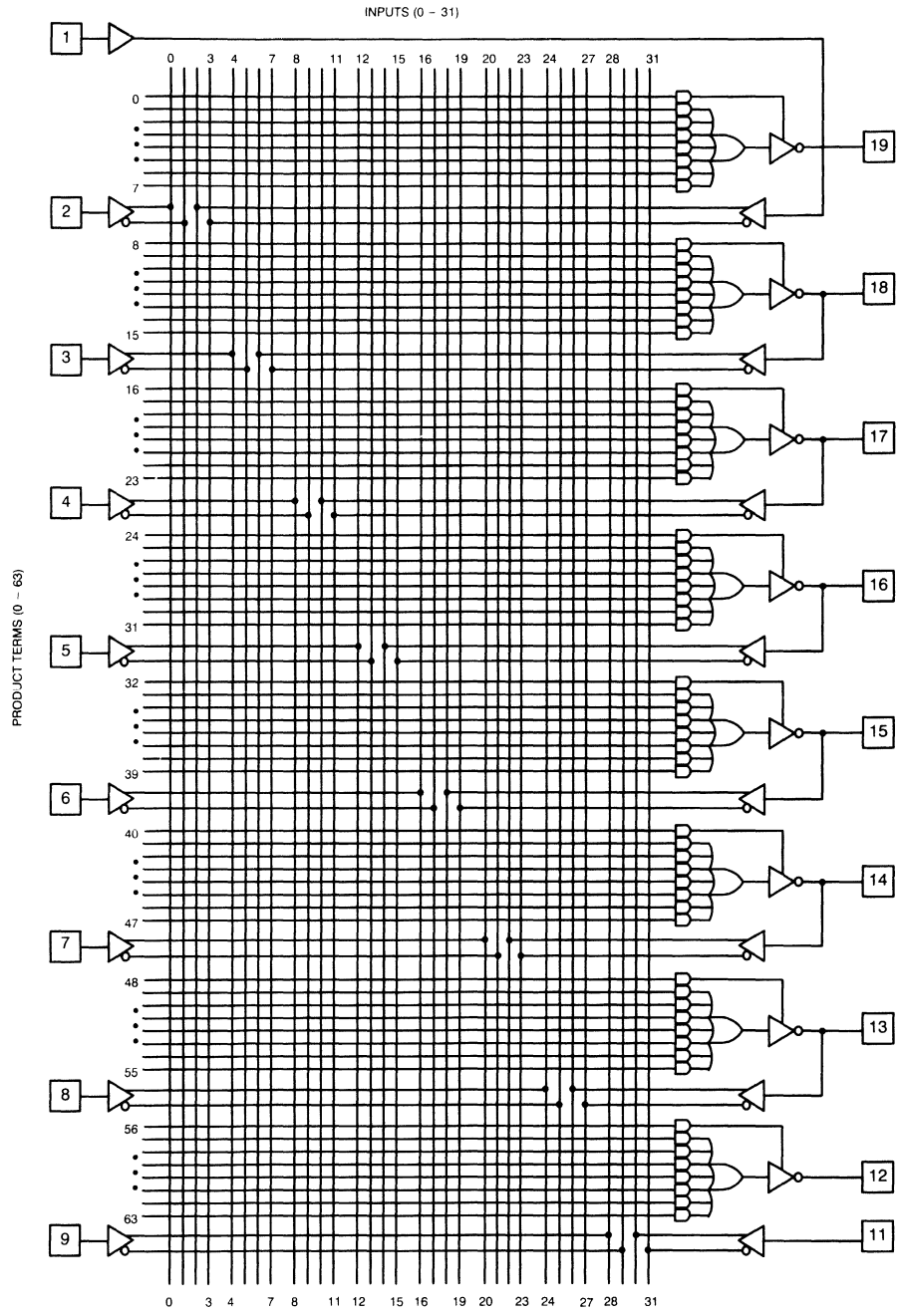
C20-22

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the PALC device. In addition, high ambient light levels can create hole-electron pairs that may cause "blank" check failures or "verify errors" when programming windowed parts. This phenomenon can be avoided by using an opaque label over the window during programming in high ambient light environments.

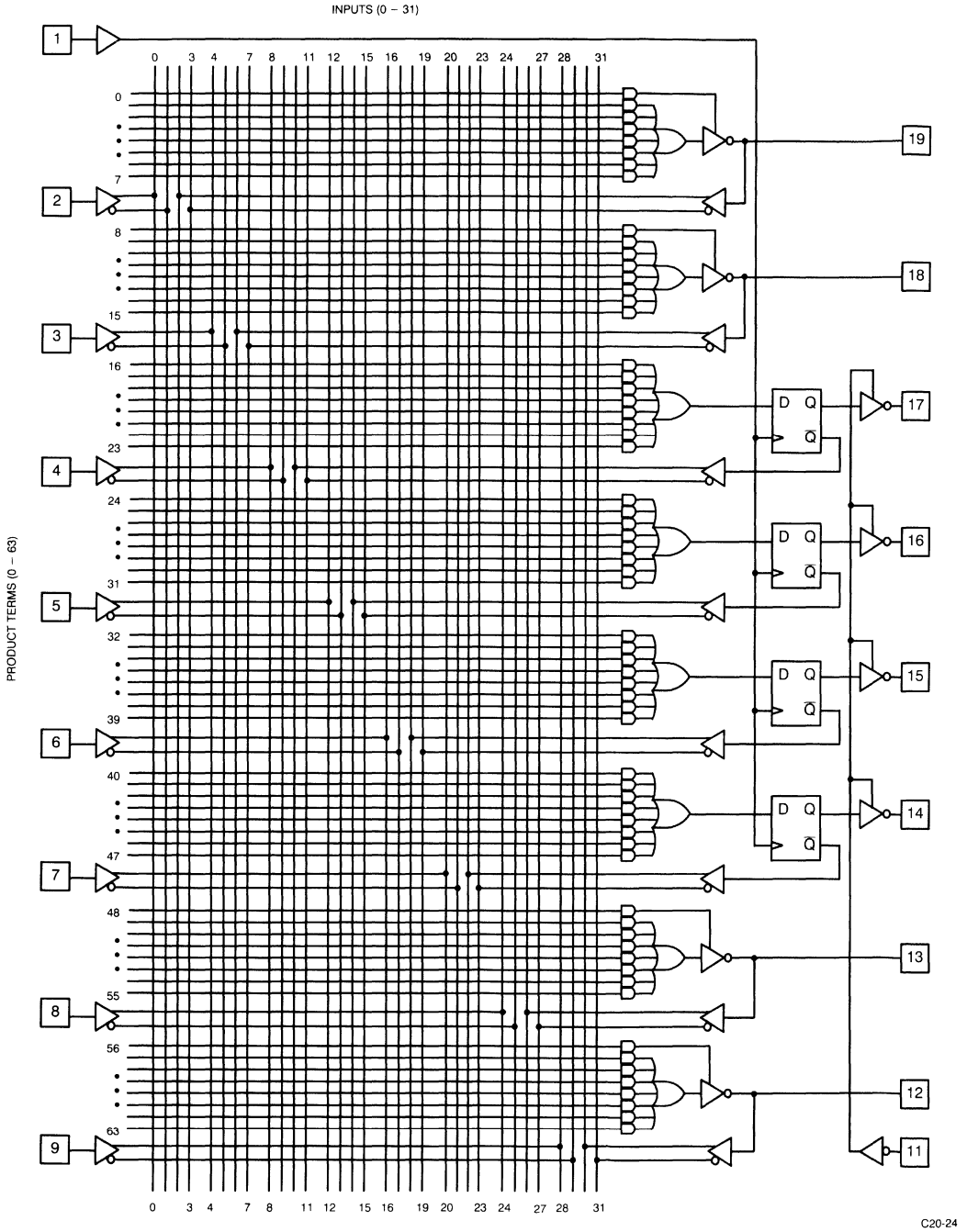
The recommended dose for erasure is ultraviolet light with a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure would be approximately 35 minutes. The PALC device needs to be placed within 1 inch of the lamp during erasure. Permanent damage may result if the device is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Logic Diagram PALC16L8

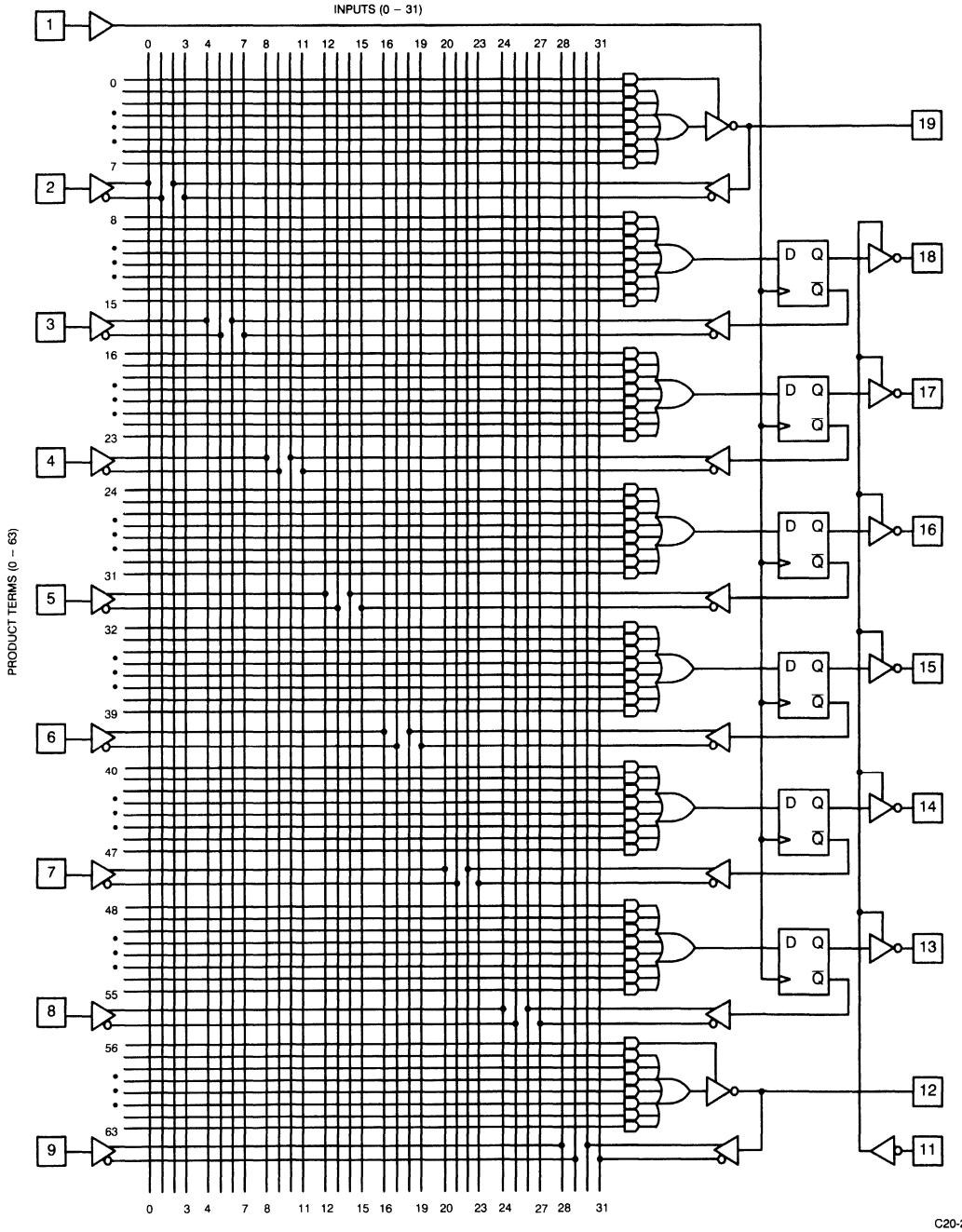


C20-23

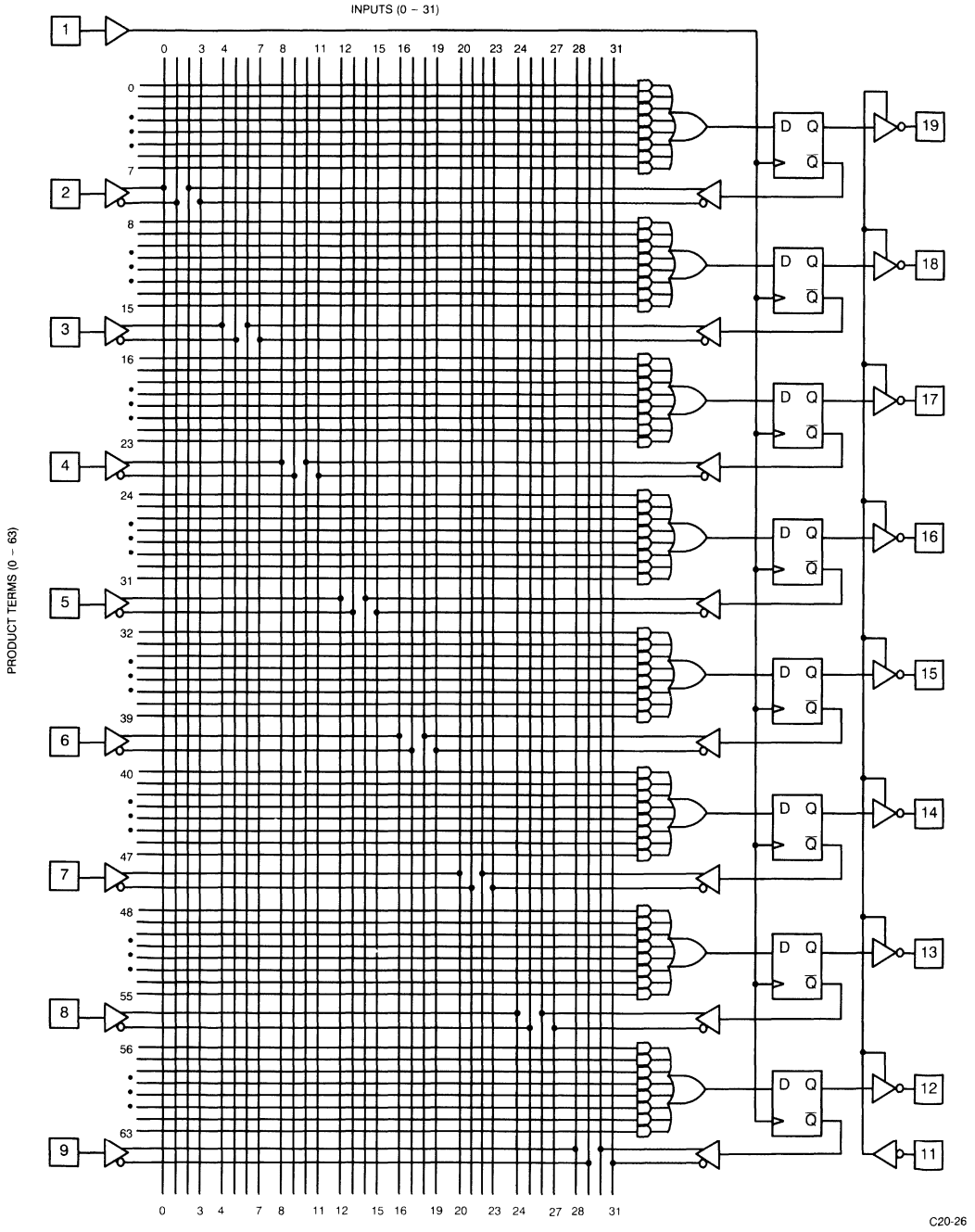
Logic Diagram PALC16R4



Logic Diagram PALC16R6

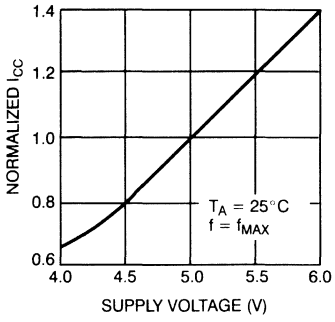


Logic Diagram PALC16R8

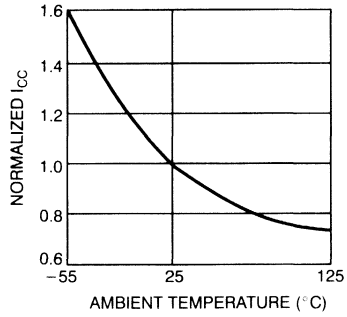


Typical DC and AC Characteristics

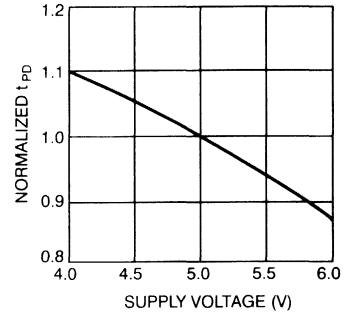
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



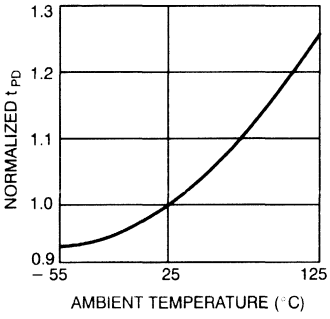
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



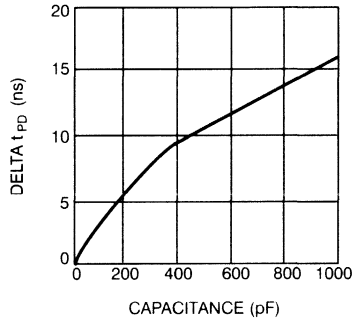
NORMALIZED PROPAGATION DELAY vs. SUPPLY VOLTAGE



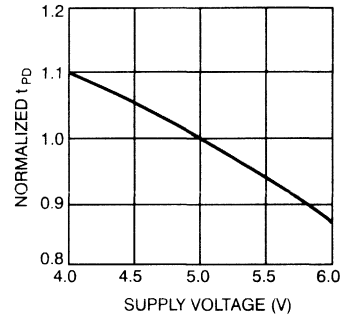
NORMALIZED PROPAGATION DELAY vs. TEMPERATURE



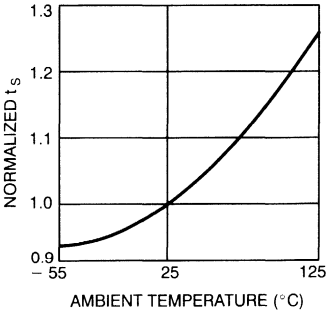
DELTA PROPAGATION TIME vs. OUTPUT LOADING



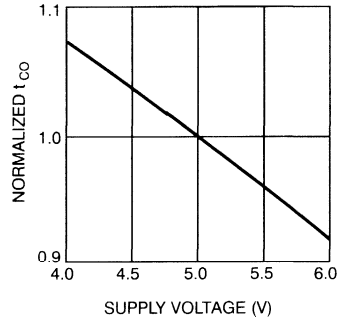
NORMALIZED SET-UP TIME vs. SUPPLY VOLTAGE



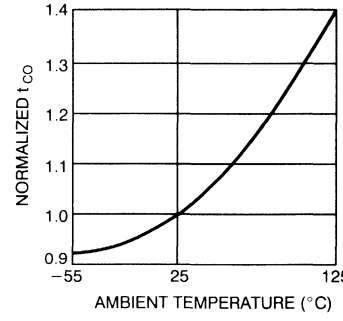
NORMALIZED SET-UP TIME vs. TEMPERATURE



NORMALIZED CLOCK-TO-OUTPUT TIME vs. SUPPLY VOLTAGE

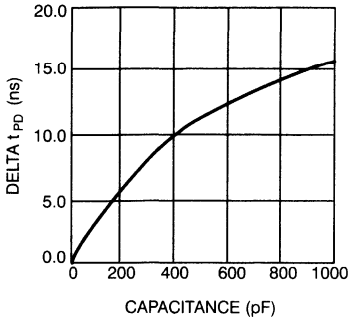


NORMALIZED CLOCK-TO-OUTPUT TIME vs. TEMPERATURE

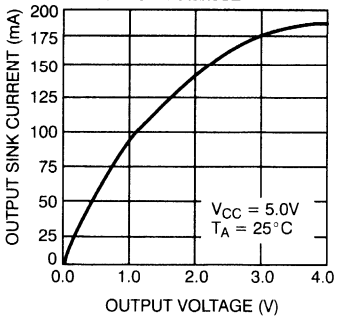


Typical DC and AC Characteristics (continued)

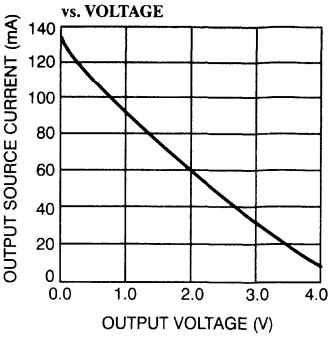
DELTA CLOCK-TO-OUTPUT TIME vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. VOLTAGE



Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
20	—	—	70	PALC16L8-20DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALC16L8-20LMB	L61	20-Pin Square Leadless Chip Carrier	
				PALC16L8-20QMB	Q61	20-Pin Windowed Square Leadless Chip Carrier	
				PALC16L8-20WMB	W6	20-Lead (300-Mil) Windowed CerDIP	
25	—	—	45	PALC16L8L-25PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
				PALC16L8L-25VC	V5	20-Lead (300-Mil) Molded SOJ	
				PALC16L8L-25WC	W6	20-Lead (300-Mil) Windowed CerDIP	
			70	PALC16L8-25PC/PI	P5	20-Lead (300-Mil) Molded DIP	
				PALC16L8-25VC	V5	20-Lead (300-Mil) Molded SOJ	
				PALC16L8-25WC	W6	20-Lead (300-Mil) Windowed CerDIP	
30	—	—	70	PALC16L8-30DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALC16L8-30LMB	L61	20-Pin Square Leadless Chip Carrier	
				PALC16L8-30QMB	Q61	20-Pin Windowed Square Leadless Chip Carrier	
				PALC16L8-30WMB	W6	20-Lead (300-Mil) Windowed CerDIP	
35	—	—	45	PALC16L8L-35PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
				PALC16L8L-35VC	V5	20-Lead (300-Mil) Molded SOJ	
				PALC16L8L-35WC	W6	20-Lead (300-Mil) Windowed CerDIP	
			70	PALC16L8-35PC/PI	P5	20-Lead (300-Mil) Molded DIP	
				PALC16L8-35VC	V5	20-Lead (300-Mil) Molded SOJ	
				PALC16L8-35WC	W6	20-Lead (300-Mil) Windowed CerDIP	
40	—	—	70	PALC16L8-40DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALC16L8-40LMB	L61	20-Pin Square Leadless Chip Carrier	
				PALC16L8-40QMB	Q61	20-Pin Windowed Square Leadless Chip Carrier	
				PALC16L8-40WMB	W6	20-Lead (300-Mil) Windowed CerDIP	

Ordering Information (continued)

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
20	20	15	70	PALC16R4-20DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALC16R4-20LMB	L61	20-Pin Square Leadless Chip Carrier	
				PALC16R4-20QMB	Q61	20-Pin Windowed Square Leadless Chip Carrier	
				PALC16R4-20WMB	W6	20-Lead (300-Mil) Windowed CerDIP	
25	20	15	45	PALC16R4L-25PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
				PALC16R4L-25VC	V5	20-Lead (300-Mil) Molded SOJ	
				PALC16R4L-25WC	W6	20-Lead (300-Mil) Windowed CerDIP	
			70	PALC16R4-25PC/PI	P5	20-Lead (300-Mil) Molded DIP	
				PALC16R4-25VC	V5	20-Lead (300-Mil) Molded SOJ	
				PALC16R4-25WC	W6	20-Lead (300-Mil) Windowed CerDIP	
30	25	20	70	PALC16R4-30DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALC16R4-30LMB	L61	20-Pin Square Leadless Chip Carrier	
				PALC16R4-30QMB	Q61	20-Pin Windowed Square Leadless Chip Carrier	
				PALC16R4-30WMB	W6	20-Lead (300-Mil) Windowed CerDIP	
35	30	25	45	PALC16R4L-35PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
				PALC16R4L-35VC	V5	20-Lead (300-Mil) Molded SOJ	
				PALC16R4L-35WC	W6	20-Lead (300-Mil) Windowed CerDIP	
			70	PALC16R4-35PC/PI	P5	20-Lead (300-Mil) Molded DIP	
				PALC16R4-35VC	V5	20-Lead (300-Mil) Molded SOJ	
				PALC16R4-35WC	W6	20-Lead (300-Mil) Windowed CerDIP	
40	35	25	70	PALC16R4-40DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALC16R4-40LMB	L61	20-Pin Square Leadless Chip Carrier	
				PALC16R4-40QMB	Q61	20-Pin Windowed Square Leadless Chip Carrier	
				PALC16R4-40WMB	W6	20-Lead (300-Mil) Windowed CerDIP	

2

Ordering Information (continued)

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
20	20	15	70	PALC16R6-20DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALC16R6-20LMB	L61	20-Pin Square Leadless Chip Carrier	
				PALC16R6-20QMB	Q61	20-Pin Windowed Square Leadless Chip Carrier	
				PALC16R6-20WMB	W6	20-Lead (300-Mil) Windowed CerDIP	
25	20	15	45	PALC16R6L-25PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
				PALC16R6L-25VC	V5	20-Lead (300-Mil) Molded SOJ	
				PALC16R6L-25WC	W6	20-Lead (300-Mil) Windowed CerDIP	
			70	PALC16R6-25PC/PI	P5	20-Lead (300-Mil) Molded DIP	
				PALC16R6-25VC	V5	20-Lead (300-Mil) Molded SOJ	
				PALC16R6-25WC	W6	20-Lead (300-Mil) Windowed CerDIP	
30	25	20	70	PALC16R6-30DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALC16R6-30LMB	L61	20-Pin Square Leadless Chip Carrier	
				PALC16R6-30QMB	Q61	20-Pin Windowed Square Leadless Chip Carrier	
				PALC16R6-30WMB	W6	20-Lead (300-Mil) Windowed CerDIP	
35	30	25	45	PALC16R6L-35PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
				PALC16R6L-35VC	V5	20-Lead (300-Mil) Molded SOJ	
				PALC16R6L-35WC	W6	20-Lead (300-Mil) Windowed CerDIP	
			70	PALC16R6-35PC/PI	P5	20-Lead (300-Mil) Molded DIP	
				PALC16R6-35VC	V5	20-Lead (300-Mil) Molded SOJ	
				PALC16R6-35WC	W6	20-Lead (300-Mil) Windowed CerDIP	
40	35	25	70	PALC16R6-40DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALC16R6-40LMB	L61	20-Pin Square Leadless Chip Carrier	
				PALC16R6-40QMB	Q61	20-Pin Windowed Square Leadless Chip Carrier	
				PALC16R6-40WMB	W6	20-Lead (300-Mil) Windowed CerDIP	

Ordering Information (continued)

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
—	20	15	70	PALC16R8-20DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALC16R8-20LMB	L61	20-Pin Square Leadless Chip Carrier	
				PALC16R8-20QMB	Q61	20-Pin Windowed Square Leadless Chip Carrier	
				PALC16R8-20WMB	W6	20-Lead (300-Mil) Windowed CerDIP	
—	20	15	45	PALC16R8L-25PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
				PALC16R8L-25WC	W6	20-Lead (300-Mil) Windowed CerDIP	
			70	PALC16R8-25PC/PI	P5	20-Lead (300-Mil) Molded DIP	
				PALC16R8-25WC	W6	20-Lead (300-Mil) Windowed CerDIP	
—	25	20	70	PALC16R8-30DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALC16R8-30LMB	L61	20-Pin Square Leadless Chip Carrier	
				PALC16R8-30QMB	Q61	20-Pin Windowed Square Leadless Chip Carrier	
				PALC16R8-30WMB	W6	20-Lead (300-Mil) Windowed CerDIP	
—	30	25	45	PALC16R8L-35PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
				PALC16R8L-35WC	W6	20-Lead (300-Mil) Windowed CerDIP	
			70	PALC16R8-35PC/PI	P5	20-Lead (300-Mil) Molded DIP	
				PALC16R8-35WC/WC	W6	20-Lead (300-Mil) Windowed CerDIP	
—	35	25	70	PALC16R8-40DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALC16R8-40LMB	L61	20-Pin Square Leadless Chip Carrier	
				PALC16R8-40QMB	Q61	20-Pin Windowed Square Leadless Chip Carrier	
				PALC16R8-40WMB	W6	20-Lead (300-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
V_{PP}	1, 2, 3
I_{CC}	1, 2, 3
I_{OZ}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	9, 10, 11
t_{PZX}	9, 10, 11
t_{CO}	9, 10, 11
t_S	9, 10, 11
t_H	9, 10, 11

Document #: 38-00001-F

PRELIMINARY **PALCE16V8**

Flash Erasable, Reprogrammable CMOS PAL® Device

Features

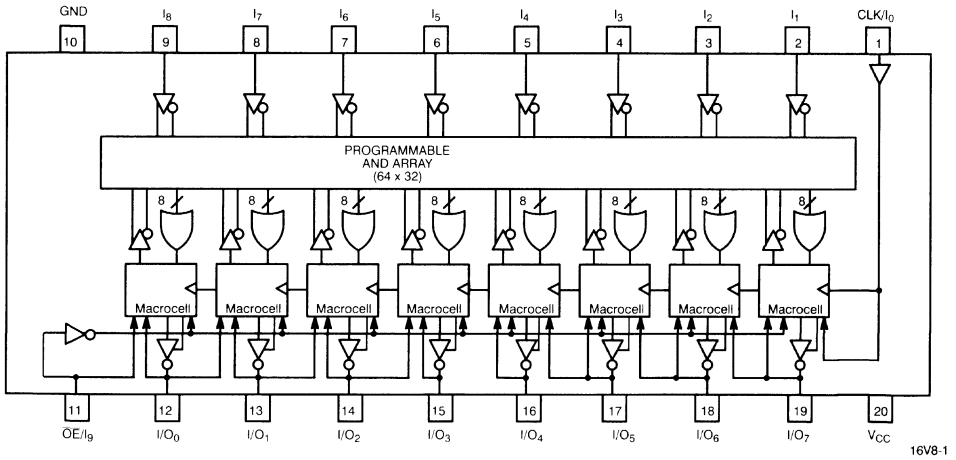
- Advanced second-generation PAL architecture
- Low power
  - 90 mA max. commercial (10, 15, 25 ns)
  - 115 mA max. commercial (7 ns)
  - 130 mA max. military/industrial (10, 15, 25 ns)
- Quarter power version
  - 55 mA max. commercial (15, 25 ns)
- CMOS Flash technology for electrical erasability and reprogrammability
- User-programmable macrocell
  - Output polarity control
  - Individually selectable for registered or combinatorial operation
- Up to 16 input terms and 8 outputs
- DIP, LCC, and PLCC available
  - 7.5, 10, 15, and 25 ns com'l version
    5 ns t_{CO}
    5 ns t_S
    7.5 ns t_{PD}
    125-MHz state machine
  - 10, 15, and 25 ns military/industrial versions
    7 ns t_{CO}
    10 ns t_S
    10 ns t_{PD}
    62-MHz state machine
- High reliability
  - Proven Flash technology
  - 100% programming and functional testing

Functional Description

The Cypress PALCE16V8 is a CMOS Flash Electrical Erasable second-generation programmable array logic device. It is implemented with the familiar sum-of-product (AND-OR) logic structure and the programmable macrocell.

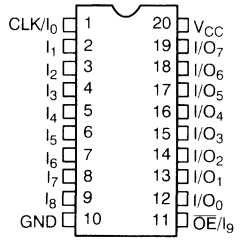
The PALCE16V8 is executed in a 20-pin 300-mil molded DIP, a 300-mil cerdip, a 20-lead square ceramic leadless chip carrier, and a 20-lead square plastic leaded chip carrier. The device provides up to 16 inputs and 8 outputs. The PALCE16V8 can be electrically erased and reprogrammed. The programmable macrocell enables the device to function as a superset to the familiar 20-pin PLDs such as 16L8, 16R8, 16R6, and 16R4.

Logic Block Diagram (PDIP/CDIP)

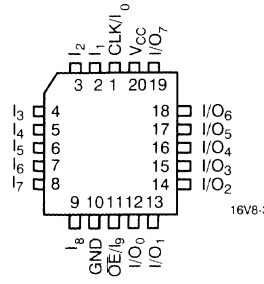


Pin Configuration

DIP
Top View



PLCC/LCC
Top View



PAL is a registered trademark of Advanced Micro Devices.

Functional Description (continued)

The PALCE16V8 features 8 product terms per output and 32 input terms into the AND array. The first product term in a macrocell can be used either as an internal output enable control or as a data product term.

There are a total of 18 architecture bits in the PALCE16V8 macrocell; two are global bits that apply to all macrocells and 16 that apply locally, two bits per macrocell. The architecture bits determine whether the macrocell functions as a register or combinatorial with inverting or noninverting output. The output enable control can come from an external pin or internally from a product term. The output can also be permanently enabled, functioning as a dedicated output or permanently disabled, functioning as a dedicated input. Feedback paths are selectable from either the input/output pin associated with the macrocell, the input/output pin associated with an adjacent pin, or from the macrocell register itself.

Power-Up Reset

All registers in the PALCE16V8 power-up to a logic LOW for predictable system initialization. For each register, the associated output pin will be HIGH due to active-LOW outputs.

Electronic Signature

An electronic signature word is provided in the PALCE16V8 that consists of 64 bits of programmable memory that can contain user-defined data.

Security Bit

A security bit is provided that defeats the readback of the internal programmed pattern when the bit is programmed.

Low Power

The Cypress PALCE16V8 provides low-power operation through the use of CMOS technology, and increased testability with Flash reprogrammability.

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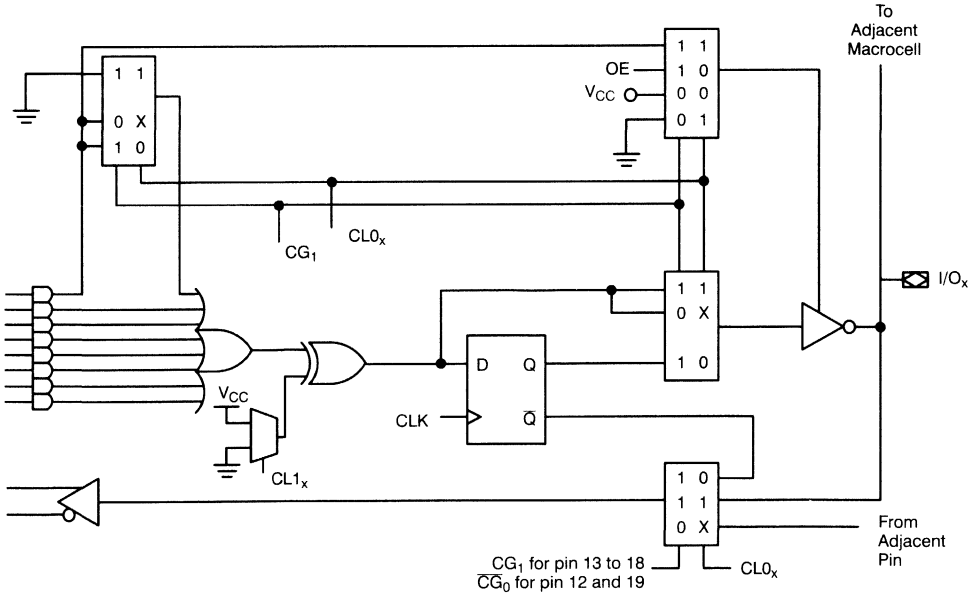
Configuration Table

CG_0	CG_1	$CL0_x$	Cell Configuration	Devices Emulated
0	1	0	Registered Output	Registered Med PALs
0	1	1	Combinatorial I/O	Registered Med PALs
1	0	0	Combinatorial Output	Small PALs
1	0	1	Input	Small PALs
1	1	1	Combinatorial I/O	16L8 only

Macrocell



16V8-4

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 24 mA

DC Programming Voltage 12.5V

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ±5%
Military[1]	−55°C to +125°C	5V ±10%
Industrial	−40°C to +85°C	5V ±10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	Com'l	2.4		V
			I_{OH} = −2 mA	Mil/Ind			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA	Com'l		0.5	V
			I_{OL} = 12 mA	Mil/Ind			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[3]			2.0		V
V_{IL}[4]	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[3]			−0.5	0.8	V
I_{IL}[5]	Input or I/O LOW Leakage Current	0V ≤ V_{IN} ≤ V_{IN} (Max.)				−100	µA
I_{IH}	Input or I/O HIGH Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}				10	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[6, 7]			−30	−90	mA
I_{CC}	Operating Power Supply Current	V_{CC} = Max., V_{IL} = 0V, V_{IH} = 3V, Output Open, f = 15 MHz (counter)	7 ns	Com'l		115	mA
			10, 15, 25 ns			90	mA
			−15L, −25L			55	mA
			10, 15, 25 ns	Mil/Ind		130	mA

Capacitance[7]

Parameter	Description	Test Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz	5	pF

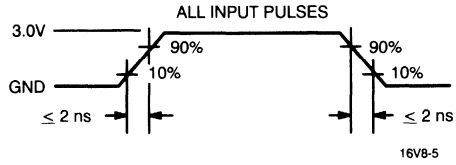
Endurance Characteristics[7]

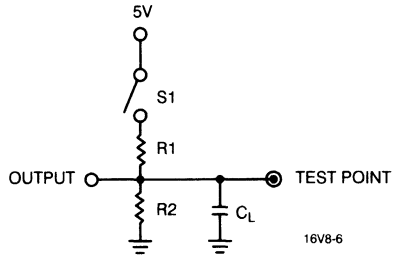
Parameter	Description	Test Conditions	Min.	Max.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions	100		Cycles

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. V_{IL} (Min.) is equal to −3.0V for pulse durations less than 20 ns.
5. The leakage current is due to the internal pull-up resistor on all pins.
6. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
7. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	200Ω	390Ω	390Ω	750Ω	1.5V
t_{PZX}, t_{EA}	Z ⧫ H: Open Z ⧫ L: Closed						1.5V
t_{PXZ}, t_{ER}	H ⧫ Z: Open L ⧫ Z: Closed	5 pF					H ⧫ Z: V_{OH} − 0.5V L ⧫ Z: V_{OL} + 0.5V

Commercial Switching Characteristics[2]

Parameter	Description	16V8–7		16V8–10		16V8–15		16V8–25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[8, 9]	3	7.5	3	10	3	15	3	25	ns
t_{PZX}	$\overline{OE}$ to Output Enable		6		10		15		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable		6		10		15		20	ns
t_{EA}	Input to Output Enable Delay[7]		9		10		15		25	ns
t_{ER}	Input to Output Disable Delay[7, 10]		9		10		15		25	ns
t_{CO}	Clock to Output Delay[8, 9]	2	5	2	7	2	10	2	12	ns
t_S	Input or Feedback Set-Up Time	5		7.5		12		15		ns
t_H	Input Hold Time	0		0		0		0		ns
t_P	External Clock Period ($t_{CO} + t_S$)	10		14.5		22		27		ns
t_{WH}	Clock Width HIGH[7]	4		6		8		12		ns
t_{WL}	Clock Width LOW[7]	4		6		8		12		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[7, 11]	100		69		45.5		37		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[7, 12]	125		83		62.5		41.6		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[7, 13]	125		74		50		40		MHz
t_{CF}	Register Clock to Feedback Input[7, 14]		3		6		8		10	ns
t_{PR}	Power-Up Reset Time[7]	1		1		1		1		µs

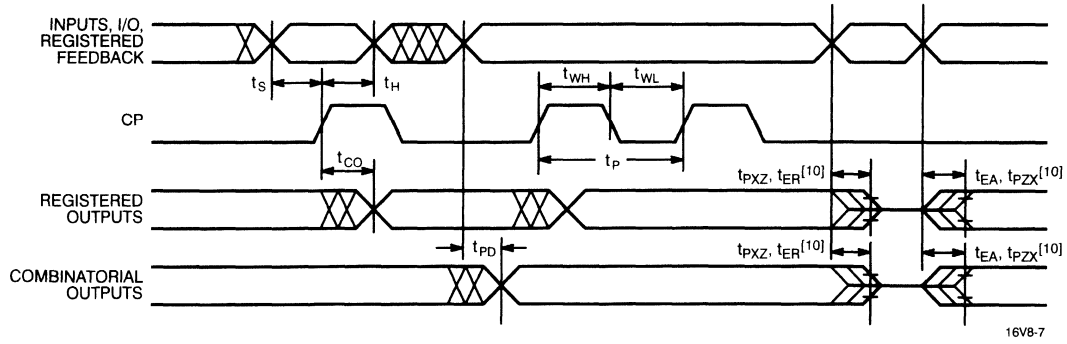
Notes:

8. Min. times are tested initially and after any design or process changes that may affect these parameters.
9. This specification is guaranteed for all device outputs changing state in a given access cycle.
10. This parameter is measured as the time after $\overline{OE}$ pin or internal disable input disables or enables the output pin. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below V_{OH} min. or a previous LOW level has risen to 0.5 volts above V_{OL} max.
11. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
12. This specification indicates the guaranteed maximum frequency at which the device can operate in data path mode.
13. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feedback can operate.
14. This parameter is calculated from the clock period at f_{MAX} internal ($1/f_{MAX3}$) as measured (see Note 10 above) minus t_S.

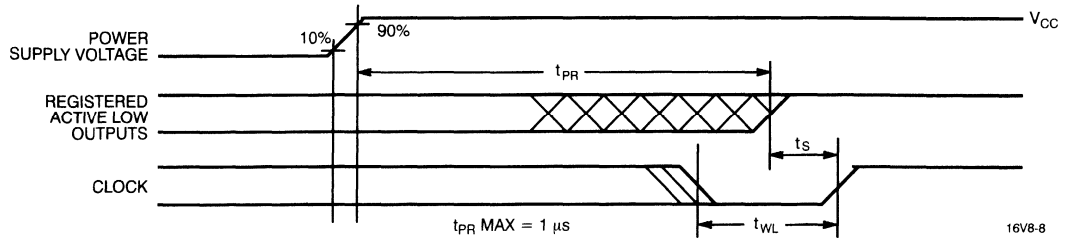
Military and Industrial Switching Characteristics[2]

Parameter	Description	16V8-10		16V8-15		16V8-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[8, 9]	3	10	3	15	3	25	ns
t_{PZX}	$\overline{OE}$ to Output Enable		10		15		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable		10		15		20	ns
t_{EA}	Input to Output Enable Delay[7]		10		15		25	ns
t_{ER}	Input to Output Disable Delay[7, 10]		10		15		25	ns
t_{CO}	Clock to Output Delay[8, 9]	2	7	2	10	2	12	ns
t_S	Input or Feedback Set-Up Time	10		12		15		ns
t_H	Input Hold Time	0		0		0		ns
t_P	External Clock Period ($t_{CO} + t_S$)	17		22		27		ns
t_{WH}	Clock Width HIGH[7]	6		8		12		ns
t_{WL}	Clock Width LOW[7]	6		8		12		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[7, 11]	58		45.5		37		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[7, 12]	83		62.5		41.6		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[7, 13]	62.5		50		40		MHz
t_{CF}	Register Clock to Feedback Input[7, 14]		6		8		10	ns
t_{PR}	Power-Up Reset Time[7]	1		1		1		µs

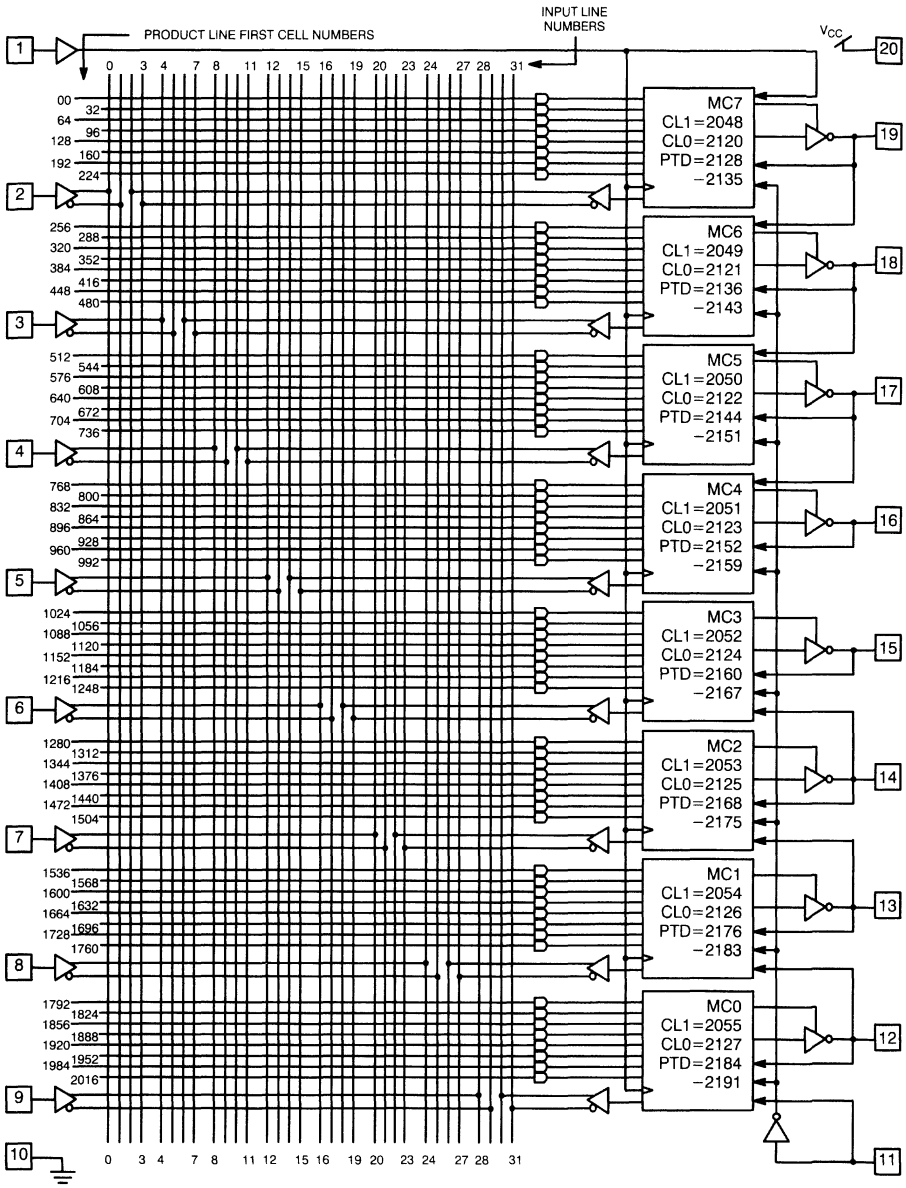
Switching Waveform



Power-Up Reset Waveform



Functional Logic Diagram for PALCE16V8



Ordering Information

I_{CC} (mA)	t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package Name	Package Type	Operating Range
115	7.5	5	5	PALCE16V8-7JC	J61	20-Lead Plastic Leaded Chip Carrier	Commercial
				PALCE16V8-7PC	P5	20-Lead (300-Mil) Molded DIP	
90	10	7.5	7	PALCE16V8-10JC	J61	20-Lead Plastic Leaded Chip Carrier	Commercial
				PALCE16V8-10PC	P5	20-Lead (300-Mil) Molded DIP	
130	10	10	7	PALCE16V8-10JI	J61	20-Lead Plastic Leaded Chip Carrier	Industrial
				PALCE16V8-10PI	P5	20-Lead (300-Mil) Molded DIP	
130	10	10	7	PALCE16V8-10DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALCE16V8-10LMB	L61	20-Pin Square Leadless Chip Carrier	
90	15	12	10	PALCE16V8-15JC	J61	20-Lead Plastic Leaded Chip Carrier	Commercial
				PALCE16V8-15PC	P5	20-Lead (300-Mil) Molded DIP	
130	15	12	10	PALCE16V8-15JI	J61	20-Lead Plastic Leaded Chip Carrier	Industrial
				PALCE16V8-15PI	P5	20-Lead (300-Mil) Molded DIP	
130	15	12	10	PALCE16V8-15DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALCE16V8-15LMB	L61	20-Pin Square Leadless Chip Carrier	
55	25	12	10	PALCE16V8L-25JC	J61	20-Lead Plastic Leaded Chip Carrier	Commercial
				PALCE16V8L-25PC	P5	20-Lead (300-Mil) Molded DIP	
55	25	15	12	PALCE16V8L-25JC	J61	20-Lead Plastic Leaded Chip Carrier	Commercial
				PALCE16V8L-25PC	P5	20-Lead (300-Mil) Molded DIP	
90	25	15	12	PALCE16V8-25JC	J61	20-Lead Plastic Leaded Chip Carrier	Commercial
				PALCE16V8-25PC	P5	20-Lead (300-Mil) Molded DIP	
130	25	15	12	PALCE16V8-25JI	J61	20-Lead Plastic Leaded Chip Carrier	Industrial
				PALCE16V8-25PI	P5	20-Lead (300-Mil) Molded DIP	
130	25	15	12	PALCE16V8-25DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALCE16V8-25LMB	L61	20-Pin Square Leadless Chip Carrier	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	9, 10, 11
t_{CO}	9, 10, 11
t_S	9, 10, 11
t_H	9, 10, 11

Document #: 38-00364-A

CYPRESS

ADVANCED INFORMATION **PALCE20V8**

Flash Erasable, Reprogrammable CMOS PAL® Device

Features

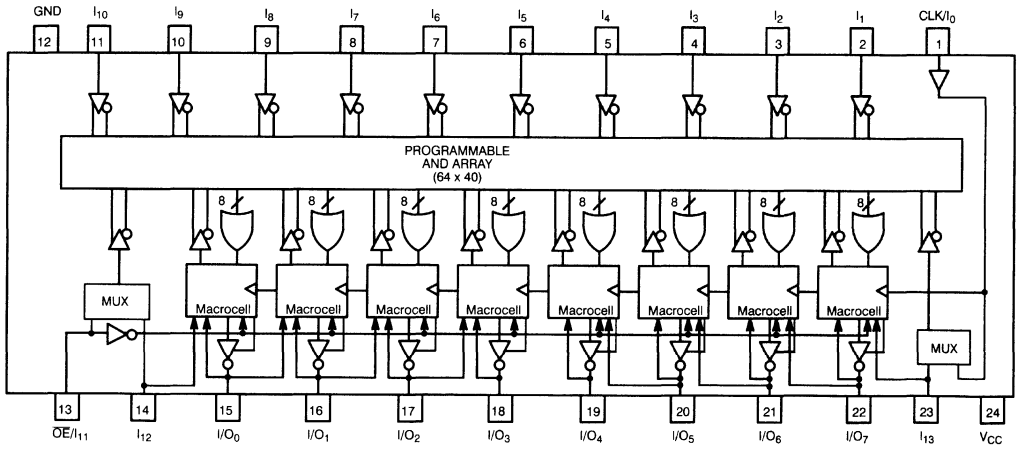
- **Advanced second-generation PAL architecture**
- **Low power**
  - **— 90 mA max. commercial (10, 15, 25 ns)**
  - **— 115 mA max. commercial (7 ns)**
  - **— 130 mA max. military/industrial (15, 25 ns)**
- **Quarter power version**
  - **— 55 mA max. commercial**
- **CMOS Flash technology for electrical erasability and reprogrammability**
- **User-programmable macrocell**
  - **— Output polarity control**
  - **— Individually selectable for registered or combinatorial operation**
- **DIP, LCC, and PLCC available**
  - **— 7.5, 10, 15, and 25 ns com'l version**
    5 ns t_{CO}
    5 ns t_S
    7.5 ns t_{PD}
    125-MHz state machine
  - **— 10, 15, and 25 ns military/industrial versions**
    7 ns t_{CO}
    10 ns t_S
    10 ns t_{PD}
    62-MHz state machine
- **High reliability**
  - **— Proven Flash technology**
  - **— 100% programming and functional testing**

Functional Description

The Cypress PALCE20V8 is a CMOS Flash Erasable second-generation programmable array logic device. It is implemented with the familiar sum-of-product (AND-OR) logic structure and the programmable macrocell.

The PALCE20V8 is executed in a 24-pin 300-mil molded DIP, a 300-mil cerdip, a 28-lead square ceramic leadless chip carrier, and a 28-lead square plastic leaded chip carrier. The device provides up to 20 inputs and 8 outputs. The PALCE20V8 can be electrically erased and reprogrammed. The programmable macrocell enables the device to function as a superset to the familiar 24-pin PLDs such as 20L8, 20R8, 20R6, 20R4.

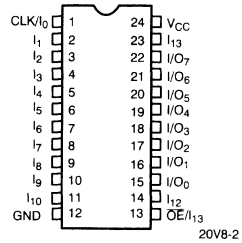
Logic Block Diagram (PDIP/CDIP)



Pin Configuration

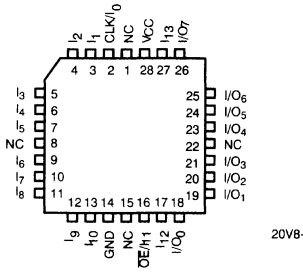
20V8-1

DIP
Top View



20V8-2

PLCC/LCC
Top View



20V8-3

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Document #: 38-00367-A

PLDC20G10B/PLDC20G10

CMOS Generic 24-Pin Reprogrammable Logic Device

Features

- **Fast**
  - **Commercial: t_{PD} = 15 ns, t_{CO} = 10 ns, t_S = 12 ns**
  - **Military: t_{PD} = 20 ns, t_{CO} = 15 ns, t_S = 15 ns**
- **Low power**
  - **I_{CC} max.: 70 mA, commercial**
  - **I_{CC} max.: 100 mA, military**
- **Commercial and military temperature range**
- **User-programmable output cells**
  - **Selectable for registered or combinatorial operation**
  - **Output polarity control**
  - **Output enable source selectable from pin 13 or product term**
- **Generic architecture to replace standard logic functions including: 20L10, 20L8, 20R8, 20R6, 20R4, 12L10, 14L8, 16L6, 18L4, 20L2, and 20V8**
- **Eight product terms and one OE product term per output**
- **CMOS EPROM technology for reprogrammability**
- **Highly reliable**
  - **Uses proven EPROM technology**
  - **Fully AC and DC tested**
  - **Security feature prevents logic pattern duplication**
  - **±10% power supply voltage and higher noise immunity**

Functional Description

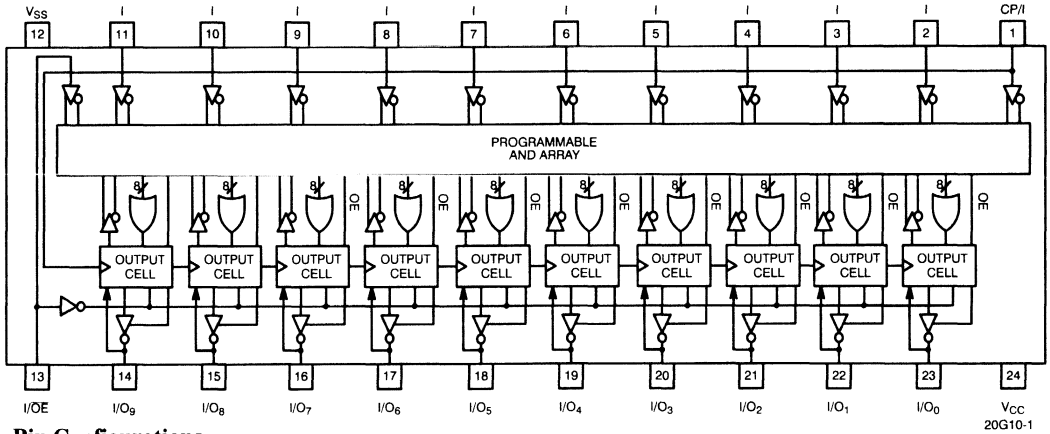
Cypress PLD devices are high-speed electrically programmable logic devices. These devices utilize the sum-of-products (AND-OR) structure providing users the ability to program custom logic functions for unique requirements.

In an unprogrammed state the AND gates are connected via EPROM cells to both the true and complement of every input. By selectively programming the EPROM cells, AND gates may be connected to either the true or complement or disconnected from both true and complement inputs.

Cypress PLDC20G10 uses an advanced 0.8-micron CMOS technology and a proven EPROM cell as the programmable element. This technology and the inherent

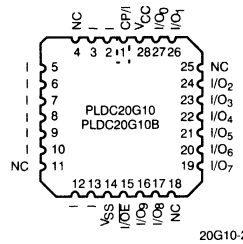
2

Logic Block Diagram

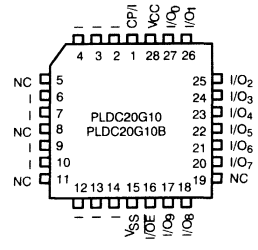


Pin Configurations

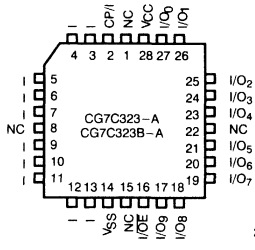
LCC
Top View



STD PLCC
Top View



JEDEC PLCC[1]
Top View



Note:

1. The CG7C323 is the PLDC20G10 packaged in the JEDEC-compatible 28-pin PLCC pinout. Pin function and pin order is identical for both PLCC pinouts. The difference is in the location of the "no connect" or NC pins.

Selection Guide

Generic Part Number	I_{CC} (mA)		t_{PD} (ns)		t_S (ns)		t_{CO} (ns)	
	Com/Ind	Mil	Com/Ind	Mil	Com/Ind	Mil	Com/Ind	Mil
20G10B-15	70		15		12		10	
20G10B-20	70	100	20	20	12	15	12	15
20G10B-25		100		25		18		15
20G10-25	55		25		15		15	
20G10-30		80		30		20		20
20G10-35	55		35		30		25	
20G10-40		80		40		35		25

Functional Description (continued)

advantage of being able to program and erase each cell enhances the reliability and testability of the circuit. This reduces the burden on the customer to test and to handle rejects.

A preload function allows the registered outputs to be preset to any pattern during testing. Preload is important for testing the functionality of the Cypress PLD device.

20G10 Functional Description

The PLDC20G10 is a generic 24-pin device that can be programmed to logic functions that include but are not limited to: 20L10, 20L8, 20R8, 20R6, 20R4, 12L10, 14L8, 16L6, 18L4, 20L2, and 20V8. Thus, the PLDC20G10 provides significant design, inventory and programming flexibility over dedicated 24-pin devices. It is executed in a 24-pin 300-mil molded DIP and a 300-mil windowed cerDIP. It provides up to 22 inputs and 10 outputs. When the windowed cerDIP is exposed to UV light, the 20G10 is erased and then can be reprogrammed.

The programmable output cell provides the capability of defining the architecture of each output individually. Each of the 10 output cells may be configured with registered or combinatorial outputs, active HIGH or active LOW outputs, and product term or Pin 13 generated output enables. Three architecture bits determine the configurations as shown in the Configuration Table and in *Figures 1* through *8*. A total of eight different configurations are possible, with the two most common shown in *Figure 3* and *Figure 5*. The default or unprogrammed state is registered/active/LOW/Pin 11 OE. The entire programmable output cell is shown in the next section.

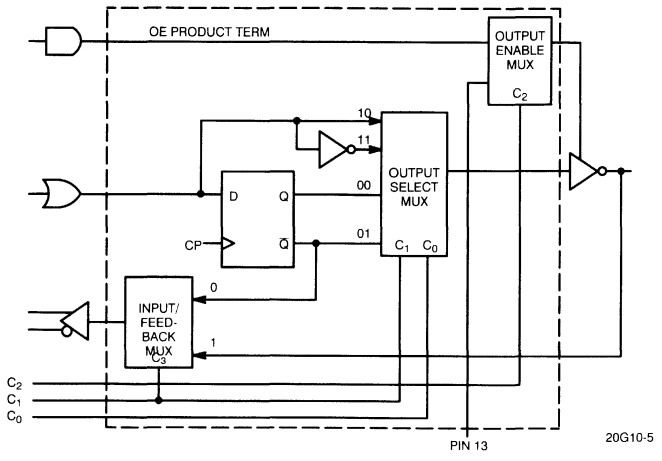
The architecture bit 'C1' controls the registered/combinatorial option. In either combinatorial or registered configuration, the output can serve as an I/O pin, or if the output is disabled, as an input only. Any unused inputs should be tied to ground. In either registered or combinatorial configuration, the output of the register is fed back to the array. This allows the creation of control-state machines by providing the next state. The register is clocked by the signal from Pin 1. The register is initialized on power up to Q output LOW and $\overline{Q}$ output HIGH.

In both the combinatorial and registered configurations, the source of the output enable signal can be individually chosen with architecture bit 'C2'. The OE signal may be generated within the array, or from the external $\overline{OE}$ (Pin 13). The Pin 13 allows direct control of the outputs, hence having faster enable/disable times.

Each output cell can be configured for output polarity. The output can be either active HIGH or active LOW. This option is controlled by architecture bit 'C0'.

Along with this increase in functional density, the Cypress PLDC20G10 provides lower-power operation through the use of CMOS technology and increased testability with a register preload feature.

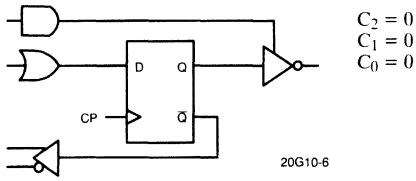
Programmable Output Cell



Configuration Table

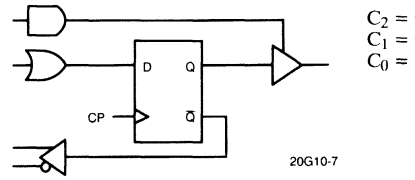
Figure	C_2	C_1	C_0	Configuration
1	0	0	0	Product Term OE/Registered/Active LOW
2	0	0	1	Product Term OE/Registered/Active HIGH
5	0	1	0	Product Term OE/Combinatorial/Active LOW
6	0	1	1	Product Term OE/Combinatorial/Active HIGH
3	1	0	0	Pin 13 OE/Registered/Active LOW
4	1	0	1	Pin 13 OE/Registered/Active HIGH
7	1	1	0	Pin 13 OE/Combinatorial/Active LOW
8	1	1	1	Pin 13 OE/Combinatorial/Active HIGH

Registered Output Configurations



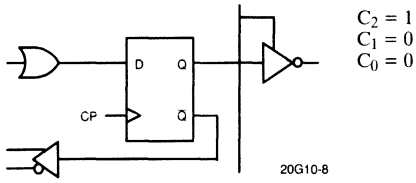
$C_2 = 0$
$C_1 = 0$
$C_0 = 0$

Figure 1. Product Term OE/Active LOW



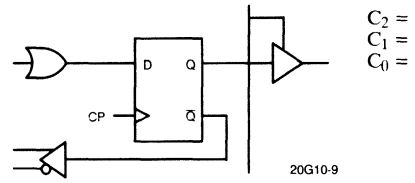
$C_2 = 0$
$C_1 = 0$
$C_0 = 1$

Figure 2. Product Term OE/Active HIGH



$C_2 = 1$
$C_1 = 0$
$C_0 = 0$

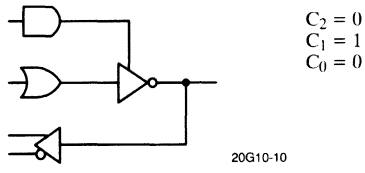
Figure 3. Pin 13 OE/Active LOW



$C_2 = 1$
$C_1 = 0$
$C_0 = 1$

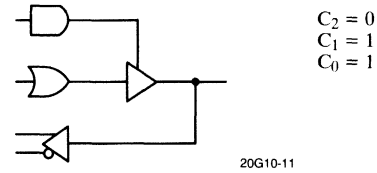
Figure 4. Pin 13 OE/Active HIGH

Combinatorial Output Configurations[2]



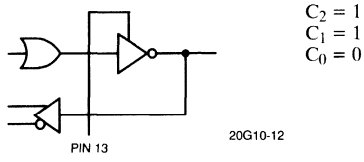
$C_2 = 0$
$C_1 = 1$
$C_0 = 0$

Figure 5. Product Term OE/Active LOW



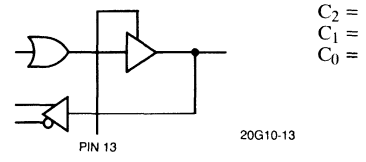
$C_2 = 0$
$C_1 = 1$
$C_0 = 1$

Figure 6. Product Term OE/Active HIGH



$C_2 = 1$
$C_1 = 1$
$C_0 = 0$

Figure 7. Pin 13 OE/Active LOW



$C_2 = 1$
$C_1 = 1$
$C_0 = 1$

Figure 8. Pin 13 OE/Active HIGH

Note:
2. Bidirectional I/O configurations are possible only when the combinatorial output option is selected

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (LOW) ..... 16 mA

DC Programming Voltage
PLDC20G10B and CG7C323B−A 13.0V
PLDC20G10 and CG7C323−A 14.0V

Latch-Up Current ..... >200 mA

Static Discharge Voltage ..... >500V (per MIL−STD−883, Method 8015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ±10%
Military[3]	−55°C to +125°C	5V ±10%
Industrial	−40°C to +85°C	5V ±10%

Electrical Characteristics Over the Operating Range (Unless Otherwise Noted)[4]

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	Com'l/Ind	2.4		V
			I_{OH} = −2 mA	Military			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA	Com'l/Ind		0.5	V
			I_{OL} = 12 mA	Military			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[5]			2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[5]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$			−10	+10	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[6, 7]				− 90	mA
I_{CC}	Power Supply Current	$0 \le V_{IN} \le V_{CC}$ V_{CC} = Max., I_{OUT} = 0 mA Unprogrammed Device	Com'l/Ind−15, −20			70	mA
			Com'l/Ind−25, −35			55	mA
			Military−20, −25			100	mA
			Military−30, −40			80	mA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			−100	100	μA

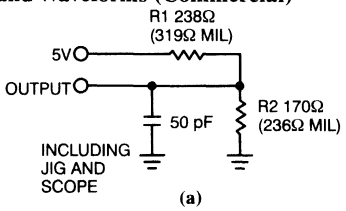
Capacitance[7]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	10	pF
C_{OUT}	Output Capacitance	V_{IN} = 2.0V, V_{CC} = 5.0V	10	pF

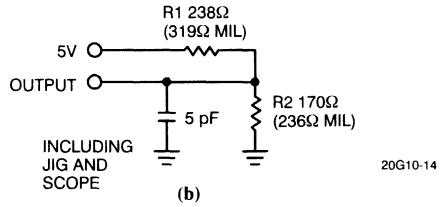
Notes:

3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.
5. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
6. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
7. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms (Commercial)



(a)



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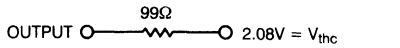
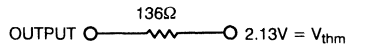
(b)

Equivalent to: THÉVENIN EQUIVALENT (Commercial)



20G10-15

Equivalent to: THÉVENIN EQUIVALENT (Military/Industrial)



20G10-16

Switching Characteristics Over Operating Range[3, 8, 9]

Parameter	Description	Commercial								Unit
		B-15		B-20		-25		-35		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Non-Registered Output		15		20		25		35	ns
t_{EA}	Input to Output Enable		15		20		25		35	ns
t_{ER}	Input to Output Disable		15		20		25		35	ns
t_{PZX}	Pin 11 to Output Enable		12		15		20		25	ns
t_{PXZ}	Pin 11 to Output Disable		12		15		20		25	ns
t_{CO}	Clock to Output		10		12		15		25	ns
t_S	Input or Feedback Set-Up Time	12		12		15		30		ns
t_H	Hold Time	0		0		0		0		ns
t_P[10]	Clock Period	22		24		30		55		ns
t_{WH}	Clock High Time	8		10		12		17		ns
t_{WL}	Clock Low Time	8		10		12		17		ns
f_{MAX}[11]	Maximum Frequency	45.4		41.6		33.3		18.1		MHz

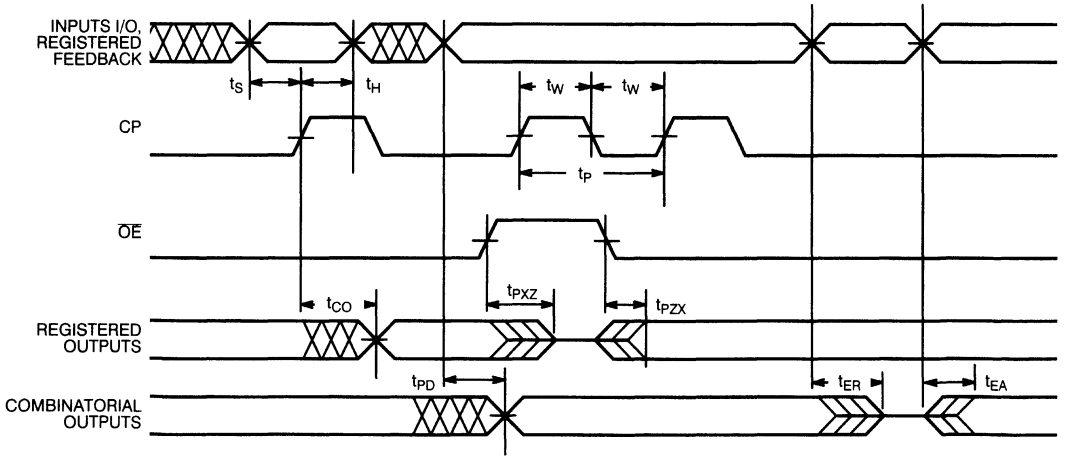
Notes:

8. Part (a) of AC Test Loads and Waveforms used for all parameters except t_{ER}, t_{PZX}, and t_{PXZ}. Part (b) of AC Test Loads and Waveforms used for t_{ER}, t_{PZX}, and t_{PXZ}.
9. The parameters t_{ER} and t_{PXZ} are measured as the delay from the input disable logic threshold transition to $V_{OH} - 0.5V$ for an enabled HIGH output or $V_{OL} + 0.5V$ for an enabled LOW input.
10. t_R minimum guaranteed clock period is that guaranteed for state machine operation and is calculated from $t_P = t_S + t_{CO}$. The minimum guaranteed period for registered data path operation (no feedback) can be calculated as the greater of $(t_{WH} + t_{WL})$ or $(t_S + t_H)$.
11. f_{MAX}, minimum guaranteed operating frequency, is that guaranteed for state machine operation and is calculated from $f_{MAX} = 1/(t_S + t_{CO})$. The minimum guaranteed f_{MAX} for registered data path operation (no feedback) can be calculated as the lower of $1/(t_{WH} + t_{WL})$ or $1/(t_S + t_H)$.

Switching Characteristics Over Operating Range[3, 8, 9] (continued)

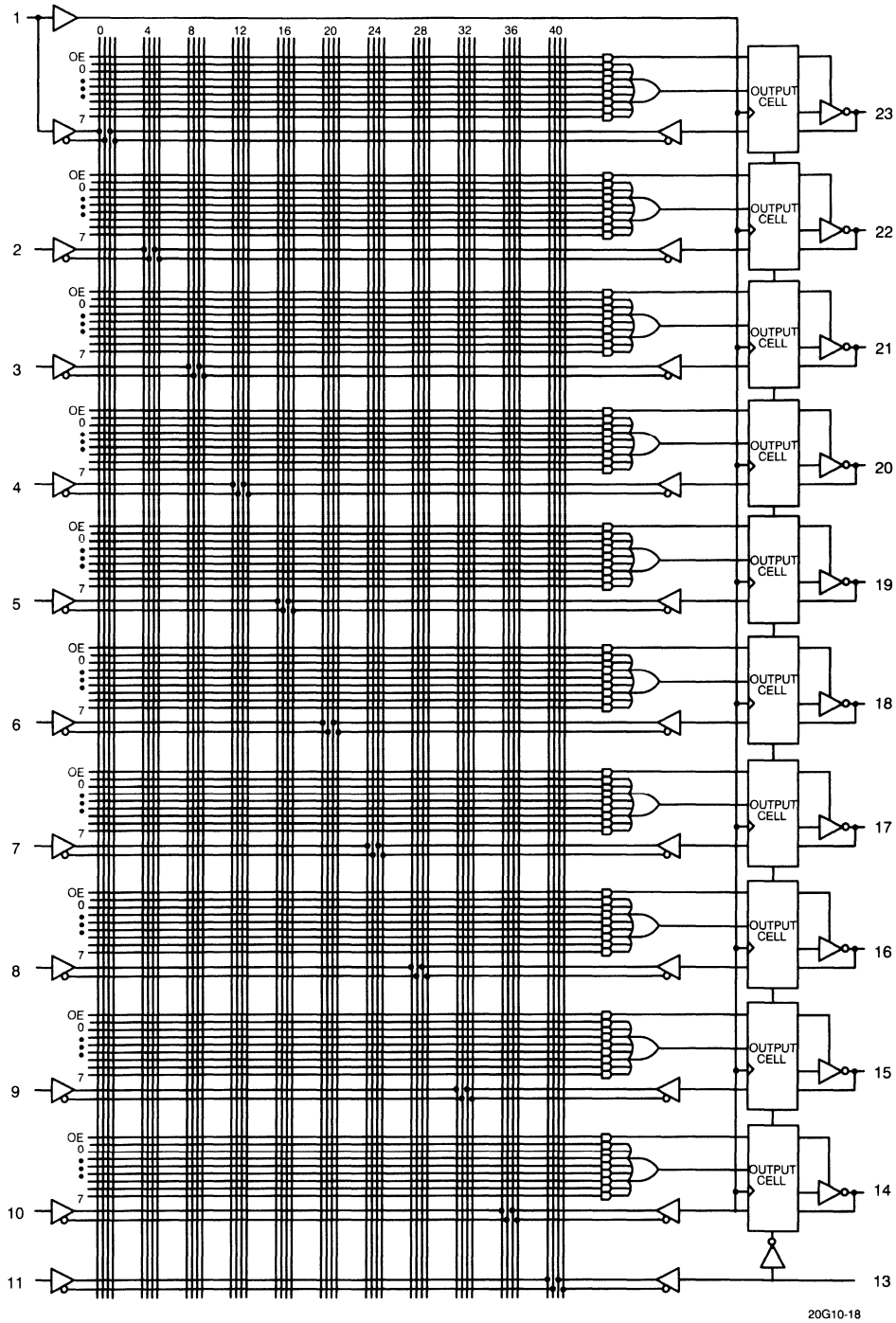
Parameter	Description	Military/Industrial								Unit
		B–20		B–25		–30		–40		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Non-Registered Output		20		25		30		40	ns
t_{EA}	Input to Output Enable		20		25		30		40	ns
t_{ER}	Input to Output Disable		20		25		30		40	ns
t_{PZX}	Pin 11 to Output Enable		17		20		25		25	ns
t_{PXZ}	Pin 11 to Output Disable		17		20		25		25	ns
t_{CO}	Clock to Output		15		15		20		25	ns
t_S	Input or Feedback Set-Up Time	15		18		20		35		ns
t_H	Hold Time	0		0		0		0		ns
t_P[10]	Clock Period	30		33		40		60		ns
t_{WH}	Clock High Time	12		14		16		22		ns
t_{WL}	Clock Low Time	12		14		16		22		ns
f_{MAX}[11]	Maximum Frequency	33.3		30.3		25.0		16.6		MHz

Switching Waveform



20G10-17

Functional Logic Diagram



Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
15	12	10	70	PLDC20G10B–15JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	Commercial/ Industrial
				PLDC20G10B–15PC/PI	P13	24-Lead (300-Mil) Molded DIP	
				PLDC20G10B–15WC	W14	24-Lead (300-Mil) Windowed CerDIP	
				CG7C323B–A15JC/JI[12]	J64	28-Lead Plastic Leaded Chip Carrier	
20	12	12	70	PLDC20G10B–20JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	Commercial/ Industrial
				PLDC20G10B–20PC/PI	P13	24-Lead (300-Mil) Molded DIP	
				PLDC20G10B–20WC	W14	24-Lead (300-Mil) Windowed CerDIP	
				CG7C323B–A20JC/JI[12]	J64	28-Lead Plastic Leaded Chip Carrier	
20	15	15	100	PLDC20G10B–20DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PLDC20G10B–20LMB	L64	28-Square Leadless Chip Carrier	
				PLDC20G10B–20WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
25	15	15	55	PLDC20G10–25JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	Commercial/ Industrial
				PLDC20G10–25PC/PI	P13	24-Lead (300-Mil) Molded DIP	
				PLDC20G10–25WC	W14	24-Lead (300-Mil) Windowed CerDIP	
				CG7C323–A25JC/JI[12]	J64	28-Lead Plastic Leaded Chip Carrier	
25	18	15	100	PLDC20G10B–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PLDC20G10B–25LMB	L64	28-Square Leadless Chip Carrier	
				PLDC20G10B–25WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
30	20	20	80	PLDC20G10–30DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PLDC20G10–30LMB	L64	28-Square Leadless Chip Carrier	
				PLDC20G10–30WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
35	30	25	55	PLDC20G10–35JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	Commercial/ Industrial
				PLDC20G10–35PC/PI	P13	24-Lead (300-Mil) Molded DIP	
				PLDC20G10–35WC	W14	24-Lead (300-Mil) Windowed CerDIP	
				CG7C323–A35JC/JI[12]	J64	28-Lead Plastic Leaded Chip Carrier	
40	35	25	80	PLDC20G10–40DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PLDC20G10–40LMB	L64	28-Square Leadless Chip Carrier	
				PLDC20G10–40WMB	W14	24-Lead (300-Mil) Windowed CerDIP	

Note:
12. The CG7C323 is the PLD20G10 packaged in the JEDEC-compatible 28-pin PLCC pinout. Pin function and pin order is identical for both PLCC pinouts. The principle difference is in the location of the "no connect" (NC) pins.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	9, 10, 11
t_{PZX}	9, 10, 11
t_{CO}	9, 10, 11
t_S	9, 10, 11
t_H	9, 10, 11

Document #: 38–00019–G

PLD20G10C

Generic 24-Pin PAL® Device

Features

- **Ultra high speed supports today's and tomorrow's fastest microprocessors**
  - **— t_{PD} = 7.5 ns**
  - **— t_{SU} = 3 ns**
  - **— f_{MAX} = 105 MHz**
- **Reduced ground bounce and undershoot**
- **PLCC and LCC packages with additional V_{CC} and V_{SS} pins for lowest ground bounce**
- **Generic architecture to replace standard logic functions including: 20L10, 20L8, 20R8, 20R6, 20R4, 12L10, 14L8, 16L6, 18L4, 20L2, and 20V8**
- **Up to 22 inputs and 10 outputs for more logic power**
- **10 user-programmable output macrocells**
  - **— Output polarity control**
  - **— Registered or combinatorial operation**
  - **— Pin or product term output enable control**
- **Preload capability for flexible design and testability**
- **High reliability**
  - **— Proven Ti-W fuse technology**
  - **— AC and DC tested at the factory**
- **Security Fuse**

Functional Description

The PLD20G10C is a generic 24-pin device that can be used in place of 24 PAL devices. Thus, the PLD20G10C provides significant design, inventory, and programming flexibility over dedicated 24-pin devices.

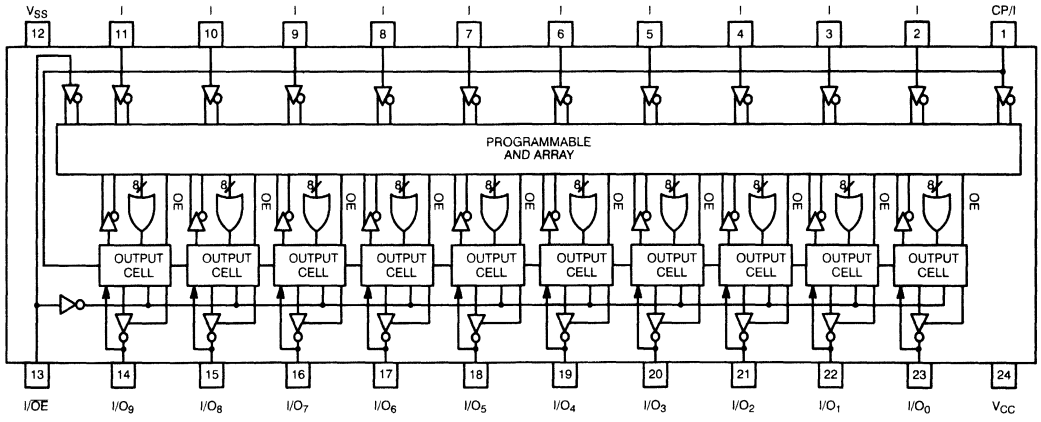
Using BiCMOS process and Ti-W fuses, the PLD20G10C implements the familiar sum-of-products (AND-OR) logic structure. It provides 12 dedicated input pins and 10 I/O pins (see Logic Block Diagram). By selecting each I/O pin as permanent or temporary input, up to 22 inputs can be achieved. Applications requiring up to 21 inputs and a single output, down to 12 inputs and 10 outputs can be realized. The output enable product term available on each I/O or a common pin controlled $\overline{OE}$ function allows this selection.

The PLD20G10C automatically resets on power-up. The Q output of all internal registers is set to a logic LOW and the $\overline{Q}$ output to a logic HIGH. In addition, the PRELOAD capability allows the registers to be set to any desired state during testing.

A security fuse is provided to prevent copying of the device fuse pattern.

2

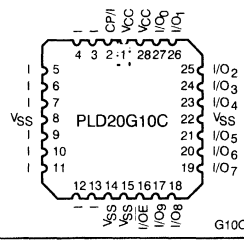
Logic Block Diagram and PDIP (P)/CDIP (D) Pin Configuration



G10C-1

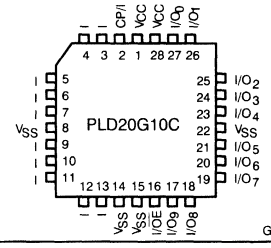
Pin Configurations

LCC (L)
Top View



G10C-2

PLCC (J)
Top View



G10C-3

PAL is a registered trademark of Advanced Micro Devices

Selection Guide

		20G10C–7	20G10C–10	20G10C–12	20G10C–15
I_{CC} (mA)	Commercial	190	190	190	
	Military		190	190	190
t_{PD} (ns)	Commercial	7.5	10	12	
	Military		10	12	15
t_S (ns)	Commercial	3.0	3.6	4.5	
	Military		3.6	4.5	7.5
t_{CO} (ns)	Commercial	6.5	7.5	9.5	
	Military		7.5	9.5	10
f_{MAX} (MHz)	Commercial	105	90	71	
	Military		90	71	57

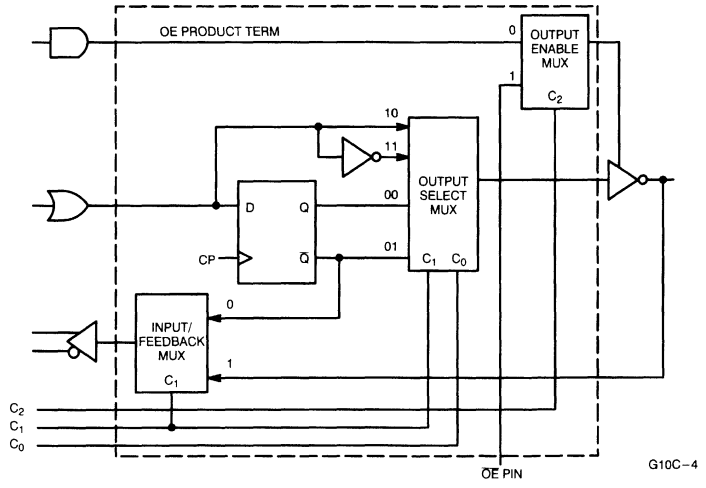
Programmable Macrocell

The PLD20G10C has 10 programmable I/O macrocells (see Macrocell). Two fuses (C_1 and C_0) can be programmed to configure output in one of four ways. Accordingly, each output can be registered or combinatorial with an active HIGH or active LOW polarity. The feedback to the array is also from this output. An additional fuse (C_2) determines the source of the output enable signal. The signal can be generated either from the individual OE product term or from a common external $\overline{OE}$ pin.

Programming

The PLD20G10C can be programmed using the *Impulse3*™ programmer available from Cypress Semiconductor. See third party information is Cypress's Third Party Tools datasheet for further information.

Macrocell

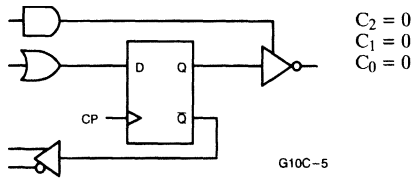


Impulse3 is a trademark of Cypress Semiconductor Corporation.

Configuration Table

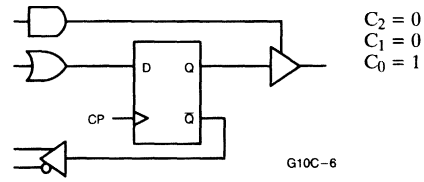
Figure	C_2	C_1	C_0	Configuration
1	0	0	0	Product Term OE/Registered/Active LOW
2	0	0	1	Product Term OE/Registered/Active HIGH
5	0	1	0	Product Term OE/Combinatorial/Active LOW
6	0	1	1	Product Term OE/Combinatorial/Active HIGH
3	1	0	0	Pin $\overline{OE}$/Registered/Active LOW
4	1	0	1	Pin $\overline{OE}$/Registered/Active HIGH
7	1	1	0	Pin $\overline{OE}$/Combinatorial/Active LOW
8	1	1	1	Pin $\overline{OE}$/Combinatorial/Active HIGH

Registered Output Configurations



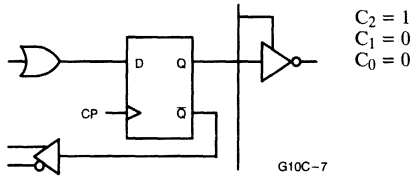
$C_2 = 0$
$C_1 = 0$
$C_0 = 0$

Figure 1. Product Term OE/Active LOW



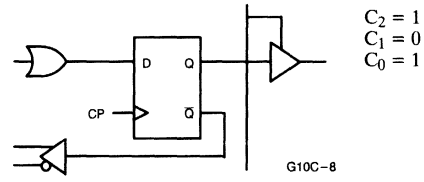
$C_2 = 0$
$C_1 = 0$
$C_0 = 1$

Figure 2. Product Term OE/Active HIGH



$C_2 = 1$
$C_1 = 0$
$C_0 = 0$

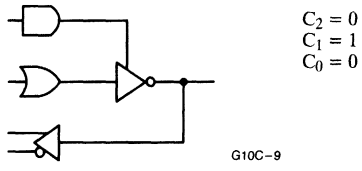
Figure 3. Pin $\overline{OE}$/Active LOW



$C_2 = 1$
$C_1 = 0$
$C_0 = 1$

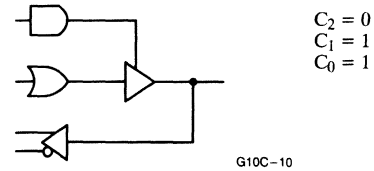
Figure 4. Pin $\overline{OE}$/Active HIGH

Combinatorial Output Configurations[1]



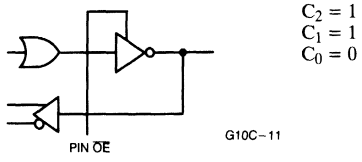
$C_2 = 0$
$C_1 = 1$
$C_0 = 0$

Figure 5. Product Term OE/Active LOW



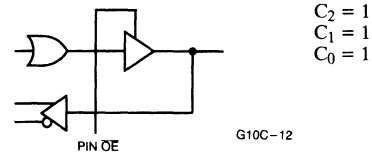
$C_2 = 0$
$C_1 = 1$
$C_0 = 1$

Figure 6. Product Term OE/Active HIGH



$C_2 = 1$
$C_1 = 1$
$C_0 = 0$

Figure 7. Pin $\overline{OE}$/Active LOW



$C_2 = 1$
$C_1 = 1$
$C_0 = 1$

Figure 8. Pin $\overline{OE}$/Active HIGH

Note:
1. Bidirectional I/O configurations are possible only when the combinatorial output option is selected.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to V_{CC}

DC Input Voltage ..... −0.5V to V_{CC}

DC Input Current ..... − 30 mA to +5 mA (except during programming)

DC Program Voltage 10V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Military[2]	−55°C to +125°C	4.75V to 5.5V

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	Com'l	2.4		V
			I_{OH} = −2 mA	Mil			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA	Com'l		0.5	V
			I_{OL} = 12 mA	Mil			
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs[3]			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs[3]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le 2.7V$, V_{CC} = Max.			−250	50	µA
I_I	Maximum Input Current	V_{IN} = V_{CC}, V_{CC} = Max.		Com'l		100	µA
				Mil		250	
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			−100	100	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[4]			−30	−120	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = GND, Outputs Open		Com'l		190	mA
				Mil		190	

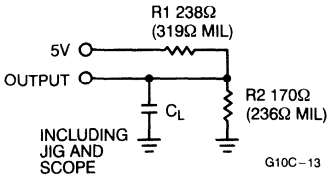
Capacitance[5]

Parameter	Description	Max.	Unit
C_{IN}	Input Capacitance	8	pF
C_{OUT}	Output Capacitance	10	pF

Notes:

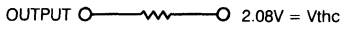
2. T_A is the "instant on" case temperature.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



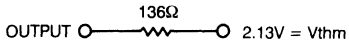
C_L[6]	Package
15 pF	P/D
50 pF	J/K/L

Equivalent to: THÉVENIN EQUIVALENT

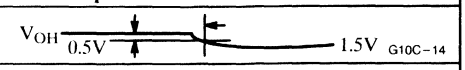
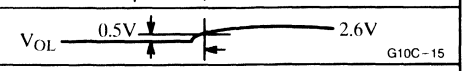
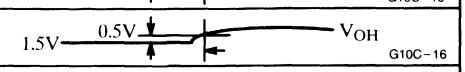
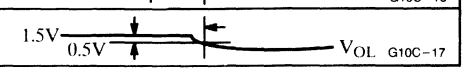


Commercial

Equivalent to: THÉVENIN EQUIVALENT



Military

Parameter	V_{th}	Output Waveform—Measurement Level
$t_{ER(-)}$, t_{PHZ}	1.5V	
$t_{ER(+)}$, t_{PLZ}	2.6V	
$t_{EA(+)}$, t_{PZH}	1.5V	
$t_{EA(-)}$, t_{PZL}	1.5V	

Note:
6. C_L = 5 pF for t_{ER} and t_{PXZ} measurements for all packages.

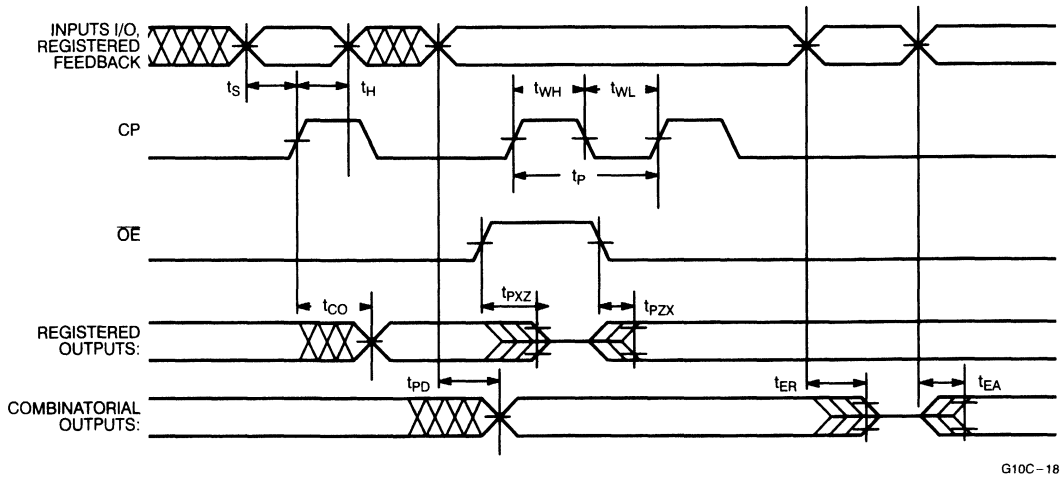
Switching Characteristics PLD20G10C[7]

Parameter	Description	20G10C–7		20G10C–10		20G10C–12		20G10C–15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[8]	2	7.5	2	10	2	12	2	15	ns
t_{EA}	Input to Output Enable Delay	2	7.5	2	10	2	12	2	15	ns
t_{ER}	Input to Output Disable Delay[9]	2	7.5	2	10	2	12	2	15	ns
t_{PZX}	$\overline{OE}$ Input to Output Enable Delay	2	7.5	2	10	2	12	2	15	ns
t_{PXZ}	$\overline{OE}$ Input to Output Disable Delay	2	7.5	2	10	2	12	2	15	ns
t_{CO}	Clock to Output Delay[8]	1	6.5	1	7.5	1	9.5	1	10	ns
t_S	Input or Feedback Set-Up Time	3		3.6		4.5		7.5		ns
t_H	Input Hold Time	0		0		0		0		ns
t_P	External Clock Period ($t_{CO} + t_S$)	9		11.1		14		17.5		ns
t_{WH}	Clock Width HIGH[5]	3		3		3		6		ns
t_{WL}	Clock Width LOW[5]	3		3		3		6		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[10]	105		90		71		57		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[5, 11]	166		166		166		83		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[12]	133		100		83		66		MHz
t_{CF}	Register Clock to Feedback Input[13]		4.5		6.4		7.5		7.5	ns
t_{PR}	Power-Up Reset Time[14]	1		1		1		1		μs

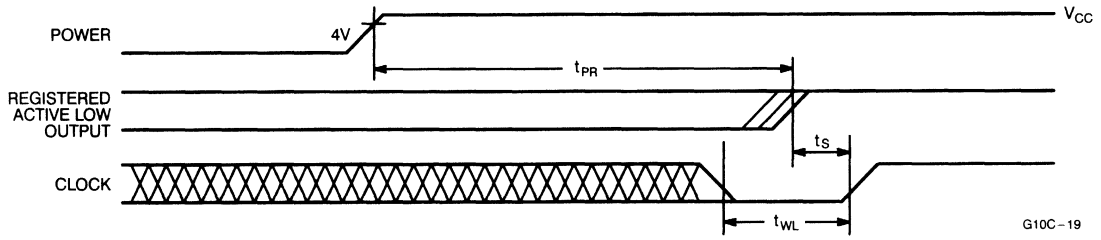
Notes:

7. AC test load used for all parameters except where noted.
8. This specification is guaranteed for all device outputs changing state in a given access cycle.
9. This parameter is measured as the time after output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below V_{OH} min. or a previous LOW level has risen to 0.5 volts above V_{OL} max.
10. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
11. This specification indicates the guaranteed maximum frequency at which an individual output register can be cycled.
12. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feedback can operate. This parameter is tested periodically by sampling production product.
13. This parameter is calculated from the clock period at f_{MAX} internal (f_{MAX3}) as measured (see Note 12) minus t_S.
14. The registers in the PLD20G10C have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to a logic LOW state. The output state will depend on the polarity of the output buffer. This feature is useful in establishing state machine initialization. To insure proper operation, the rise in V_{CC} must be monotonic and the timing constraints depicted in power-up reset waveforms must be satisfied.

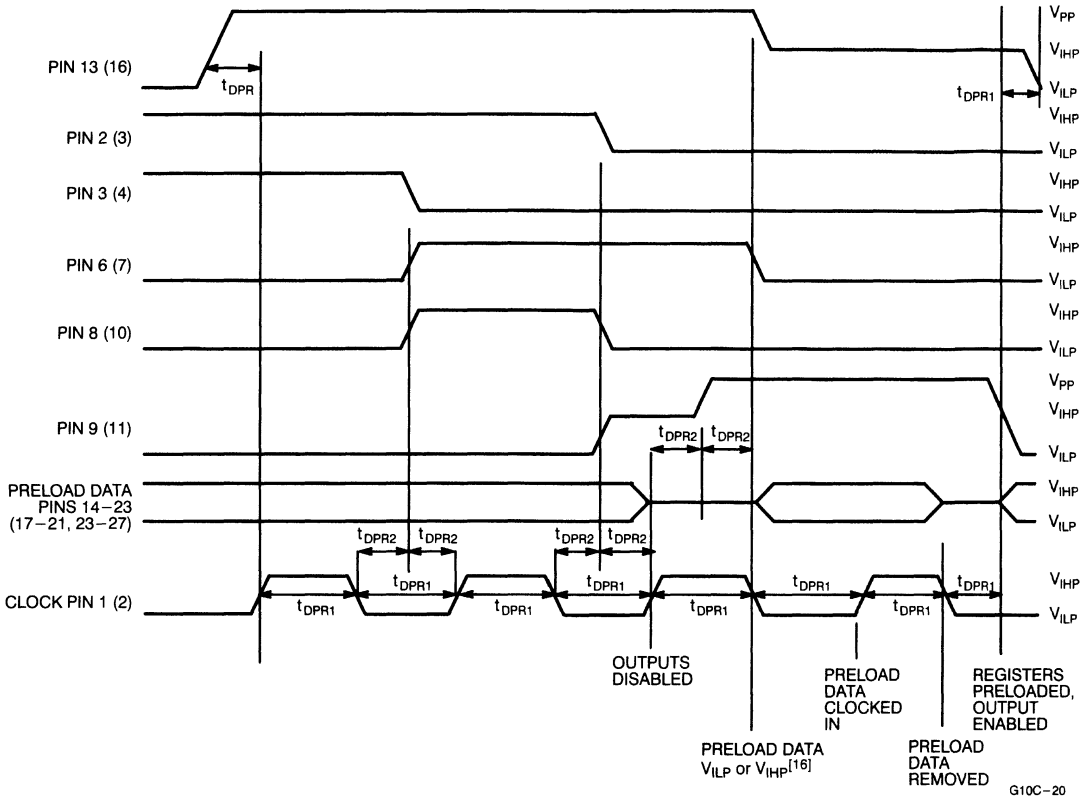
Switching Waveform



Power-Up Reset Waveform[14]



Preload Waveform[15]



Notes:

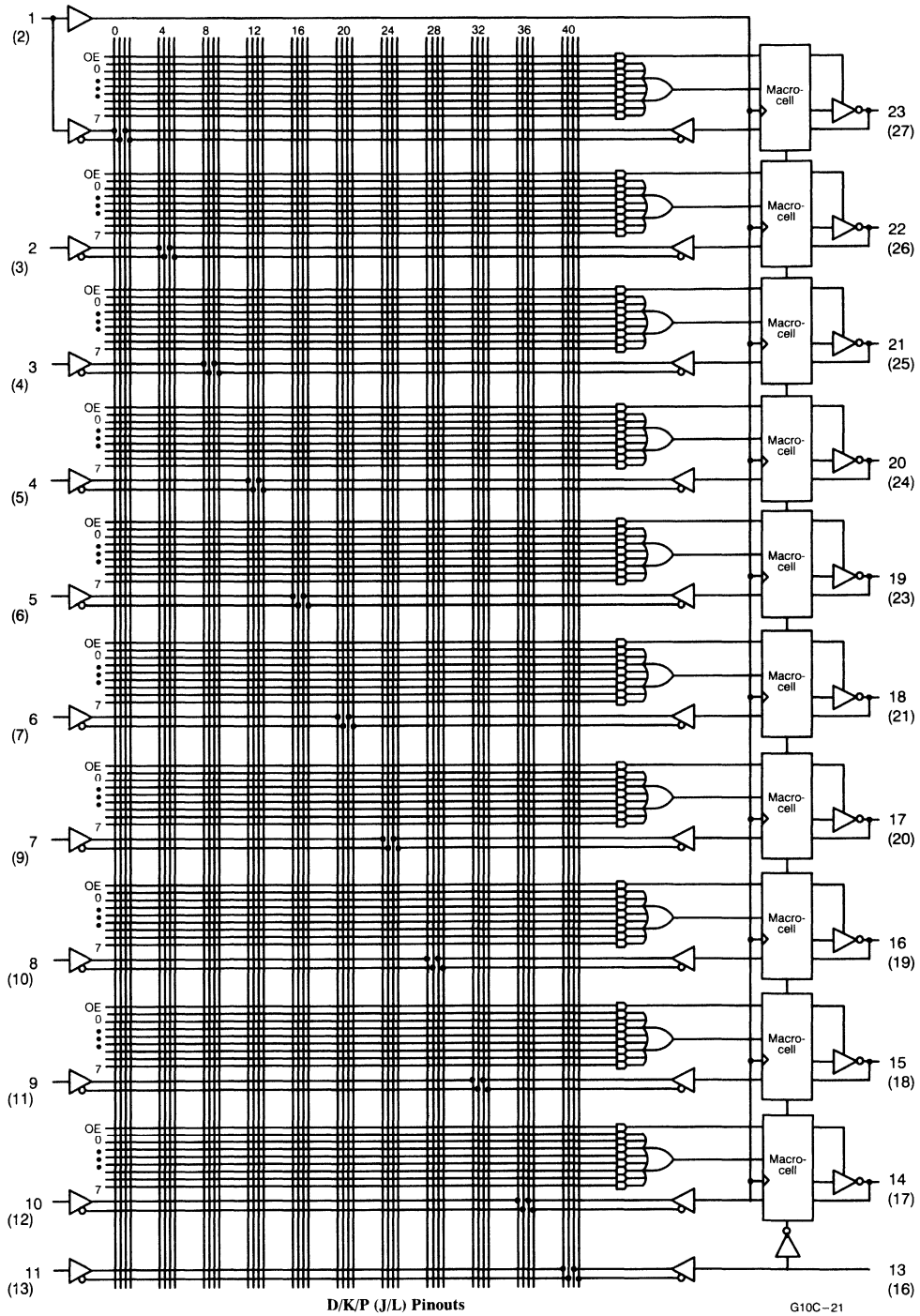
15. Pins 4 (5), 5 (6), 7 (9) at V_{ILP}; Pins 10 (12) and 11 (13) at V_{IHP}; V_{CC} (Pin 24 (1 and 28)) at V_{CCP}.
16. Pins 2–8 (3–7, 9, 10), 10 (12), 11 (13) can be set at V_{IHP} or V_{ILP} to insure asynchronous reset is not active.

D/K/P (J/L) Pinouts

Forced level on register pin during preload	Register Q output state after preload
V_{IHP}	HIGH
V_{ILP}	LOW

Name	Description	Min.	Max.	Unit
V_{PP}	Programming Voltage	9.25	9.75	V
t_{DPR1}	Delay for Preload	1		µs
t_{DPR2}	Delay for Preload	0.5		µs
V_{ILP}	Input LOW Voltage	0	0.4	V
V_{IHP}	Input HIGH Voltage	3	4.75	V
V_{CCP}	V_{CC} for Preload	4.75	5.25	V

Functional Logic Diagram for PLD20G10C



G10C–21

Ordering Information

I_{CC} (mA)	t_{PD} (ns)	f_{MAX} (MHz)	Ordering Code	Package Name	Package Type	Operating Range
190	7.5	105	PLD20G10C–7DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PLD20G10C–7JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PLD20G10C–7PC	P13	24-Lead (300-Mil) Molded DIP	
	10	90	PLD20G10C–10DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PLD20G10C–10JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PLD20G10C–10PC	P13	24-Lead (300-Mil) Molded DIP	
			PLD20G10C–10DMB	D14	24-Lead (300-Mil) CerDIP	Military
			PLD20G10C–10KMB	K73	24-Lead Rectangular Cerpack	
			PLD20G10C–10LMB	L64	28-Square Leadless Chip Carrier	
	12	71	PLD20G10C–12DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PLD20G10C–12JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PLD20G10C–12PC	P13	24-Lead (300-Mil) Molded DIP	
			PLD20G10C–12DMB	D14	24-Lead (300-Mil) CerDIP	Military
			PLD20G10C–12KMB	K73	24-Lead Rectangular Cerpack	
			PLD20G10C–12LMB	L64	28-Square Leadless Chip Carrier	
	15	57	PLD20G10C–15DMB	D14	24-Lead (300-Mil) CerDIP	Military
			PLD20G10C–15KMB	K73	24-Lead Rectangular Cerpack	
			PLD20G10C–15LMB	L64	28-Square Leadless Chip Carrier	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_S	7, 8, 9, 10, 11
t_H	7, 8, 9, 10, 11

Document #: 38–A–00027–A

PLDC20RA10

Reprogrammable Asynchronous CMOS Logic Device

Features

- **Advanced-user programmable macrocell**
- **CMOS EPROM technology for reprogrammability**
- **Up to 20 input terms**
- **10 programmable I/O macrocells**
- **Output macrocell programmable as combinatorial or asynchronous D-type registered output**
- **Product-term control of register clock, reset and set and output enable**
- **Register preload and power-up reset**
- **Four data product terms per output macrocell**
- **Fast**
  - **Commercial**
    t_{PD} = 15 ns
    t_{CO} = 15 ns
    t_{SU} = 7 ns
  - **Military/Industrial**
    t_{PD} = 20 ns
    t_{CO} = 20 ns
    t_{SU} = 10 ns
- **Low power**
  - **I_{CC} max = 80 mA (Commercial)**
  - **I_{CC} max = 85 mA (Military)**
- **High reliability**
  - **Proven EPROM technology**
  - **>2001V input protection**
  - **100% programming and functional testing**
- **Windowed DIP, windowed LCC, DIP, LCC, PLCC available**

Functional Description

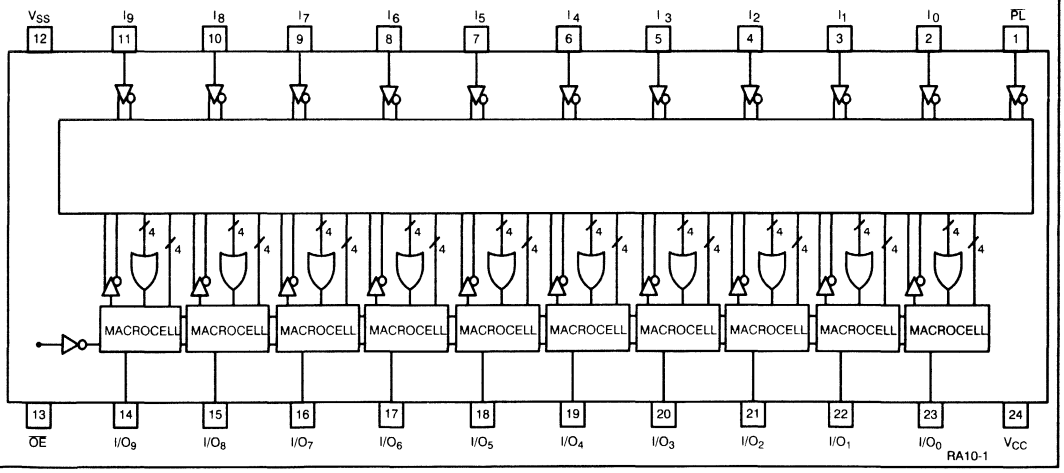
The Cypress PLDC20RA10 is a high-performance, second-generation programmable logic device employing a flexible macrocell structure that allows any individual output to be configured independently as a combinatorial output or as a fully asynchronous D-type registered output.

The Cypress PLDC20RA10 provides lower-power operation with superior speed performance than functionally equivalent bipolar devices through the use of high-performance 0.8-micron CMOS manufacturing technology.

The PLDC20RA10 is packaged in a 24 pin 300-mil molded DIP, a 300-mil windowed cerDIP, and a 28-lead square leadless chip carrier, providing up to 20 inputs and 10 outputs. When the windowed device is exposed to UV light, the 20RA10 is erased and can then be reprogrammed.

2

Logic Block Diagram

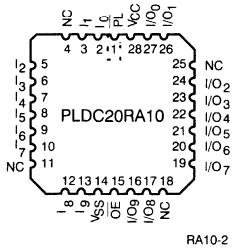


Selection Guide

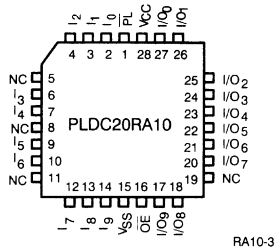
Generic Part Number	t_{PD} ns		t_{SU} ns		t_{CO} ns		I_{CC} ns	
	Com'l	Mil/Ind	Com'l	Mil/Ind	Com'l	Mil/Ind	Com'l	Mil/Ind
20RA10-15	15		7		15		80	
20RA10-20	20	20	10	10	20	20	80	85
20RA10-25		25		15		25		85
20RA10-35		35		20		35		85

Pin Configurations

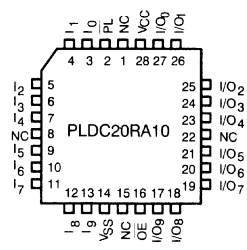
LCC
Top View



STD PLCC/HLCC
Top View



JEDEC PLCC/HLCC [1]
Top View



Macrocell Architecture

Figure 1 illustrates the architecture of the 20RA10 macrocell. The cell dedicates three product terms for fully asynchronous control of the register set, reset, and clock functions, as well as, one term for control of the output enable function.

The output enable product term output is ANDed with the input from pin 13 to allow either product term or hardwired external control of the output or a combination of control from both sources. If product-term-only control is selected, it is automatically chosen for all outputs since, for this case, the external output enable pin must be tied LOW. The active polarity of each output may be programmed independently for each output cell and is subsequently fixed. *Figure 2* illustrates the output enable options available.

When an I/O cell is configured as an output, combinatorial-only capability may be selected by forcing the set and reset product term outputs to be HIGH under all input conditions. This is achieved by programming all input term programming cells for these two product terms. *Figure 3* illustrates the available output configuration options.

An additional four uncommitted product terms are provided in each output macrocell as resources for creation of user-defined logic functions.

Programmable I/O

Because any of the ten I/O pins may be selected as an input, the device input configuration programmed by the user may vary from a total of nine programmable plus ten dedicated inputs (a total of nineteen inputs) and one output down to a ten-input, ten-output configuration with all ten programmable I/O cells configured as outputs. Each input pin available in a given configuration is available as an input to the four control product terms and four uncommitted product terms of each programmable I/O macrocell that has been configured as an output.

An I/O cell is programmed as an input by tying the output enable pin (pin 13) HIGH or by programming the output enable product term to provide a LOW, thereby disabling the output buffer, for all possible input combinations.

When utilizing the I/O macrocell as an output, the input path functions as a feedback path allowing the output signal to be fed back as an input to the product term array. When the output cell is configured as a registered output, this feedback path may be used to feed back the current output state to the device inputs to provide current state control of the next output state as required for state machine implementation.

Preload and Power-Up Reset

Functional testability of programmed devices is enhanced by inclusion of register preload capability, which allows the state of each register to be set by loading each register from an external source prior to exercising the device. Testing of complex state machine designs is simplified by the ability to load an arbitrary state without cycling through long test vector sequences to reach the desired state. Recovery from illegal states can be verified by loading illegal states and observing recovery. Preload of a particular register is accomplished by impressing the desired state on the register output pin and lowering the signal level on the preload control pin (pin1) to a logic LOW level. If the specified preload set-up, hold and pulse width minimums have been observed, the desired state is loaded into the register. To insure predictable system initialization, all registers are preset to a logic LOW state upon power-up, thereby setting the active LOW outputs to a logic HIGH.

Note:
1. The CG7C324 is the PLDC20RA10 packaged in the JEDEC-compatible 28-pin PLCC pinout. Pin fuction and pin order is identical for both PLCC pinouts. The principle differencd is in the location of the "no connect" (NC) pins.

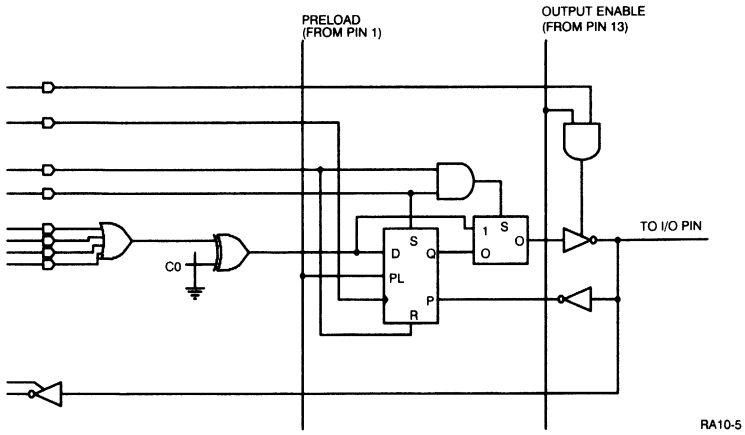


Figure 1. PLDC20RA10 Macrocell

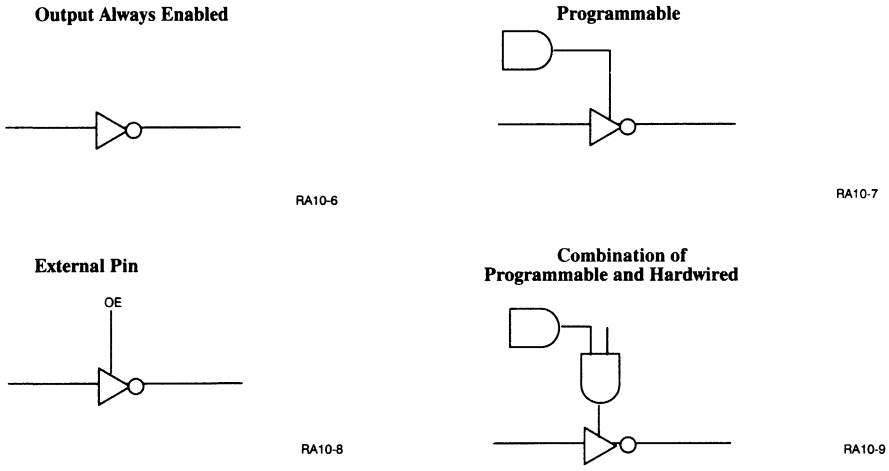
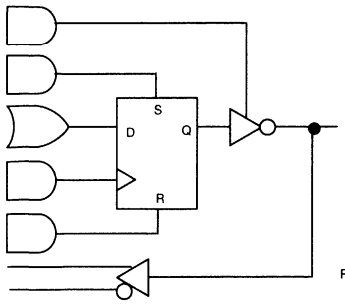


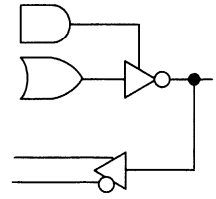
Figure 2. Four Possible Output Enable Alternatives for the PLDC20RA10

Registered/Active LOW



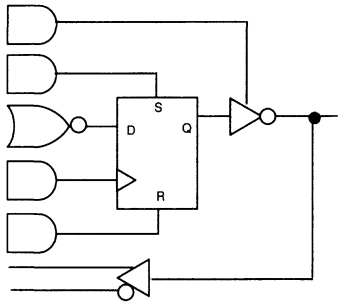
RA10-10

Combinatorial/Active LOW



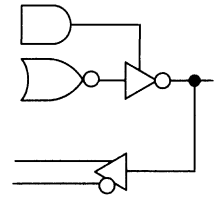
RA10-11

Registered/Active HIGH



RA10-12

Combinatorial/Active HIGH



RA10-13

Figure 3. Four Possible Macrocell Configurations for the PLDC20RA10

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0 V to + 7.0 V

Output Current into Outputs (LOW) ..... 16 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

DC Program Voltage 13.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military[2]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	Com'l	2.4		V
			I_{OH} = −2 mA	Mil/Ind			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8 mA			0.5	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[4]			2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[4]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{CC}$, V_{CC} = Max			−10	+10	μA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \leq V_{OUT} \leq V_{CC}$			−40	+40	μA
I_{SC}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = 0.5V[6]			−30	−90	mA
I_{CC1}	Standby Power Supply Current	V_{CC}= Max., V_{IN} = GND Outputs Open		Com'l		75	mA
				Mil/Ind		80	mA
I_{CC2}	Power Supply Current at Frequency[5]	V_{CC} = Max., Outputs Disabled (In High Z State) Device Operating af f_{MAX}		Com'l		80	mA
				Mil/Ind		85	mA

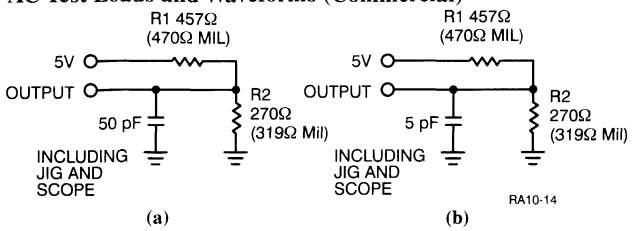
Capacitance[5]

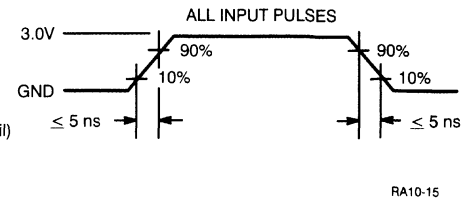
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz	10	pF

Notes:

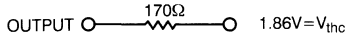
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. These are absolute values with respect to devicee ground and all overshoots due to system or tester noise are included.
5. Tested initially and after any design or process changes that may affect these parameters.
6. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

AC Test Loads and Waveforms (Commercial)

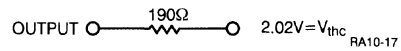


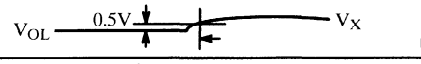
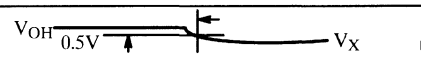
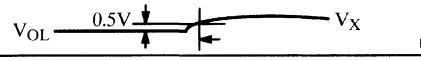
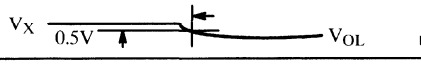


Equivalent to: THÉVENIN EQUIVALENT (Commercial)



Equivalent to: THÉVENIN EQUIVALENT (Military/Industrial)



Parameter	V_{th}	Output Waveform—Measurement Level
$t_{PXZ(-)}$	1.5V	 RA10-18
$t_{PXZ(+)}$	2.6V	 RA10-19
$t_{PZX(+)}$	V_{thc}	 RA10-20
$t_{PZX(-)}$	V_{thc}	 RA10-21
$t_{ER(-)}$	1.5V	 RA10-22
$t_{ER(+)}$	2.6V	 RA10-23
$t_{EA(+)}$	V_{thc}	 RA10-24
$t_{EA(-)}$	V_{thc}	 RA10-25

(c)

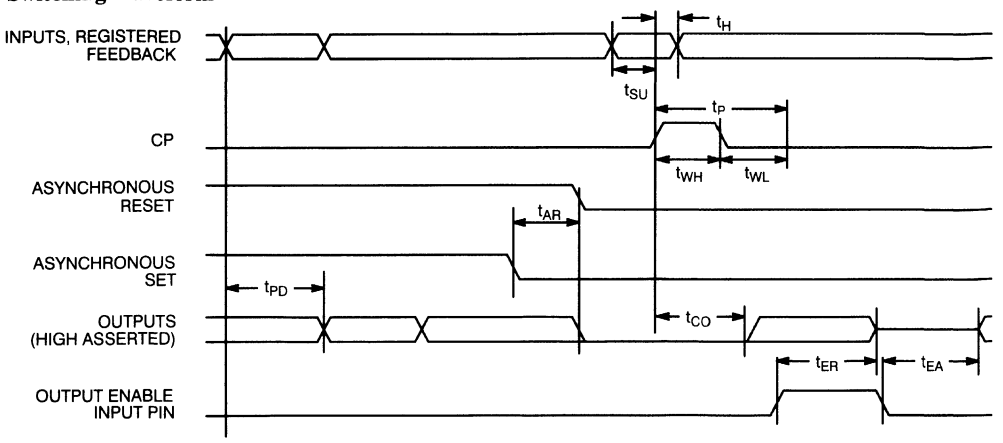
Switching Characteristics Over the Operating Range[3, 7, 8]

Parameter	Description	Commercial				Military/Industrial						Unit
		-15		-20		-20		-25		-35		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Non-Registered Output		15		20		20		25		35	ns
t_{EA}	Input to Output Enable		15		20		20		30		35	ns
t_{ER}	Input to Output Disable		15		20		20		30		35	ns
t_{PZX}	Pin 13 to Output Enable		12		15		15		20		25	ns
t_{PXZ}	Pin 13 to Output Disable		12		15		15		20		25	ns
t_{CO}	Clock to Output		15		20		20		25		35	ns
t_{SU}	Input or Feedback Set-Up Time	7		10		10		15		20		ns
t_H	Hold Time	3		5		3		5		5		ns
t_P	Clock Period ($t_{SU} + t_{CO}$)	22		30		30		40		55		ns
t_{WH}	Clock Width HIGH[5]	10		13		12		18		25		ns
t_{WL}	Clock Width LOW[5]	10		13		12		18		25		ns
f_{MAX}	Maximum Frequency ($1/t_P$)[5]	45.5		33.3		33.3		25.0		18.1		MHz
t_S	Input of Asynchronous Set to Registered Output		15		20		20		25		40	ns
t_R	Input of Asynchronous Reset to Registered Output		15		20		20		25		40	ns
t_{ARW}	Asynchronous Reset Width[5]	15		20		20		25		25		ns
t_{ASW}	Asynchronous Set Width[5]	15		20		20		25		25		ns
t_{AR}	Asynchronous Set/ Reset Recovery Time	10		12		12		15		20		ns
t_{WP}	Preload Pulse Width	15		15		15		15		15		ns
t_{SUP}	Preload Set-Up Time	15		15		15		15		15		ns
t_{HP}	Preload Hold Time	15		15		15		15		15		ns

Notes:

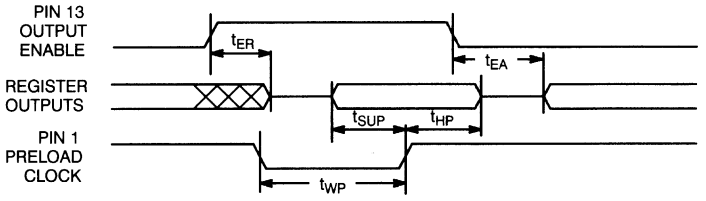
7. Part (a) of AC Test Loads was used for all parameters except t_{EA}, t_{ER}, t_{PZX} and t_{PXZ}, which use part (b).
8. The parameters t_{ER} and t_{PXZ} are measured as the delay from the input disable logic threshold transition to V_{OH} – 0.5 V for an enabled HIGH output or V_{OL} +0.5V for an enabled LOW output. Please see part (c) of AC Test Loads and Waveforms for waveforms and measurement reference levels.

Switching Waveform



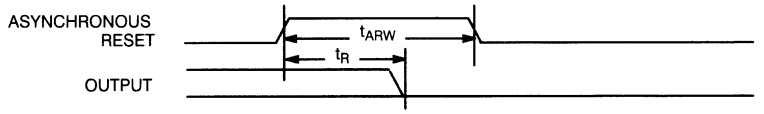
RA10-26

Preload Switching Waveform



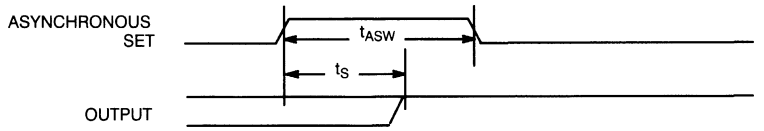
RA10-27

Asynchronous Reset



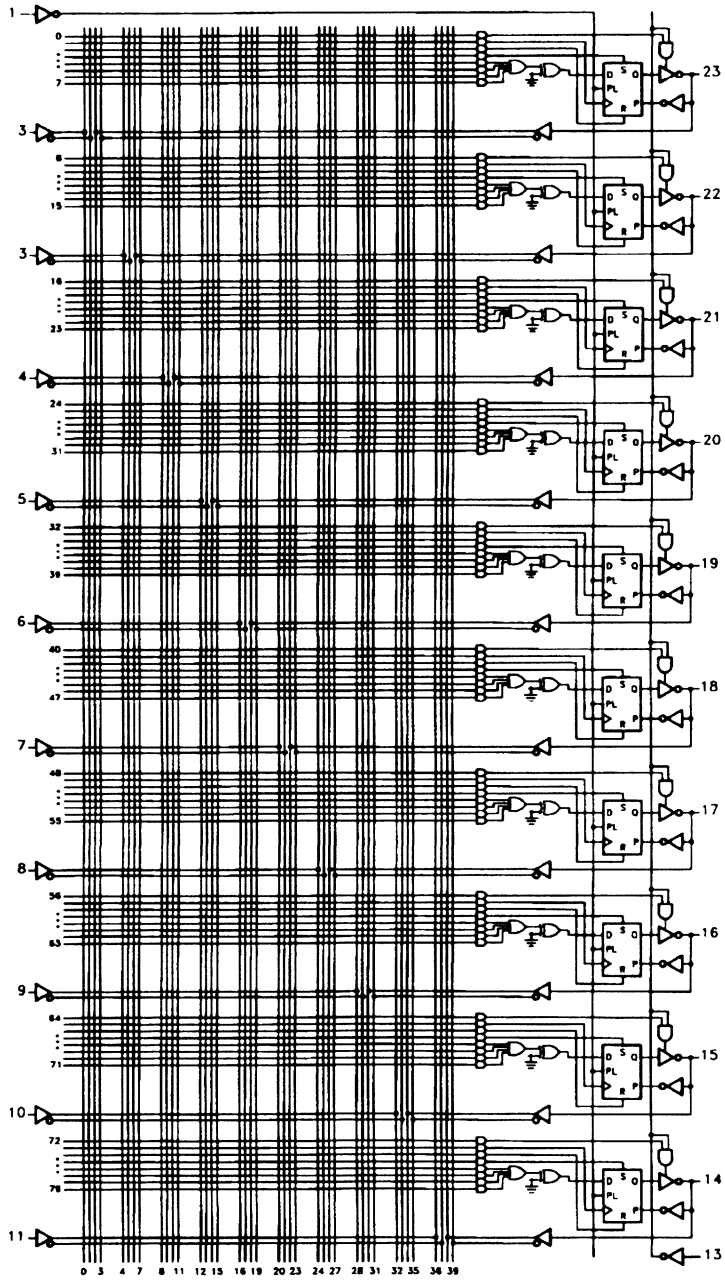
RA10-28

Asynchronous Set



RA10-29

Functional Logic Diagram



Ordering Information

I_{CC2}	t_{PD} (ns)	t_{SU} (ns)	t_{CO} (ns)	Ordering Code	Package Name	Package Type	Operating Range
80	15	7	15	PLDC20RA10-15HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
				PLDC20RA10-15JC	J64	28-Lead Plastic Leaded Chip Carrier	
				PLDC20RA10-15PC	P13	24-Lead (300-Mil) Molded DIP	
				PLDC20RA10-15WC	W14	24-Lead (300-Mil) Windowed CerDIP	
				CG7C324-A15HC	H64	28-Pin Windowed Leaded Chip Carrier	
				CG7C324-A15JC	J64	28-Lead Plastic Leaded Chip Carrier	
80	20	10	20	PLDC20RA10-20HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
				PLDC20RA10-20JC	J64	28-Lead Plastic Leaded Chip Carrier	
				PLDC20RA10-20PC	P13	24-Lead (300-Mil) Molded DIP	
				PLDC20RA10-20WC	W14	24-Lead (300-Mil) Windowed CerDIP	
				CG7C324-A20HC	H64	28-Pin Windowed Leaded Chip Carrier	
				CG7C324-A20JC	J64	28-Lead Plastic Leaded Chip Carrier	
85	20	10	20	PLDC20RA10-20DI	D14	24-Lead (300-Mil) CerDIP	Industrial
				PLDC20RA10-20JI	J64	28-Lead Plastic Leaded Chip Carrier	
				PLDC20RA10-20PI	P13	24-Lead (300-Mil) Molded DIP	
				PLDC20RA10-20WI	W14	24-Lead (300-Mil) Windowed CerDIP	
				PLDC20RA10-20DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PLDC20RA10-20HMB	H64	28-Pin Windowed Leaded Chip Carrier	
				PLDC20RA10-20LMB	L64	28-Square Leadless Chip Carrier	
				PLDC20RA10-20QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
				PLDC20RA10-20WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
85	25	15	25	PLDC20RA10-25DI	D14	24-Lead (300-Mil) CerDIP	Industrial
				PLDC20RA10-25JI	J64	28-Lead Plastic Leaded Chip Carrier	
				PLDC20RA10-25PI	P13	24-Lead (300-Mil) Molded DIP	
				PLDC20RA10-25WI	W14	24-Lead (300-Mil) Windowed CerDIP	
				PLDC20RA10-25DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PLDC20RA10-25HMB	H64	28-Pin Windowed Leaded Chip Carrier	
				PLDC20RA10-25LMB	L64	28-Square Leadless Chip Carrier	
				PLDC20RA10-25QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
				PLDC20RA10-25WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
85	35	20	35	PLDC20RA10-35DI	D14	24-Lead (300-Mil) CerDIP	Industrial
				PLDC20RA10-35JI	J64	28-Lead Plastic Leaded Chip Carrier	
				PLDC20RA10-35PI	P13	24-Lead (300-Mil) Molded DIP	
				PLDC20RA10-35WI	W14	24-Lead (300-Mil) Windowed CerDIP	
				PLDC20RA10-35DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PLDC20RA10-35HMB	H64	28-Pin Windowed Leaded Chip Carrier	
				PLDC20RA10-35LMB	L64	28-Square Leadless Chip Carrier	
				PLDC20RA10-35QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
				PLDC20RA10-35WMB	W14	24-Lead (300-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	9, 10, 11
t_{PZX}	9, 10, 11
t_{CO}	9, 10, 11
t_{SU}	9, 10, 11
t_{H}	9, 10, 11

Document #: 38–00073–E

This is an abbreviated datasheet. Contact a Cypress representative for complete specifications. For new designs, please refer to the PALC22V10D.

PALC22V10

Reprogrammable CMOS PAL® Device

Features

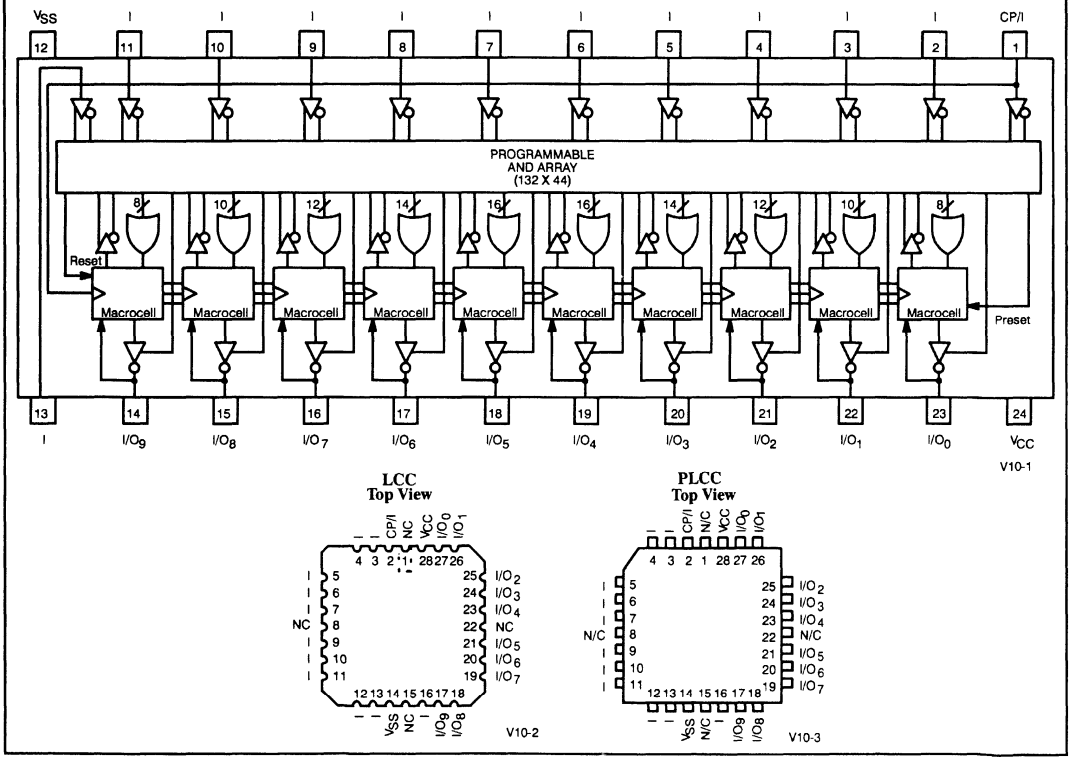
- **Advanced second-generation PAL architecture**
- **Low power**
  - **— 55 mA max. "L"**
  - **— 90 mA max. standard**
  - **— 120 mA max. military**
- **CMOS EPROM technology for reprogrammability**
- **Variable product terms**
  - **— 2 x (8 through 16) product terms**
- **User-programmable macrocell**
  - **— Output polarity control**
  - **— Individually selectable for registered or combinatorial operation**
- **20, 25, 35 ns commercial and industrial**
- **25, 30, 40 ns military**
- **Up to 22 input terms and 10 outputs**
- **High reliability**
  - **— Proven EPROM technology**
  - **— 100% programming and functional testing**
- **Windowed DIP, windowed LCC, DIP, LCC, and PLCC available**

Functional Description

The Cypress PALC22V10 is a CMOS second-generation programmable logic array device. It is implemented with the familiar sum-of-products (AND-OR) logic structure and a new concept, the "programmable macrocell."

The PALC22V10 is available in 24-pin 300-mil molded DIPs, 300-mil windowed cerDIPs, 28-lead square ceramic leadless chip carriers, 28-lead square plastic leaded chip carriers, and provides up to 22 inputs and 10 outputs. When the windowed cerDIP is exposed to UV light, the 22V10 is erased and can then be reprogrammed. The programmable macrocell provides the capability of defining the architecture of each output individually. Each of the 10 potential outputs may be specified as registered or combinatorial. Polarity of each output may also be individually selected, allowing complete flexibility of output configuration. Further configurability is provided through array-configurable output enable for each potential output. This feature allows the 10 outputs to be reconfigured as inputs on an individual basis, or alternately used as a combination I/O controlled by the programmable array.

Logic Block Diagram (PDIP/CDIP) and Pin Configurations



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Document #: 38-00020-H

This is an abbreviated datasheet. Contact a Cypress Representative for complete specifications. For new designs, please refer to the PALC22V10D.

PALC22V10B

Reprogrammable CMOS PAL® Device

Features

- **Advanced second-generation PAL architecture**
- **Low power**
  - **— 90 mA max. standard**
  - **— 100 mA max. military**
- **CMOS EPROM technology for reprogrammability**
- **Variable product terms**
  - **— 2 x (8 through 16) product terms**
- **User-programmable macrocell**
  - **— Output polarity control**
  - **— Individually selectable for registered or combinatorial operation**
  - **— "15" commercial and industrial**
    10 ns t_{CO}
    10 ns t_S
    15 ns t_{PD}
    50 MHz
  - **— "15" and "20" military**
    10/15 ns t_{CO}
    10/17 ns t_S
    15/20 ns t_{PD}
    50/31 MHz
- **Up to 22 input terms and 10 outputs**
- **Enhanced test features**
  - **— Phantom array**
  - **— Top test**
  - **— Bottom test**
  - **— Preload**
- **High reliability**
  - **— Proven EPROM technology**
  - **— 100% programming and functional testing**
- **Windowed DIP, windowed LCC, DIP, LCC, PLCC available**

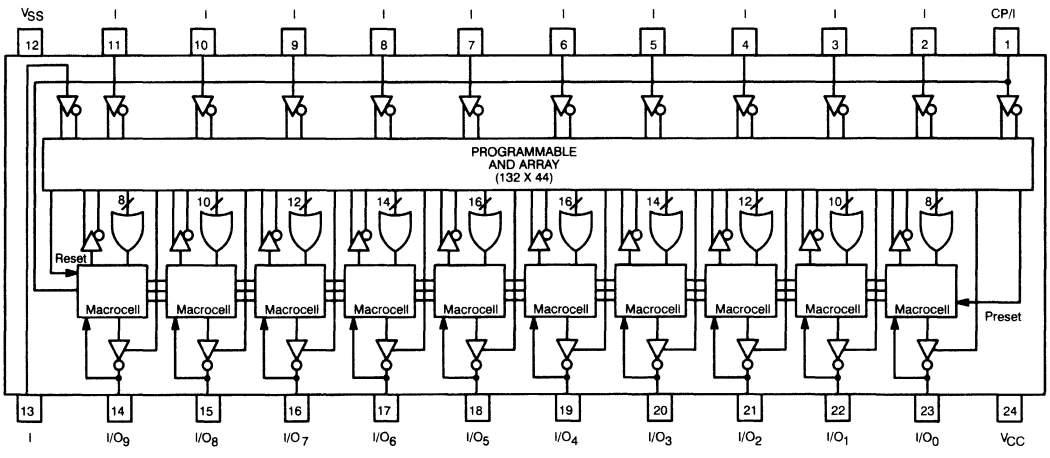
Functional Description

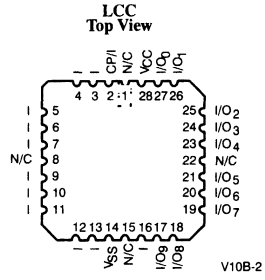
The Cypress PALC22V10B is a CMOS second-generation programmable logic array device. It is implemented with the familiar sum-of-products (AND-OR) logic structure and a new concept, the "Programmable Macrocell."

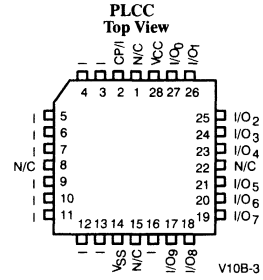
The PALC22V10B is executed in a 24-pin 300-mil molded DIP, a 300-mil windowed cerDIP, a 28-lead square ceramic leadless chip carrier, a 28-lead square plastic leaded chip carrier, and provides up to 22 inputs and 10 outputs. When the windowed cerDIP is exposed to UV light, the 22V10B is erased and can then be reprogrammed.

2

Logic Block Diagram (PDIP/CDIP) and Pin Configurations







PAL is a registered trademark of Advanced Micro Devices.

Document #: 38-00195-A

PAL22V10C
PAL22VP10C

Universal PAL® Device

Features

- **Ultra high speed supports today's and tomorrow's fastest microprocessors**
  - **— t_{PD} = 6 ns**
  - **— t_S = 3 ns**
  - **— f_{MAX} = 117 MHz**
- **Reduced ground bounce and undershoot**
- **PLCC and LCC packages with additional V_{CC} and V_{SS} pins for lowest ground bounce**
- **Up to 22 inputs and 10 outputs for more logic power**
- **Variable product terms**
  - **— 8 to 16 per output**
- **10 user-programmable output macrocells**
  - **— Output polarity control**
  - **— Registered or combinatorial operation**
  - **— 2 new feedback paths (PAL22VP10C)**
- **Synchronous PRESET, asynchronous RESET, and PRELOAD capability for flexible design and testability**
- **High reliability**
  - **— Proven Ti-W fuse technology**
  - **— AC and DC tested at the factory**
- **Security Fuse**

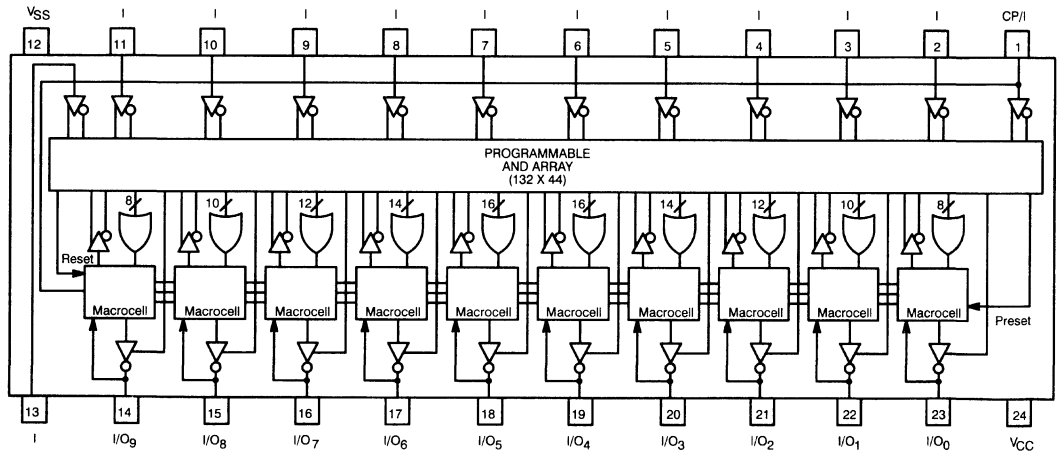
Functional Description

The Cypress PAL22V10C and PAL22VP10C are second-generation programmable array logic devices. Using BiCMOS process and Ti-W fuses, the PAL22V10C and PAL22VP10C use the familiar sum-of-products (AND-OR) logic structure and a new concept, the programmable macrocell.

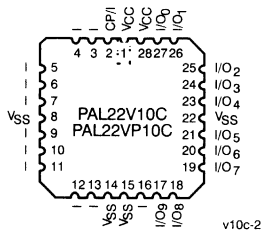
Both the PAL22V10C and PAL22VP10C provide 12 dedicated input pins and 10 I/O pins (see Logic Block Diagram). By selecting each I/O pin as either permanent or temporary input, up to 22 inputs can be achieved. Applications requiring up to 21 inputs and a single output, down to 12 inputs and 10 outputs can be realized. The output enable product term available on each I/O allows this selection.

The PAL22V10C and PAL22VP10C feature variable product term architecture, where 8 to 16 product terms are allocated to each output. This structure permits more applications to be implemented with

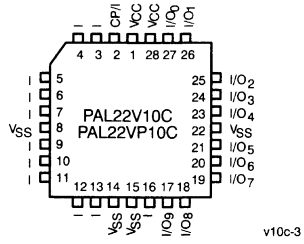
Logic Block Diagram and PDIP (P)/CDIP (D) and Pin Configurations



LCC (L)
Top View



PLCC (J)/CLCC (Y)
Top View



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Functional Description (continued)

these devices than with other PAL devices that have fixed number of product terms for each output.

Additional features include common synchronous preset and asynchronous reset product terms. They eliminate the need to use standard product terms for initialization functions

Both the PAL22V10C and PAL22VP10C automatically reset on power-up. In addition, the preload capability allows the output registers to be set to any desired state during testing.

A security fuse is provided on each of these two devices to prevent copying of the device fuse pattern.

With the programmable macrocells and variable product term architecture, the PAL22V10C and PAL22VP10C can implement logic functions in the 700 to 800 gate array complexity, with the inherent advantages of programmable logic.

Programmable Macrocell

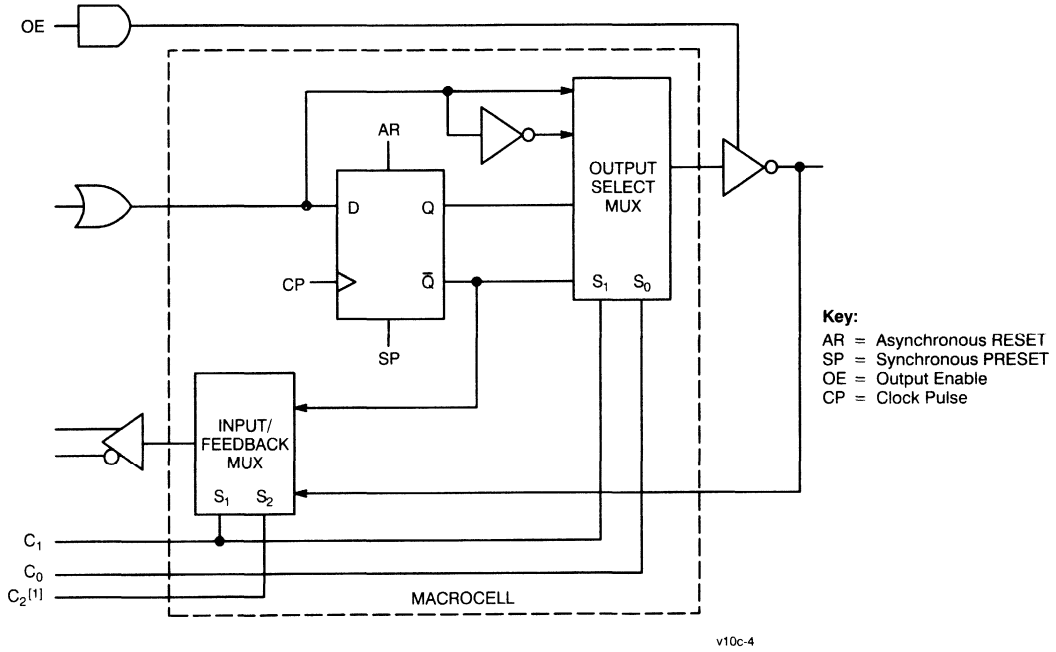
The PAL22V10C and PAL22VP10C each has 10 programmable output macrocells (see Macrocell figure). On the PAL22V10C two fuses (C_1 and C_0) can be programmed to configure output in one of four ways. Accordingly, each output can be registered or combinatorial with an active HIGH or active LOW polarity. The feedback to the array is also from this output (see *Figure 1*). An additional fuse (C_2) in the PAL22VP10C provides for two feedback paths (see *Figure 2*).

Programming

The PAL22V10C and PAL22VP10C can be programmed using the QuickPro II programmer available from Cypress Semiconductor and also with Data I/O, Logical Devices, STAG and other programmers. Please contact your local Cypress representative for further information.

2

Macrocell

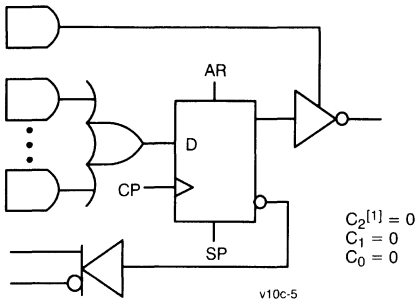


v10c-4

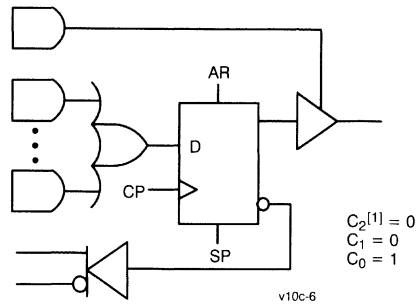
Output Macrocell Configuration

C_2[1]	C_1	C_0	Output Type	Polarity	Feedback
0	0	0	Registered	Active LOW	Registered
0	0	1	Registered	Active HIGH	Registered
X	1	0	Combinatorial	Active LOW	I/O
X	1	1	Combinatorial	Active HIGH	I/O
1	0	0	Registered	Active LOW	I/O[1]
1	0	1	Registered	Active HIGH	I/O[1]

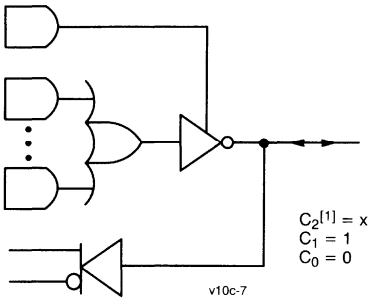
Note:
1. PAL22VP10C only.



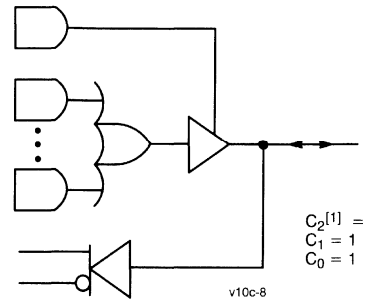
REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT

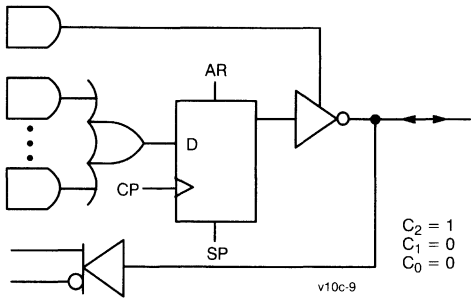


I/O FEEDBACK, COMBINATORIAL, ACTIVE-LOW OUTPUT

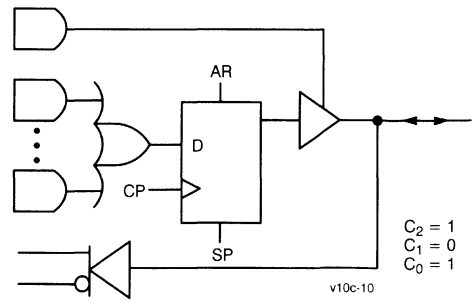


I/O FEEDBACK, COMBINATORIAL, ACTIVE-HIGH OUTPUT

Figure 1. PAL22V10C and PAL22VP10C Macrocell Configurations



I/O FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



I/O FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT

Figure 2. Additional Macrocell Configurations for the PAL22VP10C

Selection Guide

		22V10C-6 22VP10C-6	22V10C-7 22VP10C-7	22V10C-10 22VP10C-10	22V10C-12 22VP10C-12	22V10C-15 22VP10C-15
I_{CC} (mA)	Commercial	190	190	190	190	
	Military			190	190	190
t_{PD} (ns)	Commercial	6.0	7.5	10	12	
	Military			10	12	15
t_S (ns)	Commercial	3.0	3.0	3.6	4.5	
	Military			3.6	4.5	7.5
t_{CO} (ns)	Commercial	5.5	6.0	7.5	9.5	
	Military			7.5	9.5	10
f_{MAX} (MHz)	Commercial	117	111	90	71	
	Military			90	71	57

2

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to V_{CC}

DC Input Voltage ..... −0.5V to V_{CC}

DC Input Current ..... −30 mA to +5 mA (except during programming)

DC Program Voltage ..... 10.0 V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Military[2]	−55°C to +125°C	5V ± 5%

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	Com'l	2.4		V
			I_{OH} = −2 mA	Mil			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA	Com'l		0.5	V
			I_{OL} = 12 mA	Mil			
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs[3]			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs[3]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le 2.7V$, V_{CC} = Max.			−250	50	µA
I_I	Maximum Input Current	V_{IN} = V_{CC}, V_{CC} = Max.		Com'l		100	µA
				Mil		250	
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			−100	100	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[4]			−30	−120	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = GND, Outputs Open		Com'l		190	mA
				Mil		190	

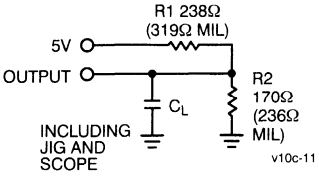
Capacitance[5]

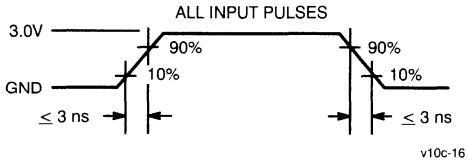
Parameter	Description	Max.	Unit
C_{IN}	Input Capacitance	8	pF
C_{OUT}	Output Capacitance	10	pF

Notes:

2. t_A is the "instant on" case temperature.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
5. Tested initially and after any design or process changes that may affect these parameters.

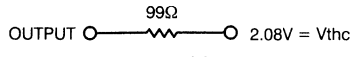
AC Test Loads and Waveforms





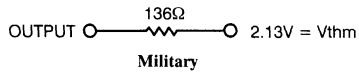
C_L[6]	Package
15 pF[7]	P/D
50 pF	J/K/L/Y

Equivalent to: THÉVENIN EQUIVALENT

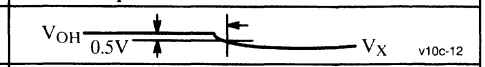
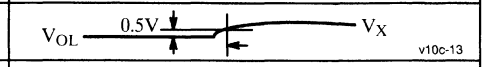
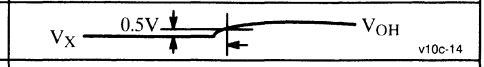
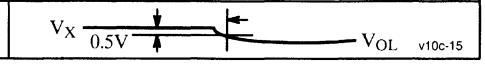


Commercial

Equivalent to: THÉVENIN EQUIVALENT



Military

Parameter	V_X	Output Waveform—Measurement Level
$t_{ER(-)}$	1.5V	 v10c-12
$t_{ER(+)}$	2.6V	 v10c-13
$t_{EA(+)}$	1.5V	 v10c-14
$t_{EA(-)}$	1.5V	 v10c-15

Notes:

6. C_L = 5 pF for t_{ER} measurement for all packages.
7. For high-capacitive load applications (C_L = 50 pF), use PAL22V10G/PAL22VP10G.

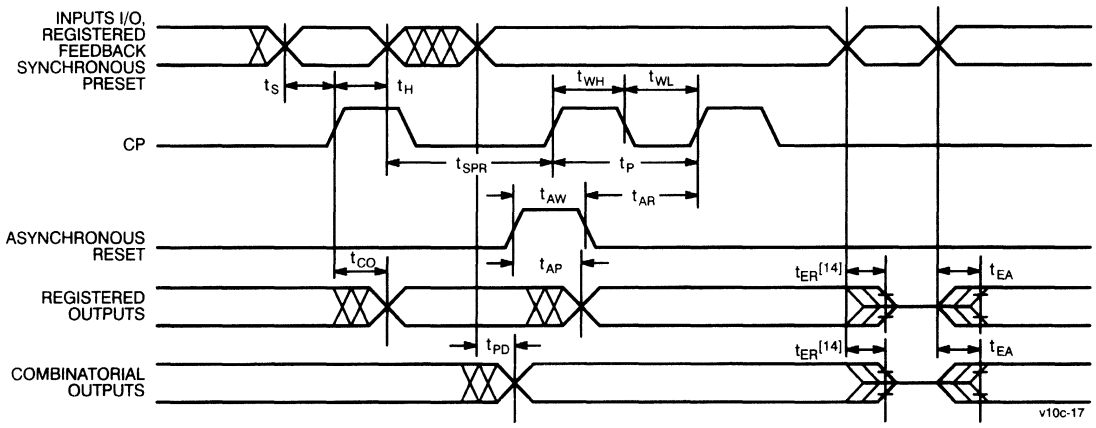
Switching Characteristics[8]

Parameter	Description	22V10C–6 22VP10C–6		22V10C–7 22VP10C–7		22V10C–10 22VP10C–10		22V10C–12 22VP10C–12		22V10C–15 22VP10C–15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[9]	1	6	2	7.5	2	10	2	12	2	15	ns
t_{EA}	Input to Output Enable Delay	1	6	2	7.5	2	10	2	12	2	15	ns
t_{ER}	Input to Output Disable Delay[10]	1	6	2	7.5	2	10	2	12	2	15	ns
t_{CO}	Clock to Output Delay[9]	1	5.5	1	6.0	1	7.5	1	9.5	1	10	ns
t_S	Input or Feedback Set-Up Time	3		3		3.6		4.5		7.5		ns
t_H	Input Hold Time	0		0		0		0		0		ns
t_P	External Clock Period (t_{CO} + t_S)	8.5		9		11.1		14		17.5		ns
t_{WH}	Clock Width HIGH[5]	3		3		3		3		6		ns
t_{WL}	Clock Width LOW[5]	3		3		3		3		6		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[11]	117		111		90		71		57		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[5, 12]	166		166		166		166		83		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[13]	142		133		100		83		66		MHz
t_{CF}	Register Clock to Feedback Input[14]		4		4.5		6.4		7.5		7.5	ns
t_{AW}	Asynchronous Reset Width	7.5		8.5		10		12		15		ns
t_{AR}	Asynchronous Reset Recovery Time	4		5		6		7		10		ns

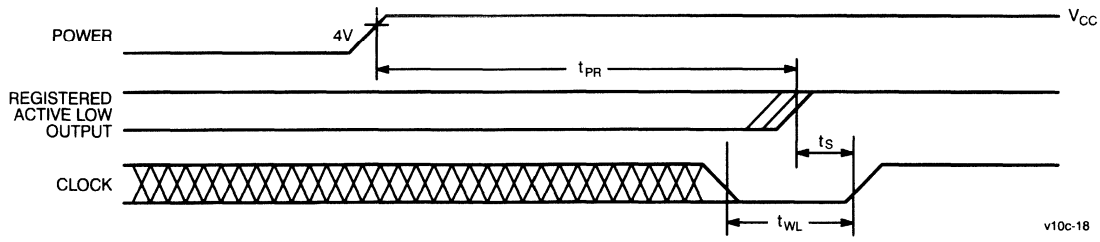
Switching Characteristics[8]

Parameter	Description	22V10C–6 22VP10C–6		22V10C–7 22VP10C–7		22V10C–10 22VP10C–10		22V10C–12 22VP10C–12		22V10C–15 22VP10C–15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AP}	Asynchronous Reset to Registered Output Delay	2	11	2	12	2	12	2	14	2	20	ns
t_{SPR}	Synchronous Preset Recovery Time	4		5		6		7		10		ns
t_{PR}	Power-Up Reset Time[15]	1		1		1		1		1		µs

Switching Waveform



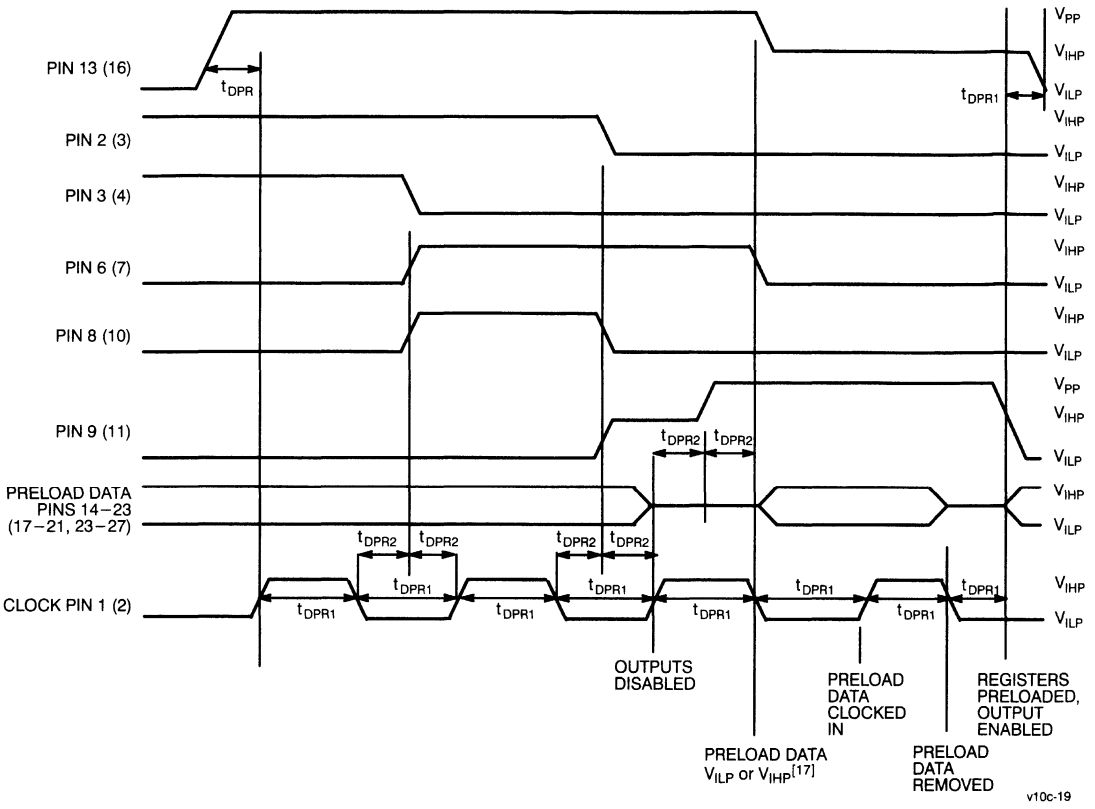
Power-Up Reset Waveform[15]



Notes:

8. AC test load used for all parameters except where noted.
9. This specification is guaranteed for all device outputs changing state in a given access cycle.
10. This parameter is measured as the time after output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below V_{OH} min. or a previous LOW level has risen to 0.5 volts above V_{OL} max.
11. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
12. This specification indicates the guaranteed maximum frequency at which an individual output register can be cycled.
13. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feedback can operate. This parameter is tested periodically by sampling production product.
14. This parameter is calculated from the clock period at f_{MAX} internal (f_{MAX3}) as measured (see Note 13) minus t_S.
15. The registers in the PAL22V10C/PAL22VP10C have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to a logic LOW state. The output state will depend on the polarity of the output buffer. This feature is useful in establishing state machine initialization. To insure proper operation, the rise in V_{CC} must be monotonic and the timing constraints depicted in power-up reset waveforms must be satisfied.

Preload Waveform[16]



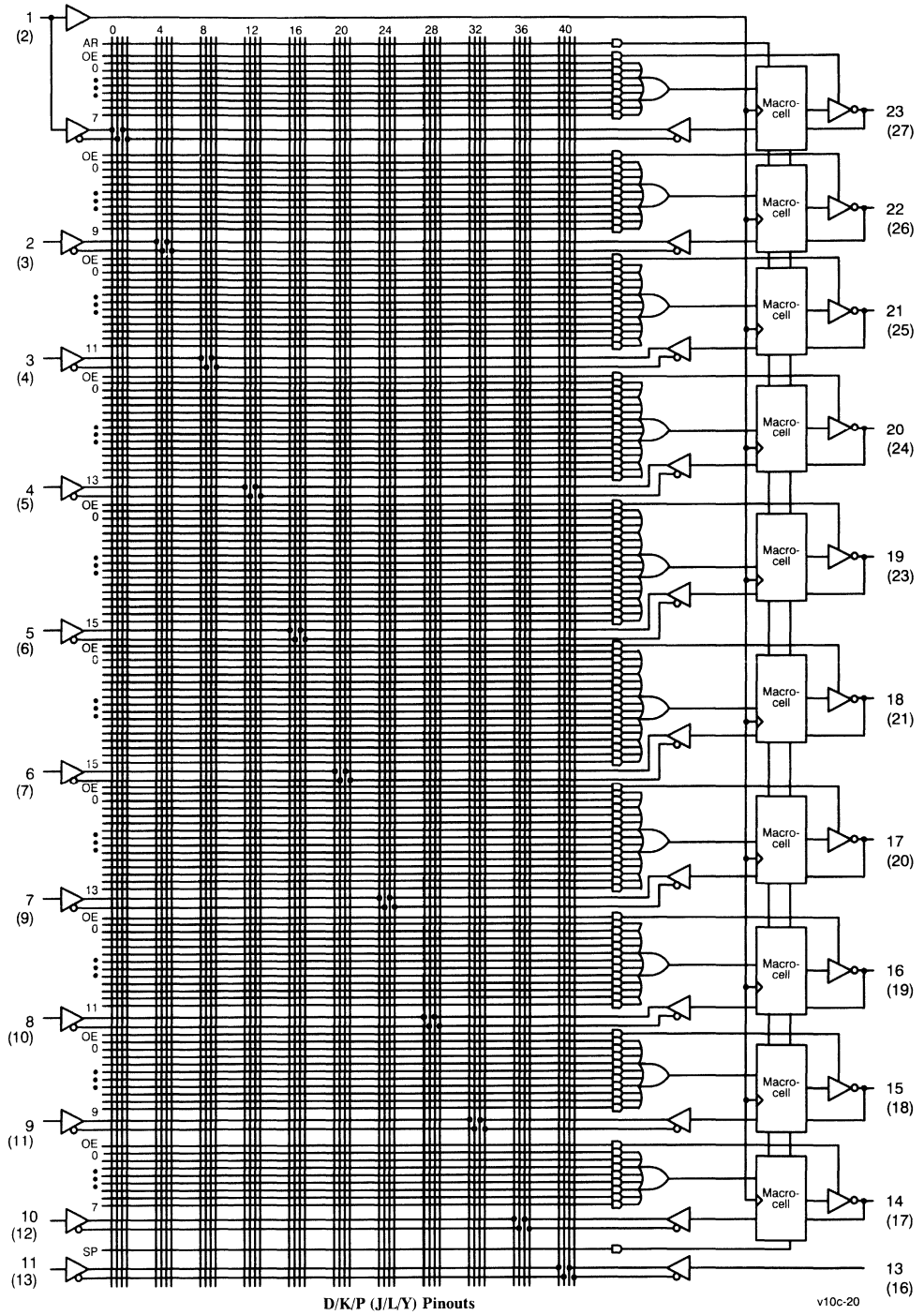
D/K/P (J/L/Y) Pinouts

Forced Level on Register Pin During Preload	Register Q Output State After Preload
V_{IHP}	HIGH
V_{ILP}	LOW

Name	Description	Min.	Max.	Unit
V_{PP}	Programming Voltage	9.25	9.75	V
t_{DPR1}	Delay for Preload	1		µs
t_{DPR2}	Delay for Preload	0.5		µs
V_{ILP}	Input LOW Voltage	0	0.4	V
V_{IHP}	Input HIGH Voltage	3	4.75	V
V_{CCP}	V_{CC} for Preload	4.75	5.25	V

Notes: (The numbers in parenthesis are for the J, L, and Y pins).
16. Pins 4 (5), 5 (6), 7 (9) at V_{ILP}; Pins 10 (12) and 11 (13) at V_{IHP}; V_{CC} (Pin 24 (1 and 28)) at V_{CCP}.
17. Pins 2–8 (3–7, 9, 10), 10 (12), 11 (13) can be set at V_{IHP} or V_{ILP} to insure asynchronous reset is not active.

Functional Logic Diagram for PAL22V10C/PAL22VP10C

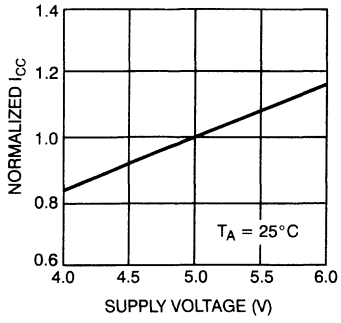


D/K/P (J/L/Y) Pinouts

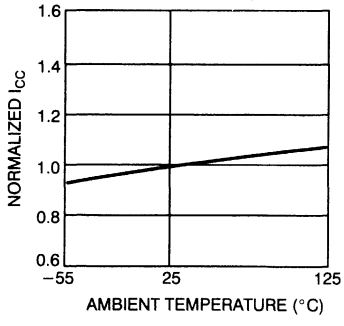
v10c-20

Typical DC and AC Characteristics

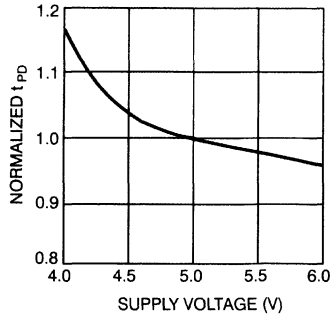
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



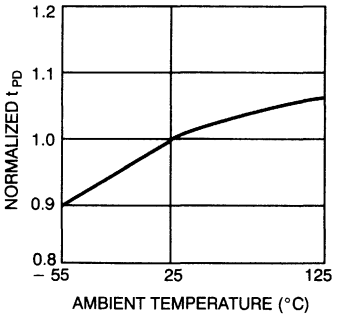
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



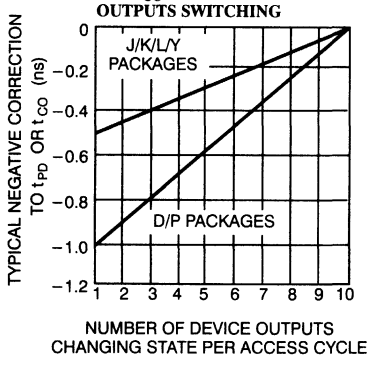
NORMALIZED PROPAGATION DELAY vs. SUPPLY VOLTAGE



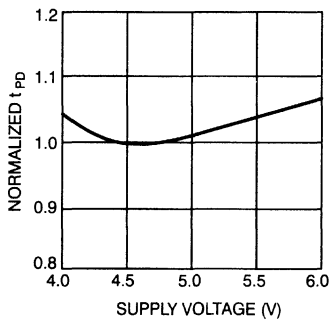
NORMALIZED PROPAGATION DELAY vs. TEMPERATURE



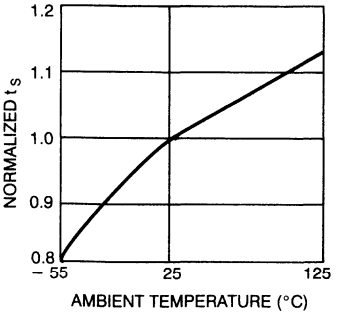
TYPICAL CORRECTION TO t_{PD} AND t_{CO} vs. NUMBER OF OUTPUTS SWITCHING



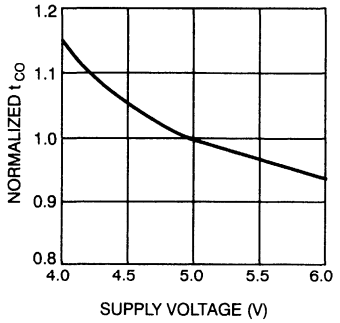
NORMALIZED SET-UP TIME vs. SUPPLY VOLTAGE



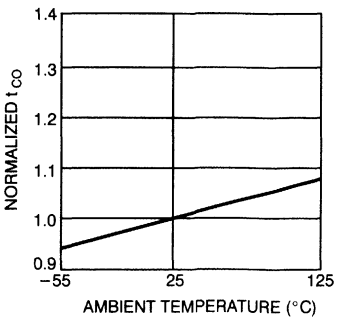
NORMALIZED SET-UP TIME vs. TEMPERATURE



NORMALIZED CLOCK TO OUTPUT TIME vs. SUPPLY VOLTAGE

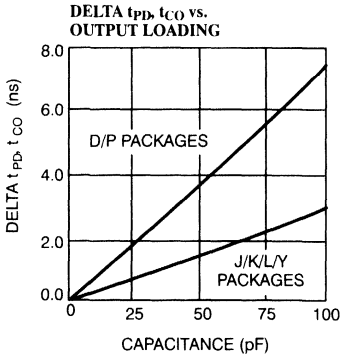


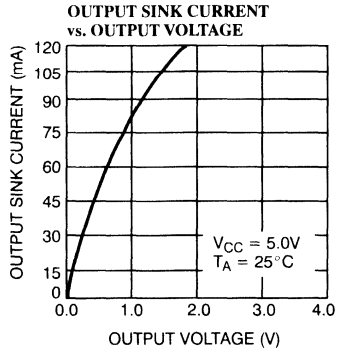
NORMALIZED CLOCK TO OUTPUT TIME vs. TEMPERATURE

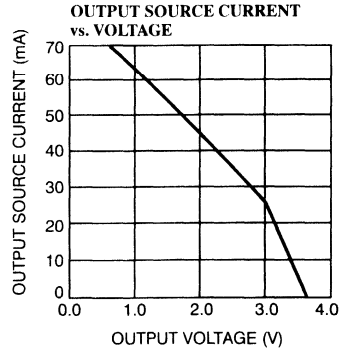


v10c-21

Typical DC and AC Characteristics (continued)







v10c-22

Ordering Information

I_{CC} (mA)	t_{PD} (ns)	f_{MAX} (MHz)	Ordering Code	Package Name	Package Type	Operating Range
190	6	117	PAL22V10C–6JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	7.5	111	PAL22V10C–7DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PAL22V10C–7JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22V10C–7PC	P13	24-Lead (300-Mil) Molded DIP	
			PAL22V10C–7YC	Y64	28-Pin Ceramic Leaded Carrier	
	10	90	PAL22V10C–10DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PAL22V10C–10JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22V10C–10PC	P13	24-Lead (300-Mil) Molded DIP	
			PAL22V10C–10YC	Y64	28-Pin Ceramic Leaded Carrier	
			PAL22V10CM–10DMB	D14	24-Lead (300-Mil) CerDIP	Military
			PAL22V10CM–10KMB	K73	24-Lead Rectangular Cerpack	
			PAL22V10CM–10LMB	L64	28-Square Leadless Chip Carrier	
			PAL22V10CM–10YMB	Y64	28-Pin Ceramic Leaded Carrier	
	12	71	PAL22V10C–12DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PAL22V10C–12JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22V10C–12PC	P13	24-Lead (300-Mil) Molded DIP	
			PAL22V10C–12YC	Y64	28-Pin Ceramic Leaded Carrier	
			PAL22V10CM–12DMB	D14	24-Lead (300-Mil) CerDIP	Military
			PAL22V10CM–12KMB	K73	24-Lead Rectangular Cerpack	
			PAL22V10CM–12LMB	L64	28-Square Leadless Chip Carrier	
			PAL22V10CM–12YMB	Y64	28-Pin Ceramic Leaded Carrier	
	15	57	PAL22V10CM–15DMB	D14	24-Lead (300-Mil) CerDIP	Military
			PAL22V10CM–15KMB	K73	24-Lead Rectangular Cerpack	
			PAL22V10CM–15LMB	L64	28-Square Leadless Chip Carrier	
			PAL22V10CM–15YMB	Y64	28-Pin Ceramic Leaded Carrier	

Ordering Information (continued)

I_{CC} (mA)	t_{PD} (ns)	f_{MAX} (MHz)	Ordering Code	Package Type		Operating Range
190	6	117	PAL22VP10C–6JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	7.5	111	PAL22VP10C–7DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PAL22VP10C–7JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22VP10C–7PC	P13	24-Lead (300-Mil) Molded DIP	
			PAL22VP10C–7YC	Y64	28-Pin Ceramic Leaded Carrier	
	10	90	PAL22VP10C–10DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PAL22VP10C–10JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22VP10C–10PC	P13	24-Lead (300-Mil) Molded DIP	
			PAL22VP10C–10YC	Y64	28-Pin Ceramic Leaded Carrier	
			PAL22VP10CM–10DMB	D14	24-Lead (300-Mil) CerDIP	Military
			PAL22VP10CM–10KMB	K73	24-Lead Rectangular Cerpack	
			PAL22VP10CM–10LMB	L64	28-Square Leadless Chip Carrier	
			PAL22VP10CM–10YMB	Y64	28-Pin Ceramic Leaded Carrier	
	12	71	PAL22VP10C–12DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PAL22VP10C–12JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22VP10C–12PC	P13	24-Lead (300-Mil) Molded DIP	
			PAL22VP10C–12YC	Y64	28-Pin Ceramic Leaded Carrier	
			PAL22VP10CM–12DMB	D14	24-Lead (300-Mil) CerDIP	Military
			PAL22VP10CM–12KMB	K73	24-Lead Rectangular Cerpack	
			PAL22VP10CM–12LMB	L64	28-Square Leadless Chip Carrier	
			PAL22VP10CM–12YMB	Y64	28-Pin Ceramic Leaded Carrier	
	15	57	PAL22VP10CM–15DMB	D14	24-Lead (300-Mil) CerDIP	Military
			PAL22VP10CM–15KMB	K73	24-Lead Rectangular Cerpack	
			PAL22VP10CM–15LMB	L64	28-Square Leadless Chip Carrier	
			PAL22VP10CM–15YMB	Y64	28-Pin Ceramic Leaded Carrier	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristerics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{PD}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_S	7, 8, 9, 10, 11
t_H	7, 8, 9, 10, 11

Document #: 38–A–00020–D

This is an abbreviated datasheet. Contact a Cypress representative for complete specifications. For new designs, please refer to the PALC22V10D or PAL22V10G.

PAL22V10CF
PAL22VP10CF

Universal PAL® Device

Features

- **Ultra high speed supports today's and tomorrow's fastest microprocessors**
  - **— t_{PD} = 7.5 ns**
  - **— t_S = 3 ns**
  - **— f_{MAX} = 100 MHz**
  - **— Drives 50-pF load (C_L)**
- **"No Connect" PLCC pinout**
- **Up to 22 inputs and 10 outputs for more logic power**
- **Variable product terms**
  - **— 8 to 16 per output**
- **10 user-programmable output macrocells**
  - **— Output polarity control**
  - **— Registered or combinatorial operation**
  - **— 2 new feedback paths (PAL22VP10CF)**
- **Synchronous PRESET, asynchronous RESET, and PRELOAD capability for flexible design and testability**
- **High reliability**
  - **— Proven Ti-W fuse technology**
  - **— AC and DC tested at the factory**
- **Security Fuse**

Functional Description

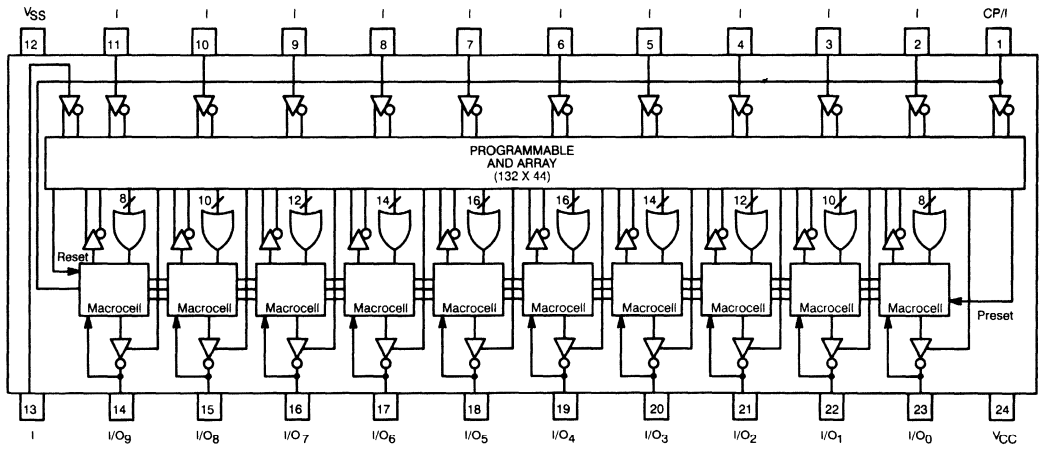
The Cypress PAL22V10CF and PAL22VP10CF are second-generation programmable array logic devices. Using BiCMOS process and Ti-W fuses, the PAL22V10CF and PAL22VP10CF use the familiar sum-of-products (AND-OR) logic structure and a new concept, the programmable macrocell.

Both the PAL22V10CF and PAL22VP10CF provide 12 dedicated input pins and 10 I/O pins (see Logic Block Diagram). By selecting each I/O pin as either permanent or temporary input, up to 22 inputs can be achieved. Applications requiring up to 21 inputs and a single output, down to 12 inputs and 10 outputs can be realized. The output enable product term available on each I/O allows this selection.

The PAL22V10CF and PAL22VP10CF feature variable product-term architecture, where 8 to 16 product terms are allocated to each output. This structure permits more applications to be implemented with these devices than with other PAL devices that have fixed number of product terms for each output.

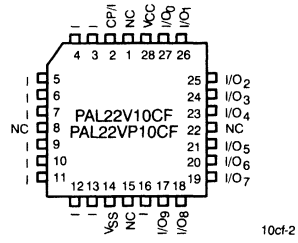
2

Logic Block Diagram and PDIP (P)/CDIP (D) Pin Configuration



Pin Configuration

PLCC (J)
Top View



PAL is a registered trademark of Advanced Micro Devices.

Document #: 38-A-00047

PALC22V10D

Flash Erasable, Reprogrammable CMOS PAL® Device

Features

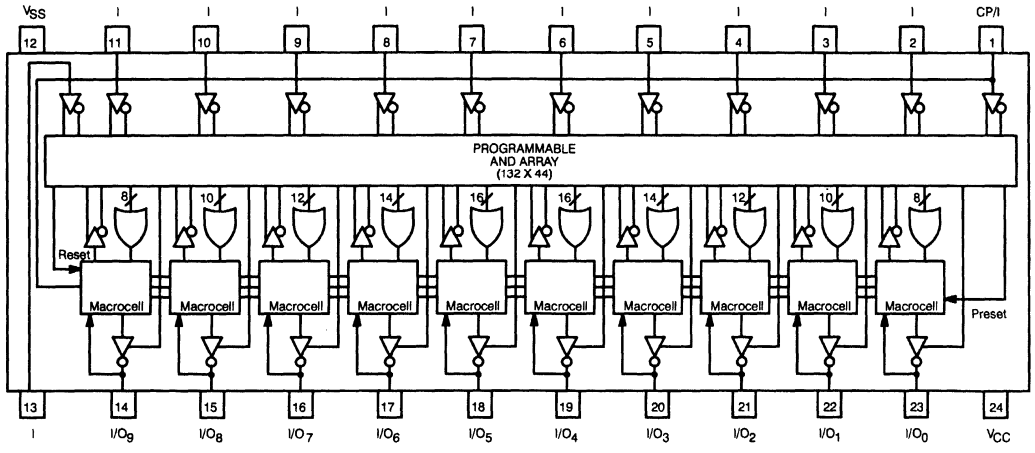
- **Advanced second-generation PAL architecture**
- **Low power**
  - **— 90 mA max. commercial (10 ns)**
  - **— 130 mA max. commercial (7.5 ns)**
- **CMOS Flash EPROM technology for electrical erasability and reprogrammability**
- **Variable product terms**
  - **— 2 x (8 through 16) product terms**
- **User-programmable macrocell**
  - **— Output polarity control**
  - **— Individually selectable for registered or combinatorial operation**
- **Up to 22 input terms and 10 outputs**
- **DIP, LCC, and PLCC available**
  - **— 7.5 ns commercial version**
    - **5 ns t_{CO}**
    - **5 ns t_S**
    - **7.5 ns t_{PD}**
    - **133-MHz state machine**
  - **— 10 ns military and industrial versions**
    - **6 ns t_{CO}**
    - **6 ns t_S**
    - **10 ns t_{PD}**
    - **110-MHz state machine**
  - **— 15-ns commercial and military versions**
  - **— 25-ns commercial and military versions**
- **High reliability**
  - **— Proven Flash EPROM technology**
  - **— 100% programming and functional testing**

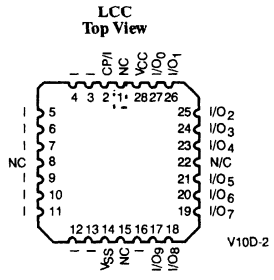
Functional Description

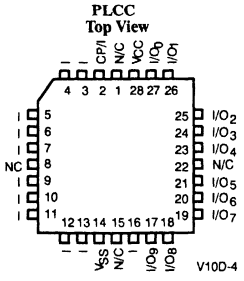
The Cypress PALC22V10D is a CMOS Flash Erasable second-generation programmable array logic device. It is implemented with the familiar sum-of-products (AND-OR) logic structure and the programmable macrocell.

The PALC22V10D is executed in a 24-pin 300-mil molded DIP, a 300-mil cerDIP, a 28-lead square ceramic leadless chip carrier, a 28-lead square plastic leaded chip carrier, and provides up to 22 inputs and 10 outputs. The 22V10D can be electrically

Logic Block Diagram (PDIP/CDIP) and Pin Configurations







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Functional Description (continued)

erased and reprogrammed. The programmable macrocell provides the capability of defining the architecture of each output individually. Each of the 10 potential outputs may be specified as "registered" or "combinatorial." Polarity of each output may also be individually selected, allowing complete flexibility of output configuration. Further configurability is provided through "array" configurable "output enable" for each potential output. This feature allows the 10 outputs to be reconfigured as inputs on an individual basis, or alternately used as a combination I/O controlled by the programmable array.

PALC22V10D features a variable product term architecture. There are 5 pairs of product term sums beginning at 8 product terms per output and incrementing by 2 to 16 product terms per output. By providing this variable structure, the PALC22V10D is optimized to the configurations found in a majority of applications without creating devices that burden the product term structures with unusable product terms and lower performance.

Additional features of the Cypress PALC22V10D include a synchronous preset and an asynchronous reset product term. These product terms are common to all macrocells, eliminating the need to dedicate standard product terms for initialization functions. The device automatically resets upon power-up.

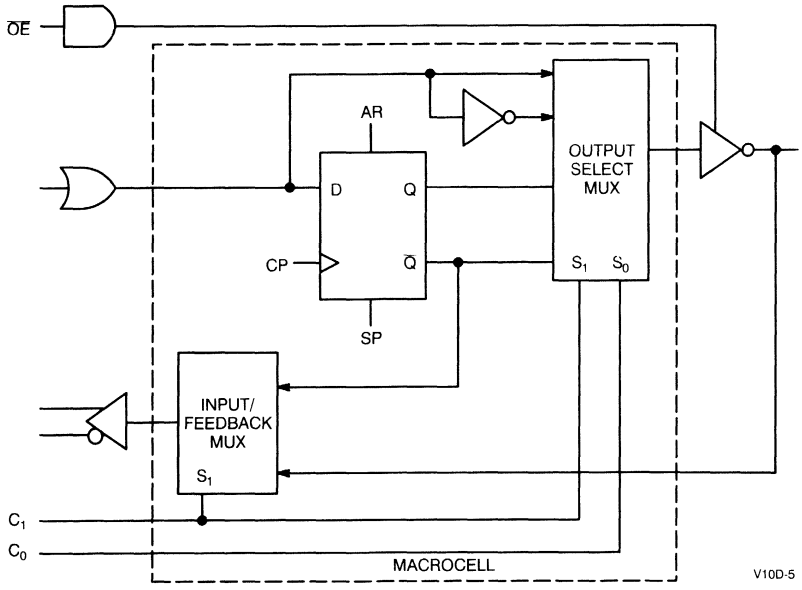
The PALC22V10D, featuring programmable macrocells and variable product terms, provides a device with the flexibility to implement logic functions in the 500- to 800-gate-array complexity. Since each of the 10 output pins may be individually configured as inputs on a temporary or permanent basis, functions requiring up to 21 inputs and only a single output and down to 12 inputs and 10 outputs are possible. The 10 potential outputs are enabled using product terms. Any output pin may be permanently selected as an output or arbitrarily enabled as an output and an input through the selective use of individual product terms associated with each output. Each of these outputs is achieved through an individual programmable macrocell. These macrocells are programmable to provide a combinatorial or registered inverting or non-inverting output. In a registered mode of operation, the output of the register is fed back into the array, providing current status information to the array. This information is available for establishing the next result in applications such as control state machines. In a combinatorial configuration, the combinatorial output or, if the output is disabled, the signal present on the I/O pin is made available to the array. The flexibility provided by both programmable product term control of the outputs and variable product terms allows a significant gain in functional density through the use of programmable logic.

Along with this increase in functional density, the Cypress PALC22V10D provides lower-power operation through the use of CMOS technology, and increased testability with Flash reprogrammability.

Configuration Table

Registered/Combinatorial		
C_1	C_0	Configuration
0	0	Registered/Active LOW
0	1	Registered/Active HIGH
1	0	Combinatorial/Active LOW
1	1	Combinatorial/Active HIGH

Macrocell



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 16 mA

DC Programming Voltage 12.5V

Latch-Up Current ..... >200 mA

Static Discharge Voltage (per MIL−STD−883, Method 3015) ..... >2001V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ±5%
Military[1]	−55°C to +125°C	5V ±10%
Industrial	−40°C to +85°C	5V ±10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	Com'l	2.4		V
			I_{OH} = −2 mA	Mil/Ind			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA	Com'l		0.5	V
			I_{OL} = 12 mA	Mil/Ind			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[3]			2.0		V
V_{IL}[4]	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[3]			−0.5	0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$, V_{CC} = Max.			−10	10	μA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			−40	40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[5, 6]			−30	−90	mA
I_{CC1}	Standby Power Supply Current	V_{CC} = Max., V_{IN} = GND, Outputs Open in Unprogrammed Device	10, 15, 25 ns	Com'l		90	mA
			7.5 ns			130	mA
			15, 25 ns	Mil/Ind		120	mA
			10 ns			120	mA
I_{CC2}[6]	Operating Power Supply Current	V_{CC} = Max., V_{IL} = 0V, V_{IH} = 3V, Output Open, Device Programmed as a 10-Bit Counter, f = 25 MHz	10, 15, 25 ns	Com'l		110	mA
			7.5 ns			140	mA
			15, 25 ns	Mil/Ind		130	mA
			10 ns			130	mA

Capacitance[6]

Parameter	Description	Test Conditions	Min.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz		10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz		10	pF

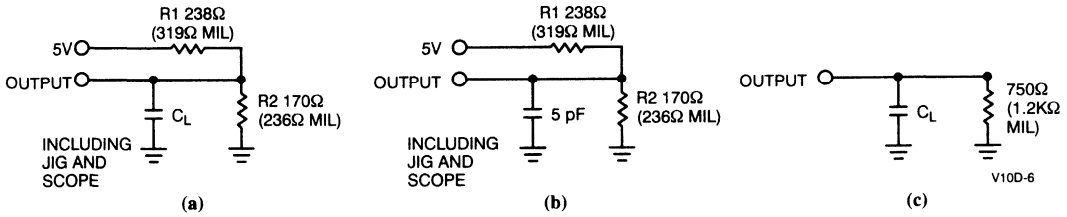
Endurance Characteristics[6]

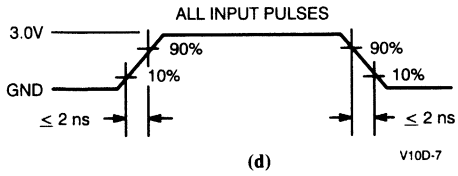
Parameter	Description	Test Conditions	Min.	Max.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions	100		Cycles

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. V_{IL} (Min.) is equal to −3.0V for pulse durations less than 20 ns.
5. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
6. Tested initially and after any design or process changes that may affect these parameters.

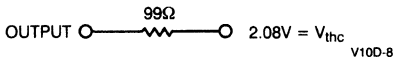
AC Test Loads and Waveforms



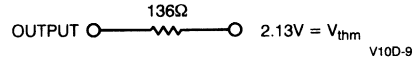


(d)

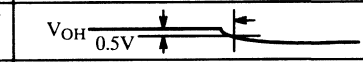
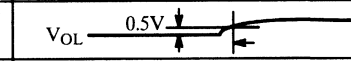
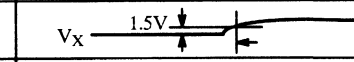
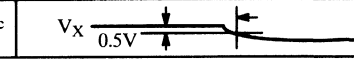
Equivalent to: THÉVENIN EQUIVALENT (Commercial)



Equivalent to: THÉVENIN EQUIVALENT (Military)



Load Speed	C_L	Package
7.5, 10, 15, 25 ns	50 pF	PDIP, CDIP, PLCC, LCC

Parameter	V_X	Output Waveform—Measurement Level
$t_{ER(-)}$	1.5V	
$t_{ER(+)}$	2.6V	
$t_{EA(+)}$	0V	
$t_{EA(-)}$	V_{thc}	

(e) Test Waveforms

Commercial Switching Characteristics (PALC22V10D)[2, 7]

Parameter	Description	22V10D-7		22V10D-10		22V10D-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[8, 9]	3	7.5	3	10	3	15	ns
t_{EA}	Input to Output Enable Delay[10]		8		10		15	ns
t_{ER}	Input to Output Disable Delay[11]		8		10		15	ns
t_{CO}	Clock to Output Delay[8, 9]	2	5	2	7	2	8	ns
t_{S1}	Input or Feedback Set-Up Time	5		6		10		ns
t_{S2}	Synchronous Preset Set-Up Time	6		7		10		ns
t_H	Input Hold Time	0		0		0		ns
t_P	External Clock Period (t_{CO} + t_S)	10		12		20		ns
t_{WH}	Clock Width HIGH[6]	3		3		6		ns
t_{WL}	Clock Width LOW[6]	3		3		6		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[12]	100		76.9		55.5		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[6, 13]	166		142		83.3		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[6, 14]	133		111		68.9		MHz
t_{CF}	Register Clock to Feedback Input[6, 15]		2.5		3		4.5	ns
t_{AW}	Asynchronous Reset Width	8		10		15		ns
t_{AR}	Asynchronous Reset Recovery Time	5		6		10		ns
t_{AP}	Asynchronous Reset to Registered Output Delay		12		13		20	ns
t_{SPR}	Synchronous Preset Recovery Time	6		8		10		ns
t_{PR}	Power-Up Reset Time[6, 16]	1		1		1		μs

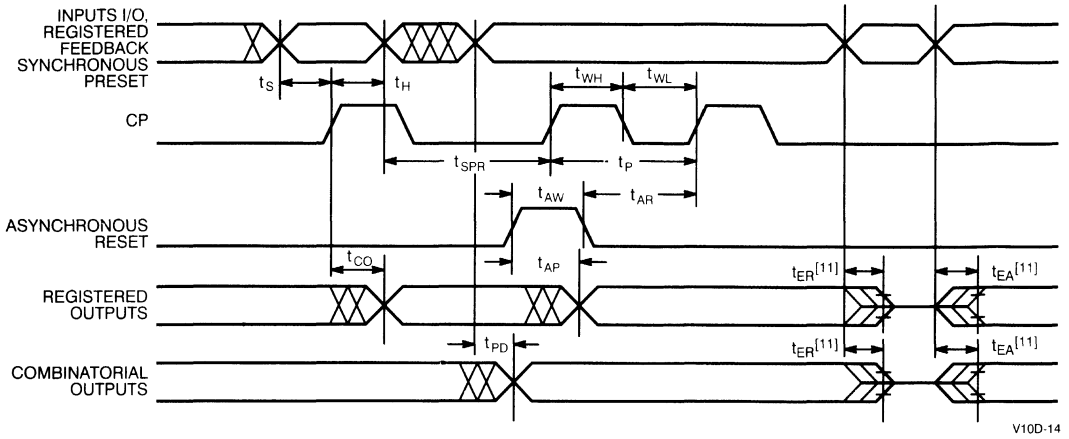
Notes:

7. Part (a) of AC Test Loads and Waveforms is used for all parameters except t_{ER} and $t_{EA(+)}$. Part (b) of AC Test Loads and Waveforms is used for t_{ER}. Part (c) of AC Test Loads and Waveforms is used for $t_{EA(+)}$.
8. Min. times are tested initially and after any design or process changes that may affect these parameters.
9. This specification is guaranteed for all device outputs changing state in a given access cycle.
10. The test load of part (a) of AC Test Loads and Waveforms is used for measuring $t_{EA(-)}$. The test load of part (c) of AC Test Loads and Waveforms is used for measuring $t_{EA(+)}$ only. Please see part (e) of AC Test Loads and Waveforms for enable and disable test waveforms and measurement reference levels.
11. This parameter is measured as the time after output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below V_{OH} min. or a previous LOW level has risen to 0.5 volts above V_{OL} max. Please see part (e) of AC Test Loads and Waveforms for enable and disable test waveforms and measurement reference levels.
12. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
13. This specification indicates the guaranteed maximum frequency at which the device can operate in data path mode.
14. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feedback can operate.
15. This parameter is calculated from the clock period at f_{MAX} internal ($1/f_{MAX3}$) as measured (see Note 11 above) minus t_S.
16. The registers in the PALC22V10D have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to a logic LOW state. The output state will depend on the polarity of the output buffer. This feature is useful in establishing state machine initialization. To insure proper operation, the rise in V_{CC} must be monotonic and the timing constraints depicted in Power-Up Reset Waveform must be satisfied.

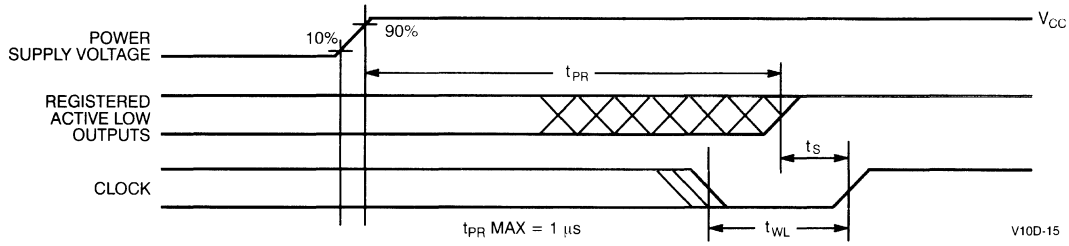
Military and Industrial Switching Characteristics (PALC22V10D)[2, 7]

Parameter	Description	22V10D–10		22V10D–15		22V10D–25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[8, 9]	3	10	3	15	3	25	ns
t_{EA}	Input to Output Enable Delay[10]		10		15		25	ns
t_{ER}	Input to Output Disable Delay[11]		10		15		25	ns
t_{CO}	Clock to Output Delay[8, 9]	2	7	2	8	2	15	ns
t_{S1}	Input or Feedback Set-Up Time	6		10		18		ns
t_{S2}	Synchronous Preset Set-Up Time	7		10		18		ns
t_H	Input Hold Time	0		0		0		ns
t_P	External Clock Period ($t_{CO} + t_S$)	12		20		33		ns
t_{WH}	Clock Width HIGH[6]	3		6		14		ns
t_{WL}	Clock Width LOW[6]	3		6		14		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[12]	76.9		50.0		30.3		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[6, 13]	142		83.3		35.7		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[6, 14]	111		68.9		32.2		MHz
t_{CF}	Register Clock to Feedback Input[6, 15]		3		4.5		13	ns
t_{AW}	Asynchronous Reset Width	10		15		25		ns
t_{AR}	Asynchronous Reset Recovery Time	6		12		25		ns
t_{AP}	Asynchronous Reset to Registered Output Delay		12		20		25	ns
t_{SPR}	Synchronous Preset Recovery Time	8		20		25		ns
t_{PR}	Power-Up Reset Time[6, 16]	1		1		1		µs

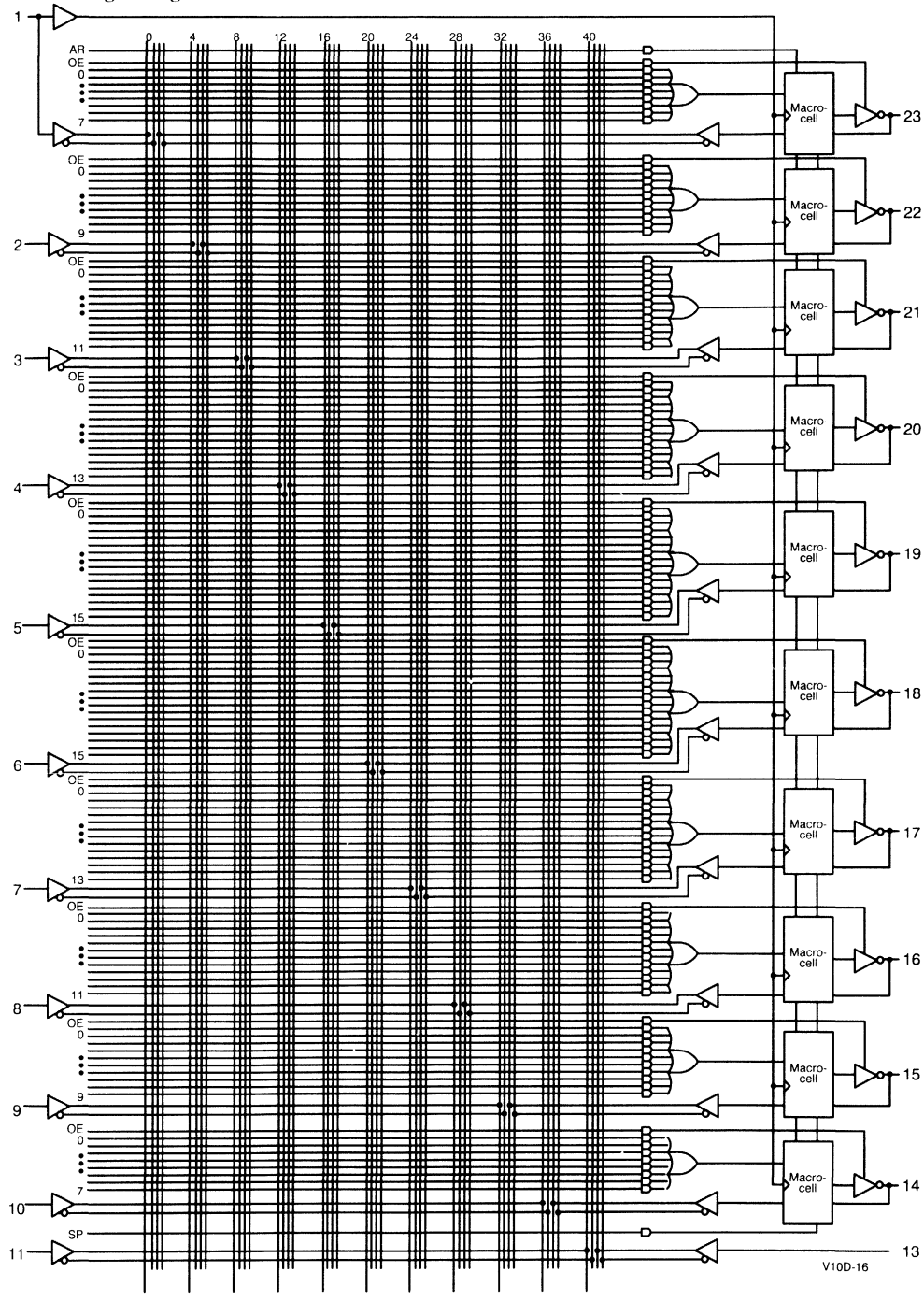
Switching Waveform



Power-Up Reset Waveform[16]



Functional Logic Diagram for PALC22V10D



Ordering Information

I_{CC} (mA)	t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package Name	Package Type	Operating Range
130	7.5	5	5	PALC22V10D–7JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
				PALC22V10D–7PC	P13	24-Lead (300-Mil) Molded DIP	
90	10	6	7	PALC22V10D–10JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
				PALC22V10D–10PC	P13	24-Lead (300-Mil) Molded DIP	
150	10	6	7	PALC22V10D–10DMB	D14	24-Lead (300-Mil) CerDIP	Military/ Industrial
				PALC22V10D–10JI	J64	28-Lead Plastic Leaded Chip Carrier	
				PALC22V10D–10KMB	K73	24-Lead Rectangular Cerpack	
				PALC22V10D–10LMB	L64	28-Square Leadless Chip Carrier	
				PALC22V10D–10PI	P13	24-Lead (300-Mil) Molded DIP	
90	15	7.5	10	PALC22V10D–15JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
				PALC22V10D–15PC	P13	24-Lead (300-Mil) Molded DIP	
120	15	7.5	10	PALC22V10D–15DMB	D14	24-Lead (300-Mil) CerDIP	Military/ Industrial
				PALC22V10D–15JI	J64	28-Lead Plastic Leaded Chip Carrier	
				PALC22V10D–15KMB	K73	24-Lead Rectangular Cerpack	
				PALC22V10D–15LMB	L64	28-Square Leadless Chip Carrier	
				PALC22V10D–15PI	P13	24-Lead (300-Mil) Molded DIP	
	25	15	15	PALC22V10D–25DMB	D14	24-Lead (300-Mil) CerDIP	
				PALC22V10D–25JI	J64	28-Lead Plastic Leaded Chip Carrier	
				PALC22V10D–25KMB	K73	24-Lead Rectangular Cerpack	
				PALC22V10D–25LMB	L64	28-Square Leadless Chip Carrier	
				PALC22V10D–25PI	P13	24-Lead (300-Mil) Molded DIP	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	9, 10, 11
t_{CO}	9, 10, 11
t_S	9, 10, 11
t_H	9, 10, 11

Document #: 38–00185–G

PAL22V10G
PAL22VP10G

Universal PAL® Device

Features

- **Ultra high speed supports today's and tomorrow's fastest microprocessors**
  - **— t_{PD} = 4 ns**
  - **— t_S = 2.5 ns**
  - **— f_{MAX} = 166 MHz (External)**
- **Reduced ground bounce and undershoot**
- **PLCC and LCC packages with additional V_{CC} and V_{SS} pins for lowest ground bounce**
- **Up to 22 inputs and 10 outputs for more logic power**
- **Variable product terms**
  - **— 8 to 16 per output**
- **10 user-programmable output macrocells**
  - **— Output polarity control**
  - **— Registered or combinatorial operation**
  - **— 2 new feedback paths (PAL22VP10G)**
- **Synchronous PRESET, asynchronous RESET, and PRELOAD capability for flexible design and testability**
- **High reliability**
  - **— Proven Ti-W fuse technology**
  - **— AC and DC tested at the factory**
- **Security Fuse**

Functional Description

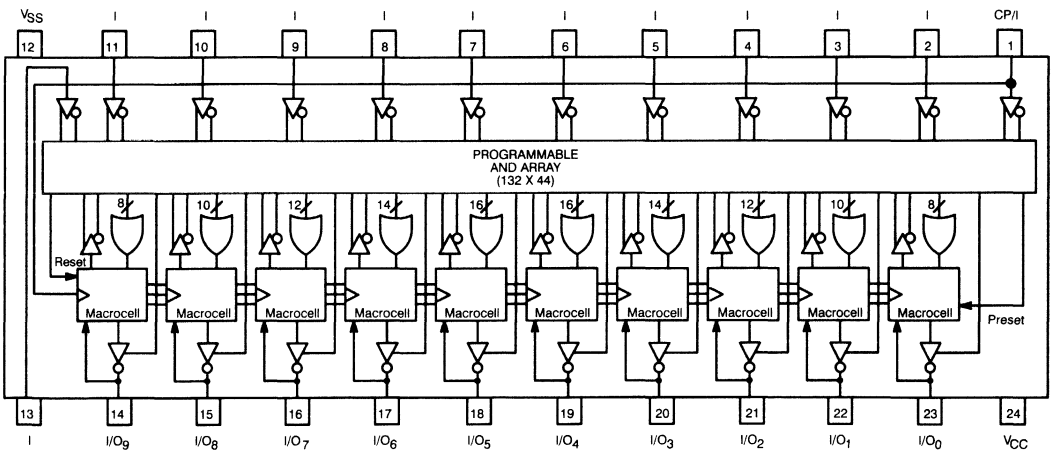
The Cypress PAL22V10G and PAL22VP10G are second-generation programmable array logic devices. Using BiCMOS process and Ti-W fuses, the PAL22V10G and PAL22VP10G use the familiar sum-of-products (AND-OR) logic structure and a new concept, the programmable macrocell.

Both the PAL22V10G and PAL22VP10G provide 12 dedicated input pins and 10 I/O pins (see Logic Block Diagram). By selecting each I/O pin as either permanent or temporary input, up to 22 inputs can be achieved. Applications requiring up to 21 inputs and a single output, down to 12 inputs and 10 outputs can be realized. The output enable product term available on each I/O allows this selection.

The PAL22V10G and PAL22VP10G feature variable product term architecture, where 8 to 16 product terms are allocated to each output. This structure permits more applications to be implemented with these devices than with other PAL devices that have fixed number of product terms for each output.

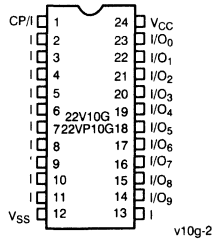
2

Logic Block Diagram and PDIP (P)/CDIP (D) Pin Configuration

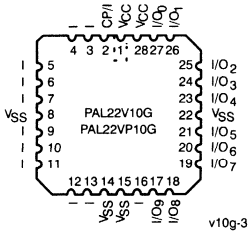


Pin Configurations

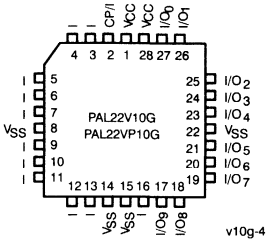
DIP (P, D) Top View



LCC (L) Top View



PLCC (J) Top View



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Functional Description (continued)

Additional features include common synchronous preset and asynchronous reset product terms. They eliminate the need to use standard product terms for initialization functions

Both the PAL22V10G and PAL22VP10G automatically reset on power-up. In addition, the preload capability allows the output registers to be set to any desired state during testing.

A security fuse is provided on each of these two devices to prevent copying of the device fuse pattern.

With the programmable macrocells and variable product term architecture, the PAL22V10G and PAL22VP10G can implement logic functions in the 700 to 800 gate array complexity, with the inherent advantages of programmable logic.

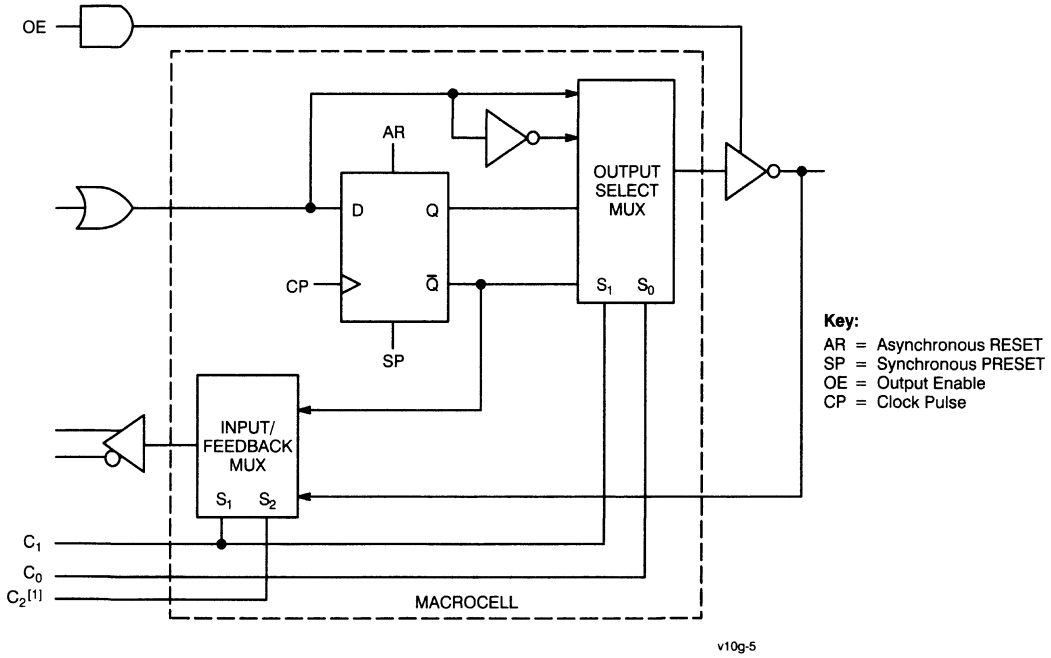
Programmable Macrocell

The PAL22V10G and PAL22VP10G each has 10 programmable output macrocells (see Macrocell figure). On the PAL22V10G two fuses (C_1 and C_0) can be programmed to configure output in one of four ways. Accordingly, each output can be registered or combinatorial with an active HIGH or active LOW polarity. The feedback to the array is also from this output (see *Figure 1*). An additional fuse (C_2) in the PAL22VP10G provides for two feedback paths (see *Figure 2*).

Programming

The PAL22V10G and PAL22VP10G can be programmed using the *Impulse3* programmer available from Cypress Semiconductor and also with Data I/O, Logical Devices, STAG and other programmers. Please contact your local Cypress representative for further information.

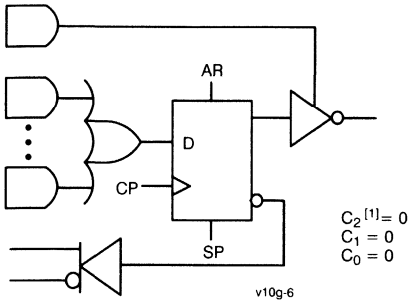
Macrocell



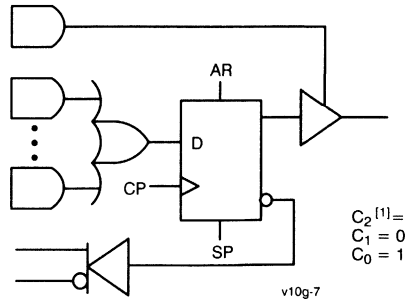
Output Macrocell Configuration

C_2[1]	C_1	C_0	Output Type	Polarity	Feedback
0	0	0	Registered	Active LOW	Registered
0	0	1	Registered	Active HIGH	Registered
X	1	0	Combinatorial	Active LOW	I/O
X	1	1	Combinatorial	Active HIGH	I/O
1	0	0	Registered	Active LOW	I/O[1]
1	0	1	Registered	Active HIGH	I/O[1]

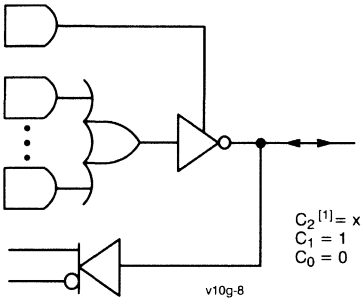
Notes:
1. PAL22VP10G only.



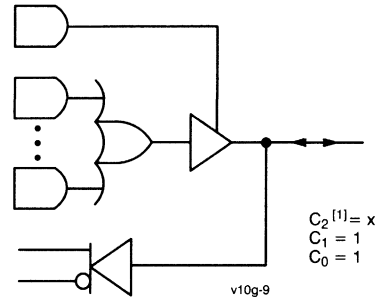
REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT

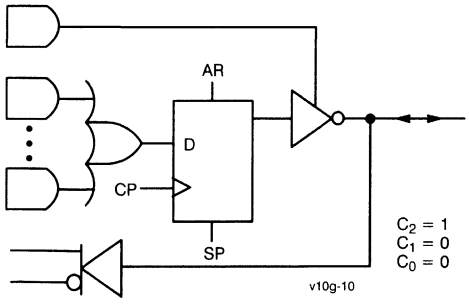


I/O FEEDBACK, COMBINATORIAL, ACTIVE-LOW OUTPUT

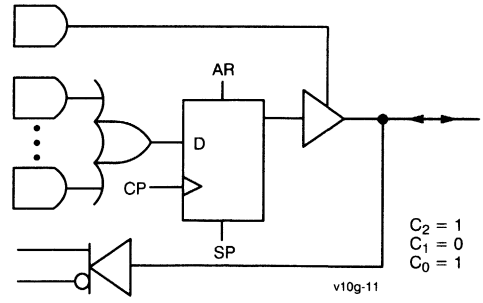


I/O FEEDBACK, COMBINATORIAL, ACTIVE-HIGH OUTPUT

Figure 1. PAL22V10G and PAL22VP10G Macrocell Configurations



I/O FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



I/O FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT

Figure 2. Additional Macrocell Configurations for the PAL22VP10G

Selection Guide

		22V10G–4 22VP10G–4	22V10G–5 22VP10G–5	22V10G–6 22VP10G–6	22V10G–7 22VP10G–7	22V10G–10 22VP10G–10
I_{CC} (mA)	Commercial	190	190	190	190	190
	Military				190	190
t_{PD} (ns)	Commercial	4	5	6.0	7.5	10
	Military				7.5	10
t_S (ns)	Commercial	2.5	2.5	3.0	3.0	3.6
	Military				3.0	3.6
t_{CO} (ns)	Commercial	3.5	4/4.5	5.5	6.0	7.5
	Military				6.0	7.5
f_{MAX} (MHz) (External)	Commercial	166	153.8	117	111	90
	Military				111	90

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to V_{CC}

DC Input Voltage ..... −0.5V to V_{CC}

DC Input Current ..... − 30 mA to +5 mA (except during programming)

DC Program Voltage 10V

Junction Temperature (PLCC) ..... 150°C

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Military[2]	−55°C to +125°C	5V ± 10%

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	Com'l	2.4		V
			I_{OH} = −2 mA	Mil	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA	Com'l		0.5	V
			I_{OL} = 12 mA	Mil		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs[3]			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs[3]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le 2.7V$, V_{CC} = Max.			−250	50	µA
I_I	Maximum Input Current	V_{IN} = V_{CC}, V_{CC} = Max.		Com'l		100	µA
				Mil		250	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			−100	100	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[4]			−30	−120	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = GND, Outputs Open		Com'l		190	mA
				Mil		190	

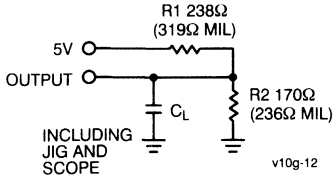
Notes:

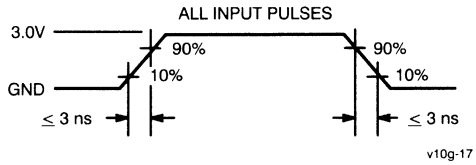
2. t_A is the "instant on" case temperature.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

Capacitance[5]

Parameter	Description	Typ.	Unit
C_{IN}	Input Capacitance	6	pF
C_{OUT}	Output Capacitance	8	pF

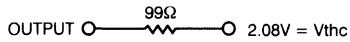
AC Test Loads and Waveforms





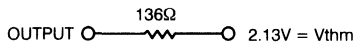
C_L[6] = 50 pF

Equivalent to: THÉVENIN EQUIVALENT

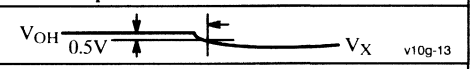
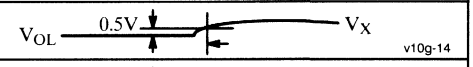
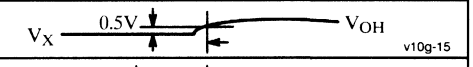
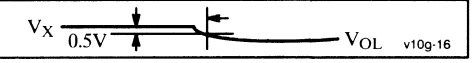


Commercial

Equivalent to: THÉVENIN EQUIVALENT



Military

Parameter	V_X	Output Waveform—Measurement Level
$t_{ER(-)}$	1.5V	 v10g-13
$t_{ER(+)}$	2.6V	 v10g-14
$t_{EA(+)}$	1.5V	 v10g-15
$t_{EA(-)}$	1.5V	 v10g-16

Notes:
5. Tested initially and after any design or process changes that may affect these parameters.
6. C_L = 5 pF for t_{ER} measurement for all packages.

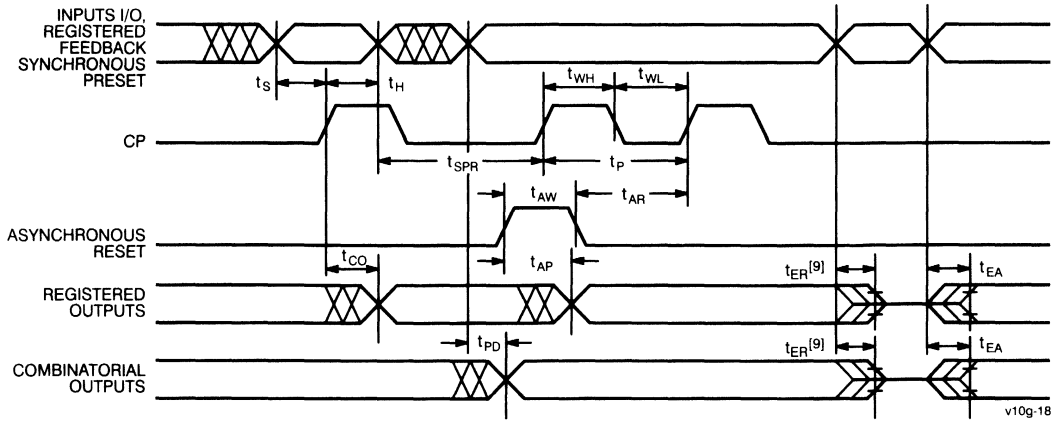
Switching Characteristics[7]

Parameter	Description	22V10G–4 22VP10G–4		22V10G–5 22VP10G–5		22V10G–6 22VP10G–6		22V10G–7 22VP10G–7		22V10G–10 22VP10G–10		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[8]	1	4	1	5	1	6	2	7.5	2	10	ns
t_{EA}	Input to Output Enable Delay	1	5	1	6	1	6	2	7.5	2	10	ns
t_{ER}	Input to Output Disable Delay[9]	1	4	1	5	1	6	2	7.5	2	10	ns
t_{CO}	Clock to Output Delay[8]	1	3.5	1	4	1	5.5	1	6.0	1	7.5	ns
t_S	Input or Feedback Set-Up Time	2.5		2.5		3		3		3.6		ns
t_H	Input Hold Time	0		0		0		0		0		ns
t_P	External Clock Period (t_{CO} + t_S)	6.0		6.5		8.5		9		11.1		ns
t_{WH}	Clock Width HIGH[5]	2.0		2.5		3		3		3		ns
t_{WL}	Clock Width LOW[5]	2.0		2.5		3		3		3		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[10]	166		153.8		117		111		90		MHz
f_{MAX2}	Data Path Maximum Frequency [5, 11, 12]	250		200		166		166		133		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[9, 13]	181.8		181.8		142		133		100		MHz
t_{CF}	Register Clock to Feedback Input[14]		3		3		4		4.5		6.4	ns
t_{AW}	Asynchronous Reset Width	5		6		7.5		8.5		10		ns
t_{AR}	Asynchronous Reset Recovery Time	4		4		4		5		6		ns
t_{AP}	Asynchronous Reset to Registered Output Delay	2	6	2	7	2	11	2	12	2	12	ns
t_{SPR}	Synchronous Preset Recovery Time	4		4		4		5		6		ns
t_{PR}	Power-Up Reset Time[15]	1		1		1		1		1		µs

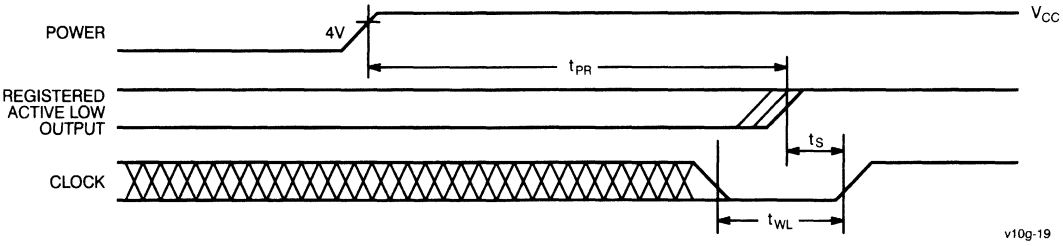
Notes:

7. AC test load used for all parameters except where noted.
8. This specification is guaranteed for all device outputs changing state in a given access cycle.
9. This parameter is measured as the time after output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below V_{OH} min. or a previous LOW level has risen to 0.5 volts above V_{OL} max.
10. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
11. This specification indicates the guaranteed maximum frequency at which an individual output register can be cycled.
12. Lesser of $1/(t_{WH} + t_{WL})$, $1/t_{CO}$ or $1/(t_S + t_H)$.
13. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal-only feedback can operate.
14. This parameter is calculated from the clock period at f_{MAX} internal (f_{MAX3}) as measured (see Note 11) minus t_S.
15. The registers in the PAL22V10G and PAL22VP10G have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to a logic LOW state. The output state will depend on the polarity of the output buffer. This feature is useful in establishing state machine initialization. To insure proper operation, the rise in V_{CC} must be monotonic and the timing constraints depicted in power-up reset waveforms must be satisfied.

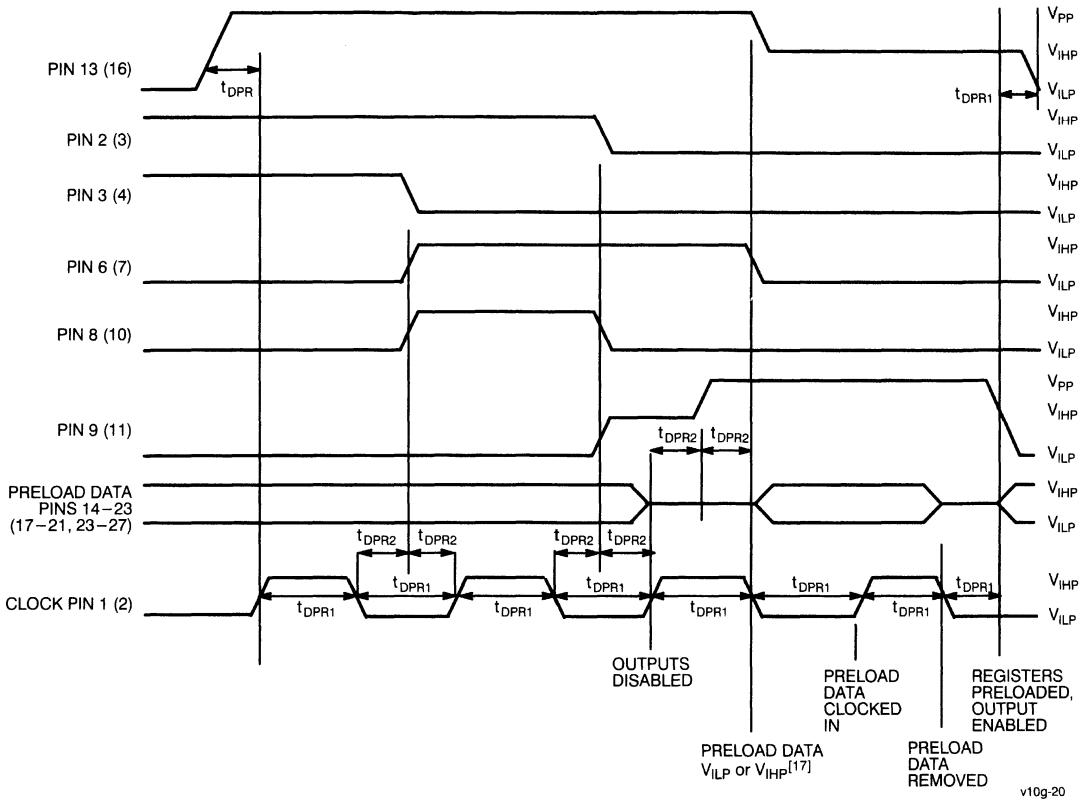
Switching Waveform



Power-Up Reset Waveform[15]



Preload Waveform[16]

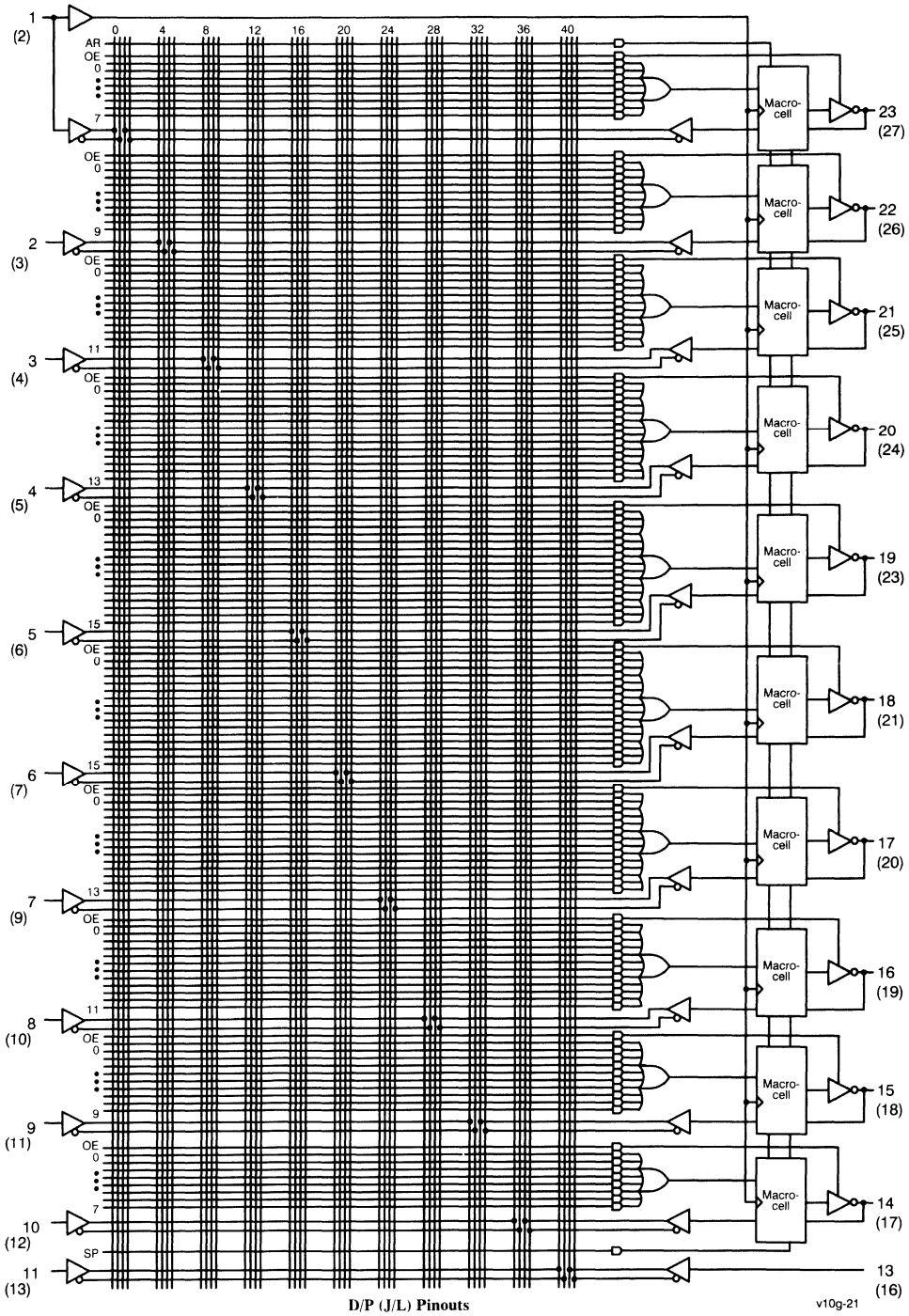


Notes (the numbers in parantheses refer to J and L packages):
16. Pins 4 (5), 5 (6), 7 (9) at V_{ILP}; Pins 10 (12) and 11 (13) at V_{IHP}; V_{CC} (Pin 24 (1 and 28)) at V_{CCP}
17. Pins 2–8 (3–7, 9, 10), 10 (12), 11 (13) can be set at V_{IHP} or V_{ILP} to insure asynchronous reset is not active.

Forced Level on Register Pin During Preload	Register Q Output State After Preload
V_{IHP}	HIGH
V_{ILP}	LOW

Name	Description	Min.	Max.	Unit
V_{PP}	Programming Voltage	9.25	9.75	V
t_{DPR1}	Delay for Preload	1		µs
t_{DPR2}	Delay for Preload	0.5		µs
V_{ILP}	Input LOW Voltage	0	0.4	V
V_{IHP}	Input HIGH Voltage	3	4.75	V
V_{CCP}	V_{CC} for Preload	4.75	5.25	V

Functional Logic Diagram for PAL22V10G/PAL22VP10G



D/P (J/L) Pinouts

Ordering Information

I_{CC} (mA)	t_{PD} (ns)	f_{MAX} (MHz)	Ordering Code	Package Name	Package Type	Operating Range
190	4	166	PAL22V10G–4JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	5	153.8	PAL22V10G–5JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	6	117	PAL22V10G–6JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	7.5	111	PAL22V10G–7JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
			PAL22V10G–7PC	P13	24-Lead (300-Mil) Molded DIP	
			PAL22V10G–7LMB	L64	28-Pin Square Leadless Chip Carrier	Military
	10	90	PAL22V10G–10JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22V10G–10PC	P13	24-Lead (300-Mil) Molded DIP	
			PAL22V10G–10LMB	L64	28-Pin Square Leadless Chip Carrier	Military

I_{CC} (mA)	t_{PD} (ns)	f_{MAX} (MHz)	Ordering Code	Package Type	Package Type	Operating Range
190	4	166	PAL22VP10G–4JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	5	153.8	PAL22VP10G–5JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	6	117	PAL22VP10G–6JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	7.5	111	PAL22VP10G–7JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
			PAL22VP10G–7PC	P13	24-Lead (300-Mil) Molded DIP	
			PAL22VP10G–7LMB	L64	28-Pin Square Leadless Chip Carrier	Military
	10	90	PAL22VP10G–10JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22VP10G–10PC	P13	24-Lead (300-Mil) Molded DIP	
			PAL22VP10G–10LMB	L64	28-Pin Square Leadless Chip Carrier	Military

Shaded area contains advanced information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristerics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{PD}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_S	7, 8, 9, 10, 11
t_H	7, 8, 9, 10, 11

Document #: 38–A–00044–B

CY7C330

CMOS Programmable Synchronous State Machine

Features

- Twelve I/O macrocells each having:
  - registered, three-state I/O pins
  - input register clock select multiplexer
  - feed back multiplexer
  - output enable (OE) multiplexer
- All twelve macrocell state registers can be hidden
- User-configurable state registers—JK, RS, T, or D
- One input multiplexer per pair of I/O macrocells allows I/O pin associated with a hidden macrocell state register to be saved for use as an input
- Four dedicated hidden registers
- Eleven dedicated, registered inputs
- Three separate clocks—two inputs, one output
- Common (pin 14–controlled) or product term–controlled output enable for each I/O pin
- 256 product terms—32 per pair of macrocells, variable distribution
- Global, synchronous, product term–controlled, state register set and reset—inputs to product term are clocked by input clock
- 66-MHz operation
  - 3-ns input set-up and 12-ns clock to output
  - 15-ns input register clock to state register clock
- Low power
  - 130 mA I_{CC}
- 28-pin, 300-mil DIP, LCC
- Erasable and reprogrammable

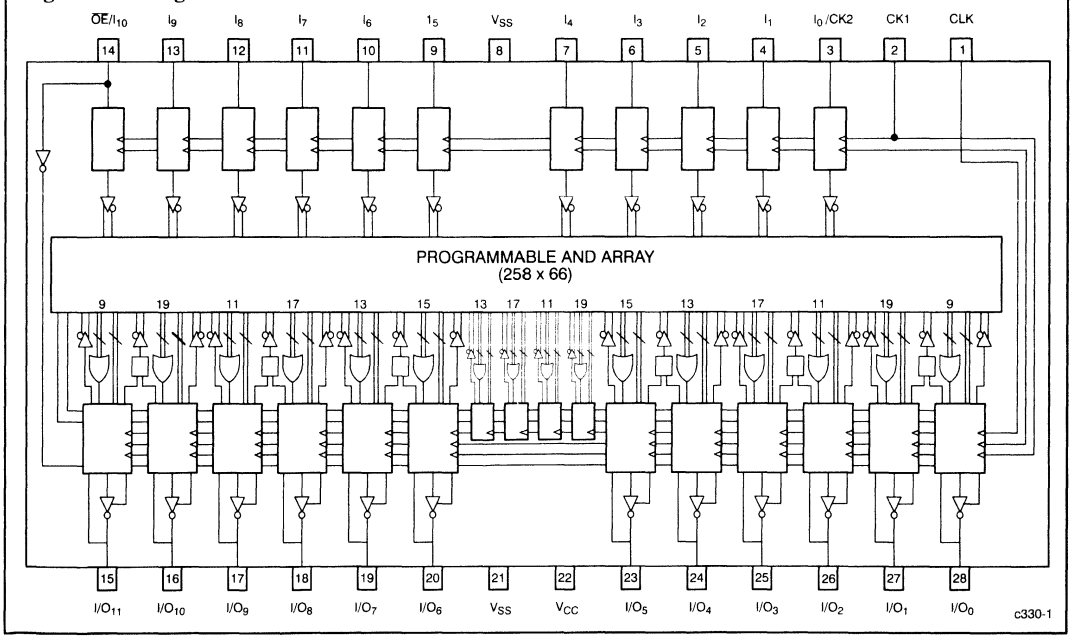
Functional Description

The CY7C330 is a high-performance, erasable, programmable, logic device (EPLD) whose architecture has been optimized to enable the user to easily and efficiently construct very high performance synchronous state machines.

The unique architecture of the CY7C330, consisting of the user-configurable output macrocell, bidirectional I/O capability, input registers, and three separate clocks, enables the user to design high-performance state machines that can communicate either with each other or with microprocessors over bidirectional parallel buses of user-definable widths.

2

Logic Block Diagram

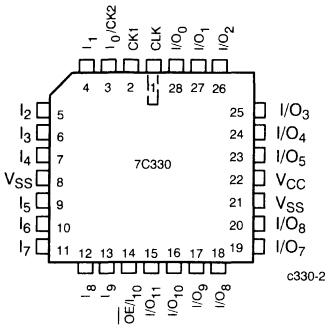


Selection Guide

		7C330–66	7C330–50	7C330–40	7C330–33	7C330–28
Maximum Operating Frequency, f_{MAX} (MHz)	Commercial	66.6	50.0		33.3	
	Military		50.0	40.0		28.5
Power Supply Current I_{CC1} (mA)	Commercial	140	130		130	
	Military		160	150		150

Pin Configuration

LCC/PLCC
Top View



Functional Description (continued)

Three separate clocks permit independent, synchronous state machines to be synchronized to each other. The two input clocks, C1, C2, enable the state machine to sample input signals that may be generated by another system and that may be available on its bus for a short period of time.

The user-configurable state register flip-flops enable the designer to designate JK-, RS-, T-, or D-type devices, so that the number of product terms required to implement the logic is minimized.

The major functional blocks of the CY7C330 are (1) the input registers and (input) clock multiplexers, (2) the EPROM (AND) cell array, (3) the twelve I/O macrocells and (4) the four hidden registers.

Input Registers and Clock Multiplexers

There are a total of eleven dedicated input registers. Each input register consists of a D flip-flop and a clock multiplexer. The clock multiplexer is user-programmable to select either CK1 or CK2 as the clock for the flip-flop. CK2 and $\overline{OE}$ can alternatively be used as inputs to the array. The twenty-two outputs of the registers (i.e., the Q and $\overline{Q}$ outputs of the input registers) drive the array of EPROM cells.

An architecture configuration bit (C4) is reserved for each dedicated input register cell to allow selection of either input clock CK1 or CK2 as the input register clock for each dedicated input cell. If the CK2 clock is not needed, that input may also be used as a general-purpose array input. In this case the input register for this input can only be clocked by input clock CK1. *Figure 1* illustrates the dedicated input cell composed of an input register, an Input Clock Multiplexer, and architecture configuration bit C4 which determines the input clock selected.

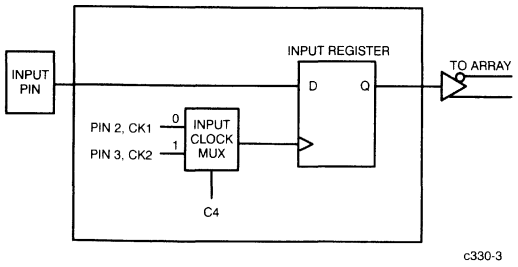


Figure 1. Dedicated Input Cell

I/O Macrocell

The logic diagram of CY7C330 I/O macrocell is shown in *Figure 2* There are a total of twelve identical macrocells.

Each macrocell consists of:

– An Output State register that is clocked by the global state counter clock, CLK (Pin 1). The state register can be configured as a D, JK, RS, or T flip-flop (default is a D-type flip-flop). Polarity can be controlled in the D flip-flop implementation by use of the exclusive or function. Data is sampled on the LOW to HIGH clock transition. All of the state registers have a common reset and set which are controlled synchronously by Product Terms which are generated in the EPROM cell array.

– A Macrocell Input register that may be clocked by either the CK1 or CK2 input clock as programmed by the user with architecture configuration bit C2, which controls the I/O Macrocell Input Clock Multiplexer. The Macrocell Input registers are initialized upon power-up such that all of the Q outputs are at logic LOW level and the $\overline{Q}$ outputs are at a logic HIGH level.

– An Output Enable Multiplexer (OE), which is user programmable using architecture configuration bit C0, can select either the common $\overline{OE}$ signal from pin 14 or, for each cell individually, the signal from the output enable product term associated with each macrocell. The output enable input signal to the array product term is clocked through the input register by the selected input register clock, CK1 or CK2.

– An Input Feedback Multiplexer, which is user programmable, can select either the output of the state register or the output of the Macrocell Input register to be fed back into the array. This option is programmed by architecture configuration bit C1. If the output of the Macrocell Input register is selected by the Feedback Multiplexer, the I/O pin becomes bidirectional.

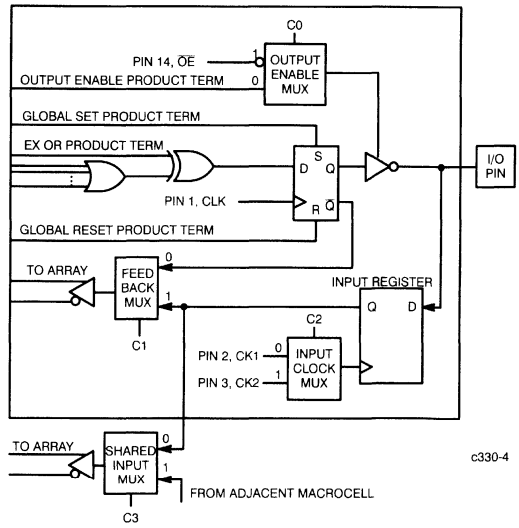


Figure 2. Macrocell and Shared Input Multiplexer

Functional Description (continued)

Macrocell Input Multiplexer

Each pair of I/O macrocells share a Macrocell Input Multiplexer that selects the output of one or the other of the pair's input registers to be fed to the input array. This multiplexer is shown in *Figure 2*. The Macrocell Input Multiplexer allows the input pin of a macrocell, for which the state register has been hidden by feeding back its input to the input array to be preserved for use as an input pin. This is possible as long as the other macrocell of the pair is not needed as an input or does not require state register feedback. The input pin input register output that would normally be blocked by the hidden state register feedback can be routed to the array input path of the companion macrocell for use as array input.

State Registers

By use of the exclusive OR gate, the state register may be configured as a JK-, RS-, or T-type register. The default is a D-type register. For the D-type register, the exclusive OR function can be used to select the polarity or the register output.

The set and reset of the state register are global synchronous signals. They are controlled by the logic of two global product terms, for which input signals are clocked through the input registers by either of the input clocks, CK1 or CK2.

Hidden Registers

In addition to the twelve macrocells, which contain a total of twenty-four registers, there are four hidden registers whose outputs are not brought out to the device output pins. The Hidden State Register Macrocell is shown in *Figure 3*.

The four hidden registers are clocked by the same clock as the macrocell state registers. All of the hidden register flip-flops have a common, synchronous set, S, as well as a common, synchronous reset, R, which override the data at the D input. The S and R signals are product terms that are generated in the array and are the same signals used to preset and reset the state register flip-flops.

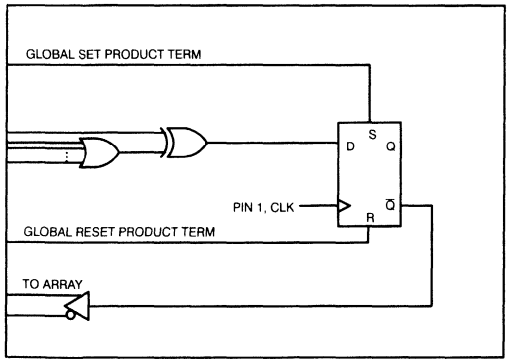


Figure 3. Hidden State Register Macrocell

Macrocell Product Term Distribution

Each pair of macrocells has a total of thirty-two product terms. Two product terms of each macrocell pair are used for the output enables (OEs) for the two output pins. Two product terms are also used as one input to each of the two exclusive OR gates in the macrocell pair. The number of product terms available to the designer is then 32 − 4 = 28 for each macrocell pair. These product terms are divided between the macrocell state register flip-flops as show in *Table 1*.

Table 1. Product Term Distribution for Macrocell State Register Flip-Flops

Macrocell	Pin Number	Product Terms
0	28	9
1	27	19
2	26	11
3	25	17
4	24	13
5	23	15
6	20	15
7	19	13
8	18	17
9	17	11
10	16	19
11	15	9

Hidden State Register Product Term Distribution

Each pair of hidden registers also has a total of 32 product terms. Two product terms are used as one input to each of the exclusive OR gates. However, because the register outputs do not go to any output pins, output enable product terms are not required. Therefore, 30 product terms are available to the designer for each pair of hidden registers. The product term distribution for the four hidden registers is shown in *Table 2*.

Table 2. Product Term Distribution for Hidden Registers

Hidden Register Cell	Product Terms
0	19
1	11
2	17
3	13

Architecture Configuration Bits

The architecture configuration bits are used to program the multiplexers. The function of the architecture bits is outlined in *Table 3*.

Table 3. Architecture Configuration Bits

Architecture Configuration Bit		Number of Bits	Value	Function
C0	Output Enable Select MUX	12 Bits, 1 per I/O Macrocell	0—Virgin State	Output Enable Controlled by Product Term
			1—Programmed	Output Enable Controlled by Pin 14
C1	State Register Feedback MUX	12 Bits, 1 per I/O Macrocell	0—Virgin State	State Register Output is Fed Back to Input Array
			1—Programmed	I/O Macrocell is Configured as an Input and Output of Input Register is Fed to Array
C2	I/O Macrocell Input Register Clock Select MUX	12 Bits, 1 per I/O Macrocell	0—Virgin State	CK1 Input Register Clock (Pin 2) is Connected to I/O Macrocell Input Register Clock Input
			1—Programmed	CK2 Input Register Clock (Pin 3) is Connected to I/O Macrocell Input Register Clock Input
C3	I/O Macrocell Pair Input Select MUX	6 Bits, 1 per I/O Macrocell Pair	0—Virgin State	Selects Data from I/O Macrocell Input Register of Macrocell A of Macrocell Pair
			1—Programmed	Selects Data from I/O Macrocell Input Register of Macrocell B of Macrocell Pair
C4	Dedicated Input Register Clock Select MUX	11 Bits, 1 per Dedicated Input Cell	0—Virgin State	CK1 Input Register Clock (Pin 2) is Connected to Dedicated Input Register Clock Input
			1—Programmed	CK2 Input Register Clock (Pin 3) is Connected to Dedicated Input Register Clock Input

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 22 to Pins 8 and 21) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (LOW) ..... 12 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

DC Programming Voltage 13.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

Note:

1. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[2]

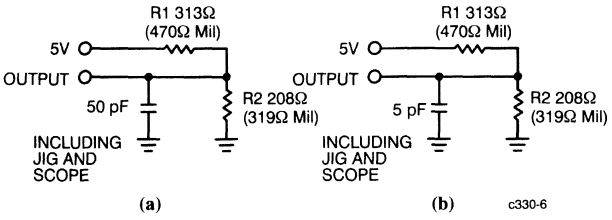
Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL} I_{OH} = −3.2 mA (Com'l), I_{OH} = −2 mA (Mil)		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}, I_{OL} = 12 mA (Com'l), I_{OH} = 8 mA (Mil)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Logical HIGH Voltage for all Inputs[3]		2.2		V
V_{IL}	Input LOW Voltage	Guaranteed Logical LOW Voltage for all Inputs[3]			0.8	V
I_{IX}	Input Leakage Current	V_{SS} < V_{IN} < V_{CC}, V_{CC} = Max.		−10	+10	μA
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{SS} < V_{OUT} < V_{CC},		−40	+40	μA
I_{SC}[4]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[5]		−30	−90	mA
I_{CC1}	Standby Power Supply Current	V_{CC} = Max., V_{IN} = GND Outputs Open	Commercial −66		140	mA
			Commercial −33, −50		130	
			Military −50		160	
			Military −28, −40		150	
I_{CC2}	Power Supply Current at Frequency[4,6]	V_{CC} = Max. Outputs Disabled (in High Z State), Device Operating at f_{MAX} External (f_{MAX1})	Commercial −66		180	mA
			Commercial −33, −50		160	
			Military −50		200	
			Military −28, −40		180	

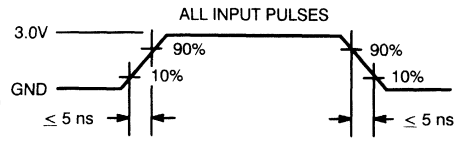
Capacitance[4]

Parameter	Description	Test Conditions	Min.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V at f = 1 MHz,		10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V at f = 1 MHz,		10	pF

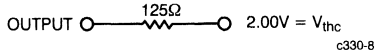
Notes:
2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
4. Tested initially and after any design or process changes that may affect these parameters.
5. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
6. Tested by periodic sampling of production product.

AC Test Loads and Waveforms

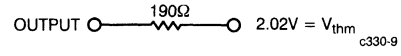




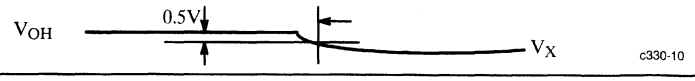
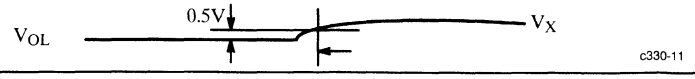
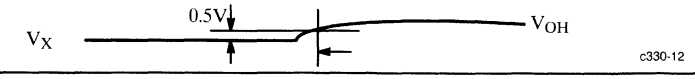
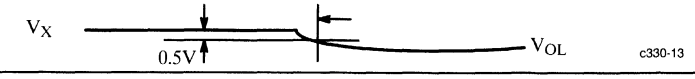
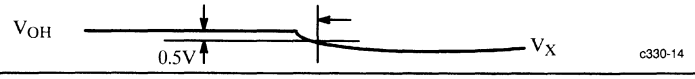
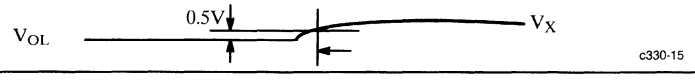
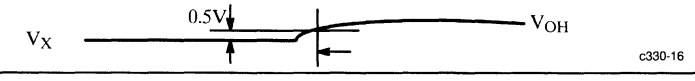
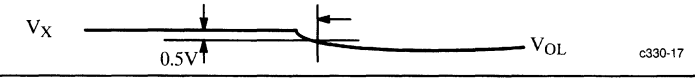
Equivalent to: THÉVENIN EQUIVALENT (Commercial)



Equivalent to: THÉVENIN EQUIVALENT (Military)



AC Test Loads and Waveforms (continued)

Parameter	V_X	Output Waveform—Measurement Level
$t_{PXZ(-)}$	1.5V	
$t_{PXZ(+)}$	2.6V	
$t_{PZX(+)}$	V_{thc}	
$t_{PZX(-)}$	V_{thc}	
$t_{CER(-)}$	1.5V	
$t_{CER(+)}$	2.6V	
$t_{CEA(+)}$	V_{thc}	
$t_{CEA(-)}$	V_{thc}	

(c) Test Waveforms and Measurement Levels

Switching Characteristics Over the Operating Range[2, 7]

Parameter	Description	Commercial						Military						Unit
		−66		−50		−33		−50		−40		−28		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{IS}	Input or Feedback Set-Up Time to Input Register Clock	3		5		10		5		5		10		ns
t_{OS}	Input Register Clock to Output Register Clock	15		20		30		20		25		35		ns
t_{CO}	Output Register Clock to Output Delay		12		15		20		15		20		25	ns
t_{IH}	Input Register Hold Time	5		5		5		5		5		5		ns
t_{CEA}	Input Register Clock to Output Enable Delay		20		20		30		20		25		35	ns
t_{CER}	Input Register Clock to Output Disable Delay[8]		20		20		30		20		25		35	ns
t_{PZX}	Pin 14 Enable to Output Enable Delay		20		20		30		20		25		35	ns
t_{PXZ}	Pin 14 Disable to Output Disable Delay[8]		20		20		30		20		25		35	ns
t_{WH}	Input or Output Clock Width HIGH[4, 6]	6		8		12		8		10		15		ns
t_{WL}	Input or Output Clock Width LOW[4, 6]	6		8		12		8		10		15		ns

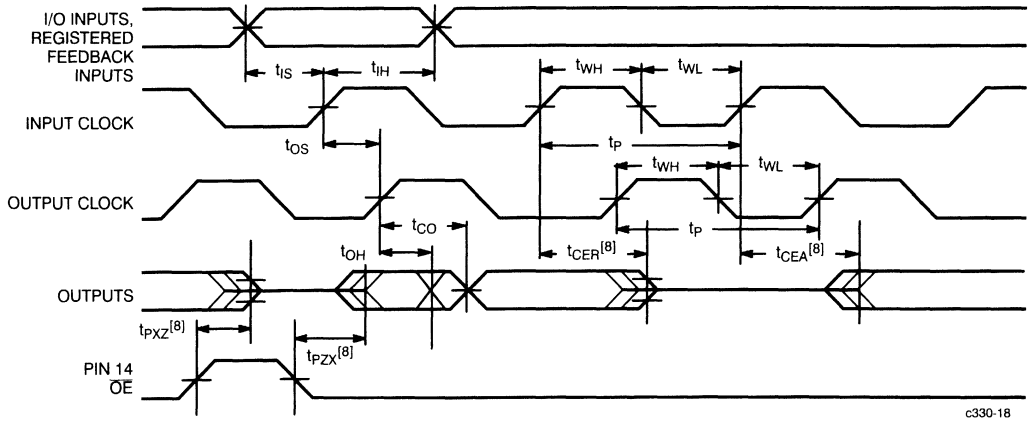
Switching Characteristics Over the Operating Range[2, 7] (continued)

Parameter	Description	Commercial						Military						Unit
		-66		-50		-33		-50		-40		-28		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{OH}	Output Data Stable Time from Synchronous Clock Input[9]	3		3		3		3		3		3		ns
$t_{IOH} - t_{IH}$	Output Data Stable Time This Device Minus I/P Reg Hold Time Same Device[10]	0		0		0		0		0		0		ns
$t_{OH} - t_{IH}$ 33X	Output Data Stable Time Minus I/P Reg Hold Time 7C330 and 7C332 Devices[11]	0		0		0		0		0		0		ns
t_P	External Clock Period ($t_{ICO} + t_{IS}$), Input and Output Clock Common	15		20		30		20		25		35		ns
f_{MAX1}	Maximum External Operating Frequency ($1/(t_{CO} + t_{IS})$)[12]	66.6		50.0		33.3		50.0		40.0		28.5		MHz
f_{MAX2}	Maximum Register Toggle Frequency[6, 13]	83.3		62.5		41.6		62.5		50.0		33.3		MHz
f_{MAX3}	Maximum Internal Operating Frequency[14]	74.0		57.0		37.0		57.0		45.0		30.0		MHz

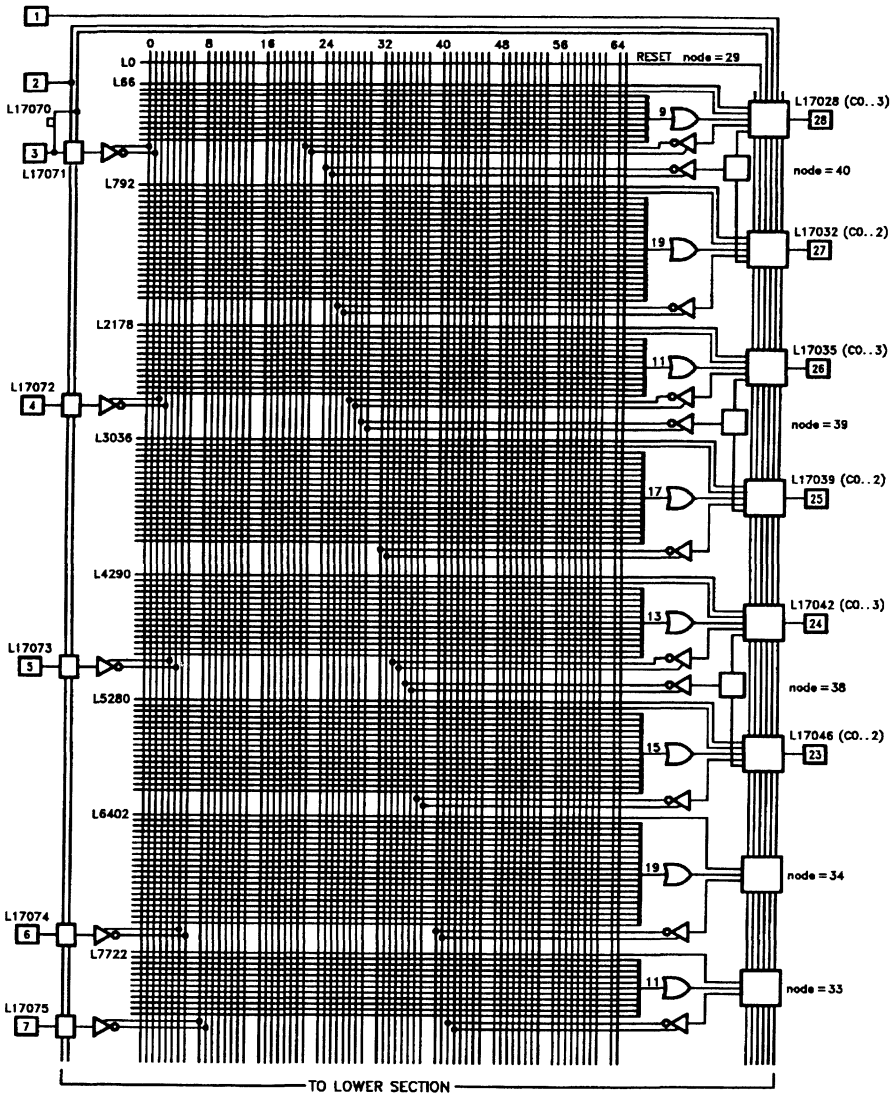
Notes:

7. Part (a) of AC Test Loads is used for all parameters except t_{CEA}, t_{CER}, t_{PZX}, and t_{PXZ}, which use part (b).
8. This parameter is measured as the time after output register disable input that the previous output data state remains stable on the output. This delay is measure to the point at which a previous HIGH level has fallen to 0.5V below V_{OH} Min. or a previous LOW level has risen to 0.5V above V_{OL} Max. Please see part (c) of AC Test Loads and Waveforms for enable and disable test waveforms and measurement reference levels.
9. This parameter is measured as the time after output register clock input that the previous output data state remains stable on the output.
10. This difference parameter is designed to guarantee that any 7C330 output fed back to its own inputs externally or internally will satisfy the input register minimum input hold time. This parameter is guaranteed for a given individual device and is tested by a periodic sampling of production product.
11. This specification is intended to guarantee feeding of this signal to another 33X family input register cycled by the same clock with sufficient output data stable time to insure that the input hold time minimum of the following input register is satisfied. This parameter difference specification is guaranteed by periodic sampling of production product of 7C330 and 7C332. It is guaranteed to be met only for devices at the same ambient temperature and V_{CC} supply voltage.
12. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
13. This specification indicates the guaranteed maximum frequency at which an individual input or output register can be cycled.
14. This specification indicates the guaranteed maximum frequency at which a state machine configuration with only internal feedback can operate. This parameter is tested periodically on a sample basis.

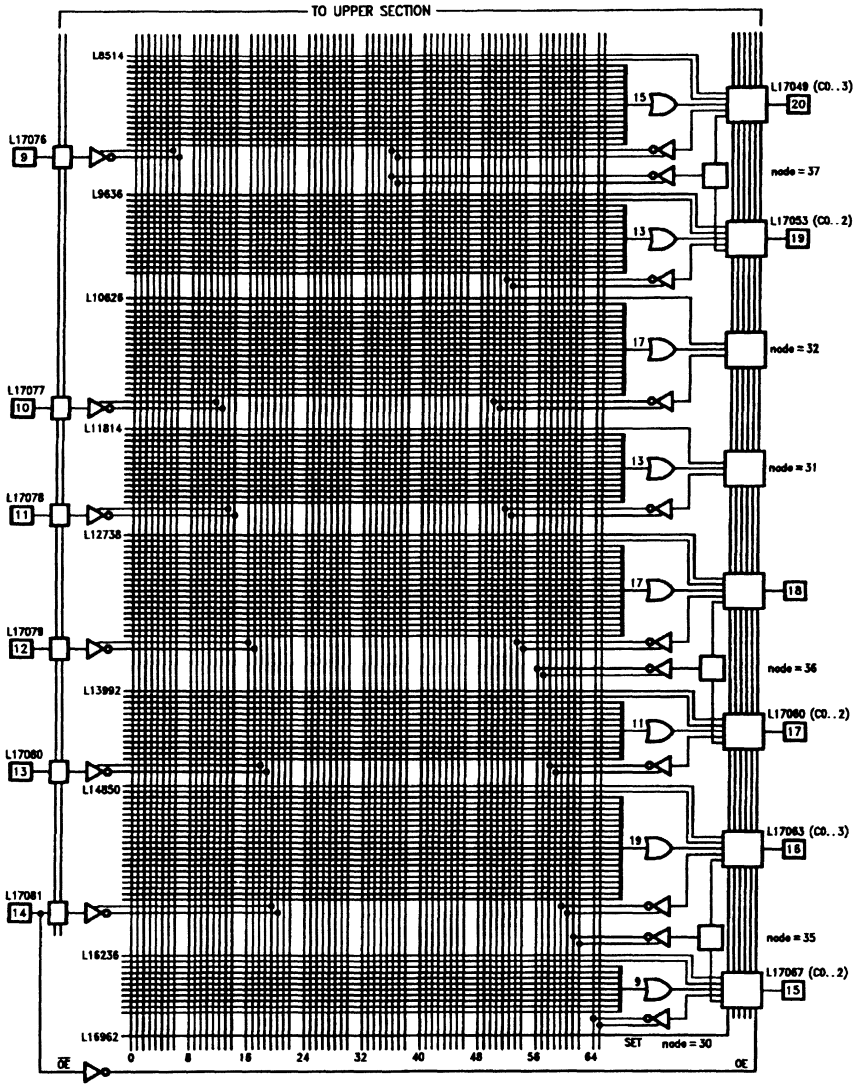
Switching Waveform



CY7C330 Logic Diagram (Upper Half)



CY7C330 Logic Diagram (Lower Half)



Ordering Information

I_{CC1} (max)	f_{MAX} (MHz)	Ordering Code	Package Name	Package Type	Operating Range
140	66.6	CY7C330–66HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
		CY7C330–66JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C330–66PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C330–66WC	W22	28-Lead (300-Mil) Windowed CerDIP	
160	50	CY7C330–50DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C330–50HMB	H64	28-Pin Windowed Leaded Chip Carrier	
		CY7C330–50LMB	L64	28-Square Leadless Chip Carrier	
		CY7C330–50QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C330–50TMB	T74	28-Lead Windowed Cerpack	
		CY7C330–50WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
130	50	CY7C330–50HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
		CY7C330–50JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C330–50PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C330–50WC	W22	28-Lead (300-Mil) Windowed CerDIP	
150	40	CY7C330–40DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C330–40HMB	H64	28-Pin Windowed Leaded Chip Carrier	
		CY7C330–40LMB	L64	28-Square Leadless Chip Carrier	
		CY7C330–40QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C330–40TMB	T74	28-Lead Windowed Cerpack	
		CY7C330–40WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
130	33.3	CY7C330–33HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
		CY7C330–33JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C330–33PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C330–33WC	W22	28-Lead (300-Mil) Windowed CerDIP	
150	28.5	CY7C330–28DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C330–28HMB	H64	28-Pin Windowed Leaded Chip Carrier	
		CY7C330–28LMB	L64	28-Square Leadless Chip Carrier	
		CY7C330–28QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C330–28TMB	T74	28-Lead Windowed Cerpack	
		CY7C330–28WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{IS}	9, 10, 11
t_{OS}	9, 10, 11
t_{CO}	9, 10, 11
t_{CEA}	9, 10, 11
t_{PZX}	9, 10, 11

Document #: 38-00064-D

CY7C331

Asynchronous Registered EPLD

Features

- Twelve I/O macrocells each having:
  - One state flip-flop with an XOR sum-of-products input
  - One feedback flip-flop with input coming from the I/O pin
  - Independent (product term) set, reset, and clock inputs on all registers
  - Asynchronous bypass capability on all registers under product term control (r = s = 1)
  - Global or local output enable on three-state I/O
  - Feedback from either register to the array
- 192 product terms with variable distribution to macrocells
- 13 inputs, 12 feedback I/O pins, plus 6 shared I/O macrocell feedbacks for a total of 31 true and complementary inputs
- High speed: 20 ns maximum t_{PD}
- Security bit
- Space-saving 28-pin slim-line DIP package; also available in 28-pin PLCC
- Low power
  - 90 mA typical I_{CC} quiescent
  - 180 mA I_{CC} maximum
  - UV-erasable and reprogrammable
  - Programming and operation 100% testable

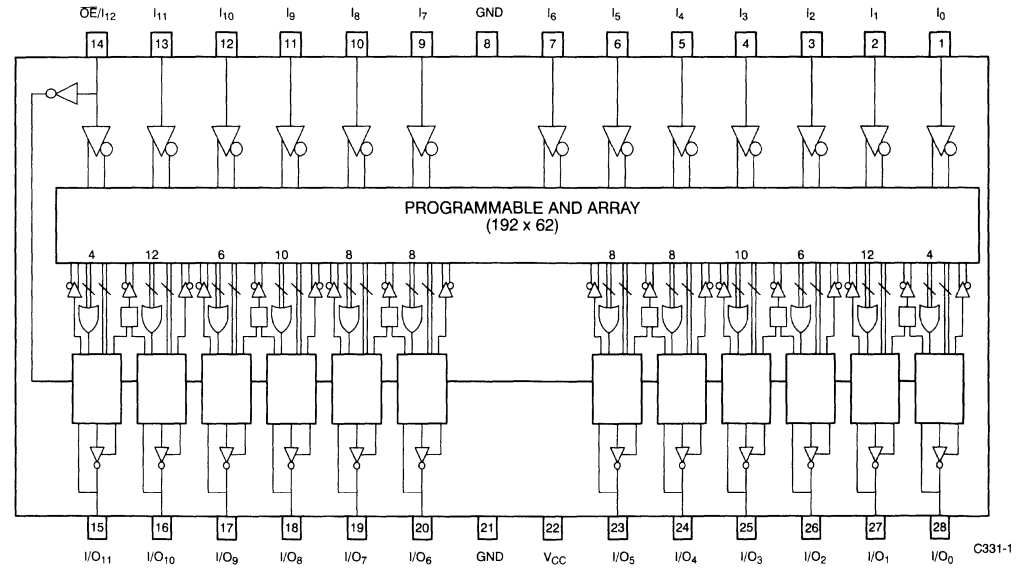
Functional Description

The CY7C331 is the most versatile PLD available for asynchronous designs. Central resources include twelve full D-type flip-flops with separate set, reset, and clock capability. For increased utility, XOR gates are provided at the D-inputs and the product term allocation per flip-flop is variably distributed.

I/O Resources

Pins 1 through 7 and 9 through 14 serve as array inputs; pin 14 may also be used as a global output enable for the I/O macrocell three-state outputs. Pins 15 through 20 and 23 through 28 are connected to I/O macrocells and may be managed as inputs or outputs depending on the configuration and the macrocell OE terms.

Logic Block Diagram

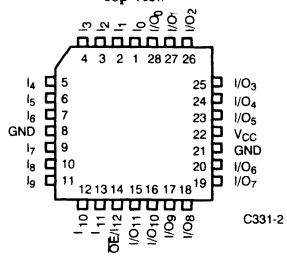


Selection Guide

Generic Part Number	I_{CC1} (mA)		t_{PD} (ns)		t_S (ns)		t_{CO} (ns)	
	Com'l	Mil	Com'l	Mil	Com'l	Mil	Com'l	Mil
CY7C331-20	130		20		12		20	
CY7C331-25	120	160	25	25	12	15	25	25
CY7C331-30		150		30		15		30
CY7C331-40		150		40		20		40

Pin Configuration

PLCC
Top View



I/O Resources (continued)

It should be noted that there are two ground connections (pins 8 and 21) which, together with V_{CC} (pin 22) are located centrally on the package. The reason for this placement and dual-ground structure is to minimize the ground-loop noise when the outputs are driving simultaneously into a heavy capacitive load.

The CY7C331 has twelve I/O macrocells (see *Figure 1*). Each macrocell has two D-type flip-flops. One is fed from the array, and one from the I/O pin. For each flip-flop there are three dedicated product terms driving the R, S, and clock inputs, respectively. Each macrocell has one input to the array and for each pair of macrocells there is one shared input to the array. The macrocell input to the array may be configured to come from the 'Q' output of either flip-flop.

The D-type flip-flop that is fed from the array (i.e., the state flip-flop) has a logical XOR function on its input that combines a single product term with a sum(OR) of a number of product terms. The single product term is used to set the polarity of the output or to implement toggling (by including the current output in the product term).

The R and S inputs to the flip-flops override the current setting of the 'Q' output. The S input sets 'Q' true and the R input resets 'Q' (sets it false). If both R and S are asserted (true) at once, then the output will follow the input ('Q' = 'D') (see *Table 1*).

Table 1. RS Truth Table

R	S	Q
1	0	0
0	1	1
1	1	D

Shared Input Multiplexer

The input associated with each pair of macrocells may be configured by the shared input multiplexer to come from either macrocell; the 'Q' output of the flip-flop coming from the I/O pin is used as the input signal source (see *Figure 2*).

Product Term Distribution

The product terms are distributed to the macrocells such that 32 product terms are distributed between two adjacent macrocells.

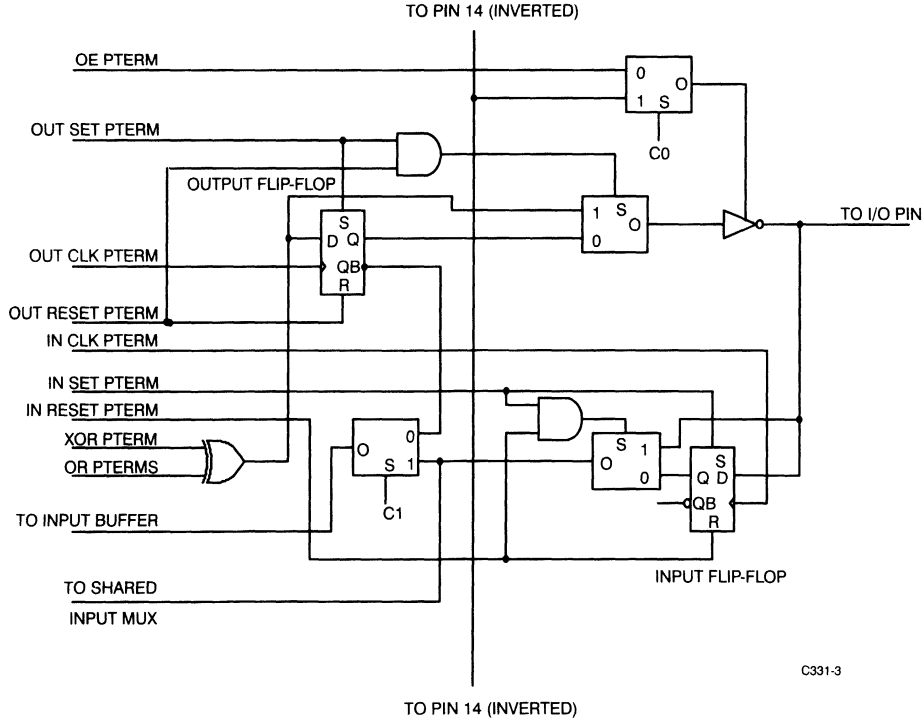


Figure 1. I/O Macrocell

Product Term Distribution (continued)

The pairing of macrocells is the same as it is for the shared inputs. Eight of the product terms are used in each macrocell for set, reset, clock, output enable, and the upper part of the XOR gate. This leaves 16 product terms per pair of macrocells to be divided between the sum-of-products inputs to the two state registers. The following table shows the I/O pin pairing for shared inputs, and the product term (PT) allocation to macrocells associated with the I/O pins (see *Table 2*).

Table 2. Product Term Distribution

Macrocell	Pin Number	Product Terms
0	28	4
1	27	12
2	26	6
3	25	10
4	24	8
5	23	8
6	20	8
7	19	8
8	18	10
9	17	6
10	16	12
11	15	4

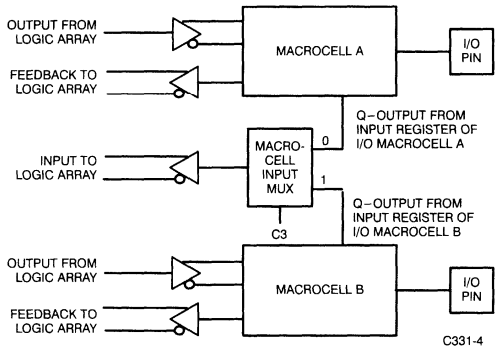


Figure 2. Shared Input Multiplexer

The CY7C331 is configured by three arrays of configuration bits (C0, C1, C2). For each macrocell, there is one C0 bit and one C1 bit. For each pair of macrocells there is one C2 bit.

There are twelve C0 bits, one for each macrocell. If C0 is programmed for a macrocell, then the three-state enable (OE) will be controlled by pin 14 (the global OE). If C0 is not programmed, then the OE product term for that macrocell will be used.

There are twelve C1 bits, one for each macrocell. The C1 bit selects inputs for the product term (PT) array from either the state register (if the bit is unprogrammed) or the input register (if the bit is programmed).

There are six C2 bits, providing one C2 bit for each pair of macrocells. The C2 bit controls the shared input multiplexer; if the C2 bit is not programmed, then the input to the product term array comes from the upper macrocell (A). If the C2 bit is programmed, then the input comes from the lower macrocell (B).

The timing diagrams for the CY7C331 cover state register, input register, and various combinational delays. Since internal clocks are the outputs of product terms, all timing is from the transition of the inputs causing the clock transition.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 8 or 21) ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (LOW) ..... 12 mA

Static Discharge Voltage ..... >1500V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

DC Programming Voltage ..... 13.0 V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL} I_{OH} = − 3.2 mA (Com'l), I_{OH} = − 2 mA (Mil)		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL} I_{OL} = 12 mA (Com'l), I_{OL} = 8 mA (Mil)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed HIGH Input, all Inputs[3]		2.2		V
V_{IL}	Input LOW Voltage	Guaranteed LOW Input, all Inputs[3]			0.8	V
I_{IX}	Input Leakage Current	V_{SS} < V_{IN} < V_{CC}, V_{CC} = Max.		−10	+10	μA
I_{OZ}	Output Leakage Current	V_{SS} < V_{OUT} < V_{CC}, V_{CC} = Max.		−40	+40	μA
I_{SC}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = 0.5V[5]		−30	−90	mA
I_{CC1}	Standby Power Supply Current	V_{CC} = Max., V_{IN} = GND, Outputs Open	Com'l −20		130	mA
			Com'l −25		120	
			Mil −25		160	mA
			Mil −30, −40		150	
I_{CC2}	Power Supply Current at Frequency[4, 6]	V_{CC} = Max., Outputs Disabled (in High Z State) Device Operating at f_{MAX} External (f_{MAX1})	Com'l		180	mA
			Mil		200	

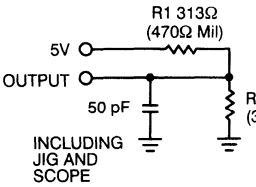
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V at f = 1 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V at f = 1 MHz	10	pF

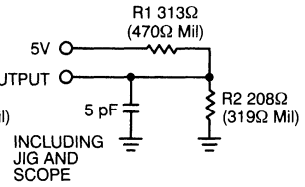
Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
4. Tested initially and after any design or process changes that may affect these parameters.
5. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
6. Because these input signals are controlled by product terms, active input polarity may be of either polarity. Internal active input polarity has been shown for clarity.

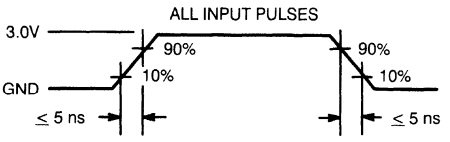
AC Test Loads and Waveforms



(a)

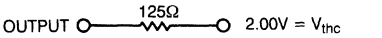


(b) C331-5



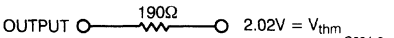
C331-6

Equivalent to: THÉVENIN EQUIVALENT (Commercial)

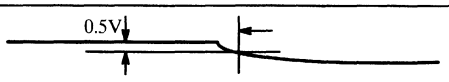
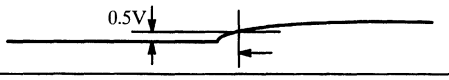
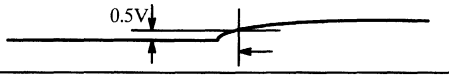
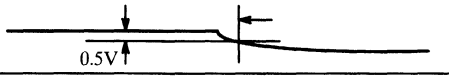
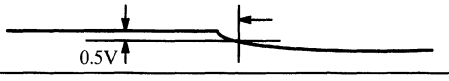
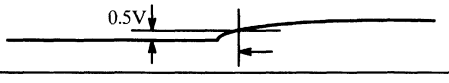
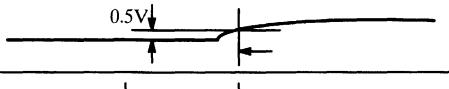
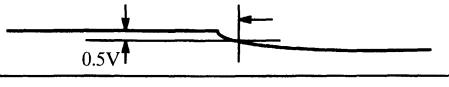


C331-7

Equivalent to: THÉVENIN EQUIVALENT (Military)



C331-8

Parameter	V_X	Output Waveform—Measurement Level
$t_{PXZ(-)}$	1.5V	 C331-9
$t_{PXZ(+)}$	2.6V	 C331-10
$t_{PZX(+)}$	V_{thc}	 C331-11
$t_{PZX(-)}$	V_{thc}	 C331-12
$t_{ER(-)}$	1.5V	 C331-13
$t_{ER(+)}$	2.6V	 C331-14
$t_{EA(+)}$	V_{thc}	 C331-15
$t_{EA(-)}$	V_{thc}	 C331-16

(c) Test Waveforms and Measurement Levels

Switching Characteristics Over the Operating Range[2]

Parameter	Description	Commercial				Unit
		−20		−25		
		Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[7]		20		25	ns
t_{ICO}	Input Register Clock to Output Delay[8]		35		40	ns
t_{IOH}	Output Data Stable Time from Input Clock[8]	5		5		ns
t_{IS}	Input or Feedback Set-Up Time to Input Register Clock[8]	2		2		ns
t_{IH}	Input Register Hold Time from Input Clock[8]	11		13		ns

Switching Characteristics Over the Operating Range[2] (continued)

Parameter	Description	Commercial				Unit
		-20		-25		
		Min.	Max.	Min.	Max.	
t_{IAR}	Input to Input Register Asynchronous Reset Delay[8]		35		40	ns
t_{IRW}	Input Register Reset Width[4, 8]	35		40		ns
t_{IRR}	Input Register Reset Recovery Time[4, 8]	35		40		ns
t_{IAS}	Input to Input Register Asynchronous Set Delay[8]		35		40	ns
t_{ISW}	Input Register Set Width[4, 8]	35		40		ns
t_{ISR}	Input Register Set Recovery Time[4, 8]	35		40		ns
t_{WH}	Input and Output Clock Width HIGH[8, 9, 10]	12		15		ns
t_{WL}	Input and Output Clock Width LOW[8, 9, 10]	12		15		ns
f_{MAX1}	Maximum Frequency with Feedback in Input Registered Mode ($1/(t_{ICO} + t_{IS})$)[11]	27.0		23.8		MHz
f_{MAX2}	Maximum Frequency Data Path in Input Registered Mode (Lowest of $1/t_{ICO}$, $1/(t_{WH} + t_{WL})$, or $1/(t_{IS} + t_{IH})$)[8]	28.5		25.0		MHz
$t_{IOH}-t_{IH}33X$	Output Data Stable from Input Clock Minus Input Register Input Hold Time for 7C330 and 7C332[12, 13]	0		0		ns
t_{CO}	Output Register Clock to Output Delay[9]		20		25	ns
t_{OH}	Output Data Stable Time from Output Clock[9]	3		3		ns
t_S	Output Register Input Set-Up Time to Output Clock[9]	12		12		ns
t_H	Output Register Input Hold Time from Output Clock[9]	8		8		ns
t_{OAR}	Input to Output Register Asynchronous Reset Delay[9]		20		25	ns
t_{ORW}	Output Register Reset Width[9]	20		25		ns
t_{ORR}	Output Register Reset Recovery Time[9]	20		25		ns
t_{OAS}	Input to Output Register Asynchronous Set Delay[9]		20		25	ns
t_{OSW}	Output Register Set Width[9]	20		25		ns
t_{OSR}	Output Register Set Recovery Time[9]	20		25		ns
t_{EA}	Input to Output Enable Delay[14, 15]		25		25	ns
t_{ER}	Input to Output Disable Delay[14, 15]		25		25	ns
t_{PZX}	Pin 14 to Output Enable Delay[14, 15]		20		20	ns
t_{PXZ}	Pin 14 to Output Disable Delay[14, 15]		20		20	ns
f_{MAX3}	Maximum Frequency with Feedback in Output Registered Mode ($1/(t_{CO} + t_S)$)[16, 17]	31.2		27.0		MHz
f_{MAX4}	Maximum Frequency Data Path in Output Registered Mode (Lowest of $1/t_{CO}$, $1/(t_{WH} + t_{WL})$, or $1/(t_S + t_H)$))[9]	41.6		33.3		MHz
$t_{OH}-t_{IH}33X$	Output Data Stable from Output Clock Minus Input Register Input Hold Time for 7C330 and 7C332[13, 18]	0		0		ns
f_{MAX5}	Maximum Frequency Pipelined Mode[10, 17]	35.0		30.0		MHz

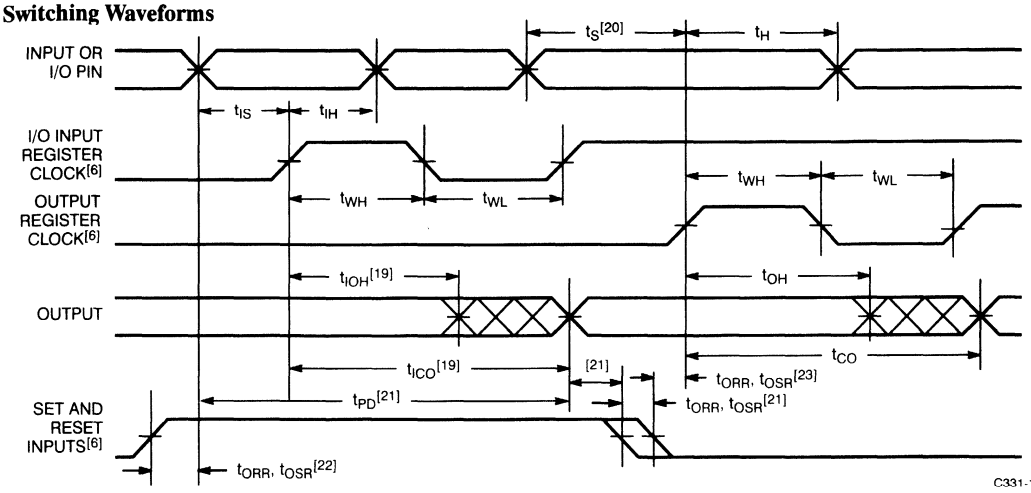
Notes:

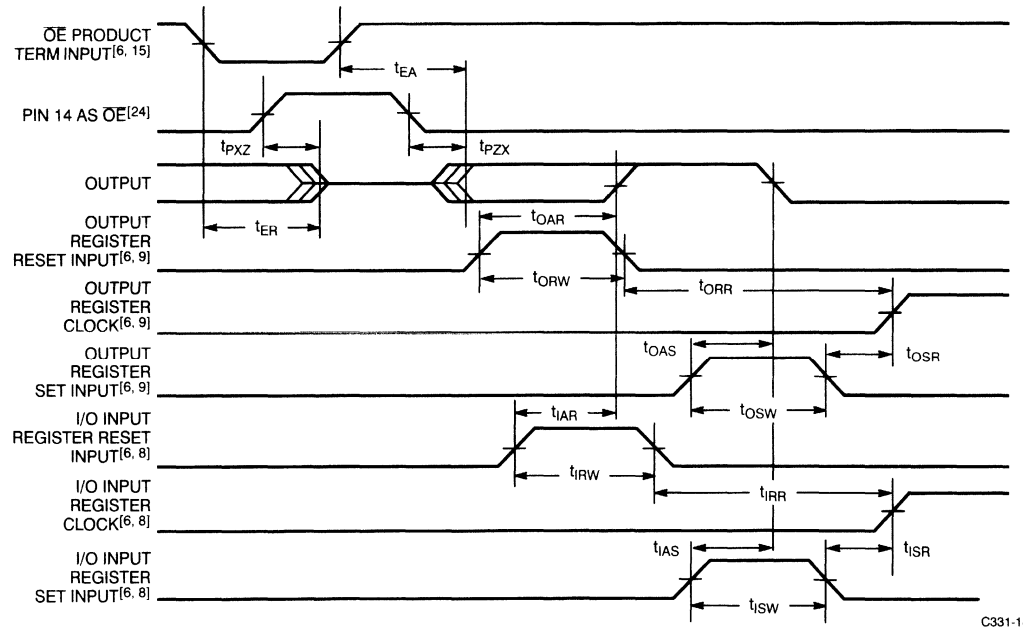
7. Refer to *Figure 3*, configuration 1.
8. Refer to *Figure 3*, configuration 2.
9. Refer to *Figure 3*, configuration 3.
10. Refer to *Figure 3*, configuration 6.
11. Refer to *Figure 3*, configuration 7.
12. Refer to *Figure 3*, configuration 9.
13. This specification is intended to guarantee interface compatibility of the other members of the CY7C330 family with the CY7C331. This specification is met for the devices noted operating at the same ambient temperature and at the same power supply voltage. These parameters are tested periodically by sampling of production product.
14. Part (a) of AC Test Loads and Waveforms used for all parameters except t_{PZXI}, t_{PXZI}, t_{PZX}, and t_{PXZ}, which use part (b). Part (c) shows the test waveforms and measurement levels.
15. Refer to *Figure 3*, configuration 4.
16. Refer to *Figure 3*, configuration 8.
17. This specification is intended to guarantee that a state machine configuration created with internal or external feedback can be operated with output register and input register clocks controlled by the same source. These parameters are tested by periodic sampling of production product.
18. Refer to *Figure 3*, configuration 10.

Switching Characteristics Over the Operating Range[2] (continued)

Parameter	Description	Military						Unit
		−25		−30		−40		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[7]		25		30		40	ns
t_{ICO}	Input Register Clock to Output Delay[4, 8]		45		50		65	ns
t_{IOH}	Output Data Stable Time from Input Clock[4, 8]	5		5		5		ns
t_{IS}	Input or Feedback Set-Up Time to Input Register Clock[8]	5		5		5		ns
t_{IH}	Input Register Hold Time from Input Clock[4, 8]	13		15		20		ns
t_{IAR}	Input to Input Register Asynchronous Reset Delay[4, 8]		45		50		65	ns
t_{IRW}	Input Register Reset Width[8]	45		50		65		ns
t_{IRR}	Input Register Reset Recovery Time[8]	45		50		65		ns
t_{IAS}	Input to Input Register Asynchronous Set Delay[8]		45		50		65	ns
t_{ISW}	Input Register Set Width[8]	45		50		65		ns
t_{ISR}	Input Register Set Recovery Time[8]	45		50		65		ns
t_{WH}	Input and Output Clock Width High[8, 9, 10]	15		20		25		ns
t_{WL}	Input and Output Clock Width Low[8, 9, 10]	15		20		25		ns
f_{MAX1}	Maximum frequency with Feedback in Input Registered Mode $(1/(t_{ICO} + t_{IS}))$[11]	20.0		18.1		14.2		MHz
f_{MAX2}	Maximum frequency Data Path in Input Registered Mode (Lowest of $1/t_{ICO}$, $1/(t_{WH} + t_{WL})$, or $1/(t_{IS} + t_{IH})$[8]	22.2		20.0		15.3		MHz
$t_{IOH} - t_{IH}33X$	Output Data Stable from Input Clock Minus Input Register Input Hold Time for 7C330 and 7C332[12, 13]	0		0		0		ns
t_{CO}	Output Register Clock to Output Delay[9]		25		30		40	ns
t_{OH}	Output Data Stable Time from Output Clock[9]	3		3		3		ns
t_S	Output Register Input Set−Up Time to Output Clock[9]	15		15		20		ns
t_H	Output Register Input Hold Time from Output Clock[9]	10		10		12		ns
t_{OAR}	Input to Output Register Asynchronous Reset Delay[9]		25		30		40	ns
t_{ORW}	Output Register Reset Width[9]	25		30		40		ns
t_{ORR}	Output Register Reset Recovery Time[9]	25		30		40		ns
t_{OAS}	Input to Output Register Asynchronous Set Delay[9]		25		30		40	ns
t_{OSW}	Output Register Set Width[9]	25		30		40		ns
t_{OSR}	Output Register Set Recovery Time[9]	25		30		40		ns
t_{EA}	Input to Output Enable Delay[14, 15]		25		30		40	ns
t_{ER}	Input to Output Disable Delay[14, 15]		25		30		40	ns
t_{PZX}	Pin 14 to Output Enable Delay[14, 15]		20		25		35	ns
t_{PXZ}	Pin 14 to Output Disable Delay[14, 15]		20		25		35	ns
f_{MAX3}	Maximum Frequency with Feedback in Output Registered Mode $)1/(t_{CO} + t_S)$[16, 17]	25.0		22.2		16.6		MHz
f_{MAX4}	Maximum Frequency Data Path in Output Registered Mode (Lowest of $1/t_{CO}$, $1/(t_{WH} + t_{WL})$, or $1/(t_S + t_H)$[9]	33.3		25.0		20.0		MHz
$t_{OH} - t_{IH}33X$	Output Data Stable from Output Clock Minus Input Register Input Hold Time for 7C330 and 7C332[13, 18]	0		0		0		ns
f_{MAX5}	Maximum Frequency Pipelined Mode[10, 17]	28.0		23.5		18.5		MHz

Switching Waveforms





Notes:

19. Output register is set in Transparent mode. Output register set and reset inputs are in a HIGH state.
20. Dedicated input or input register set in Transparent mode. Input register set and reset inputs are in a HIGH state.
21. Combinatorial Mode. Reset and set inputs of the input and output registers should remain in a HIGH state at least until the output responds at t_{PD}. When returning set and reset inputs to a LOW state, one of these signals should go LOW a minimum of t_{OSR} (set input) or t_{ORR} (reset input) prior to the other. This guarantees predictable register states upon exit from Combinatorial mode.
22. When entering the Combinatorial mode, input and output register set and reset inputs must be stable in a HIGH state a minimum of t_{ISR} or t_{IRR} and t_{OSR} or t_{ORR} respectively prior to application of logic input signals.
23. When returning to the input and/or output Registered mode, register set and reset inputs must be stable in a LOW state a minimum of t_{ISR} or t_{IRR} and t_{OSR} or t_{ORR} respectively prior to the application of the register clock input.
24. Refer to *Figure 3*, configuration 5.

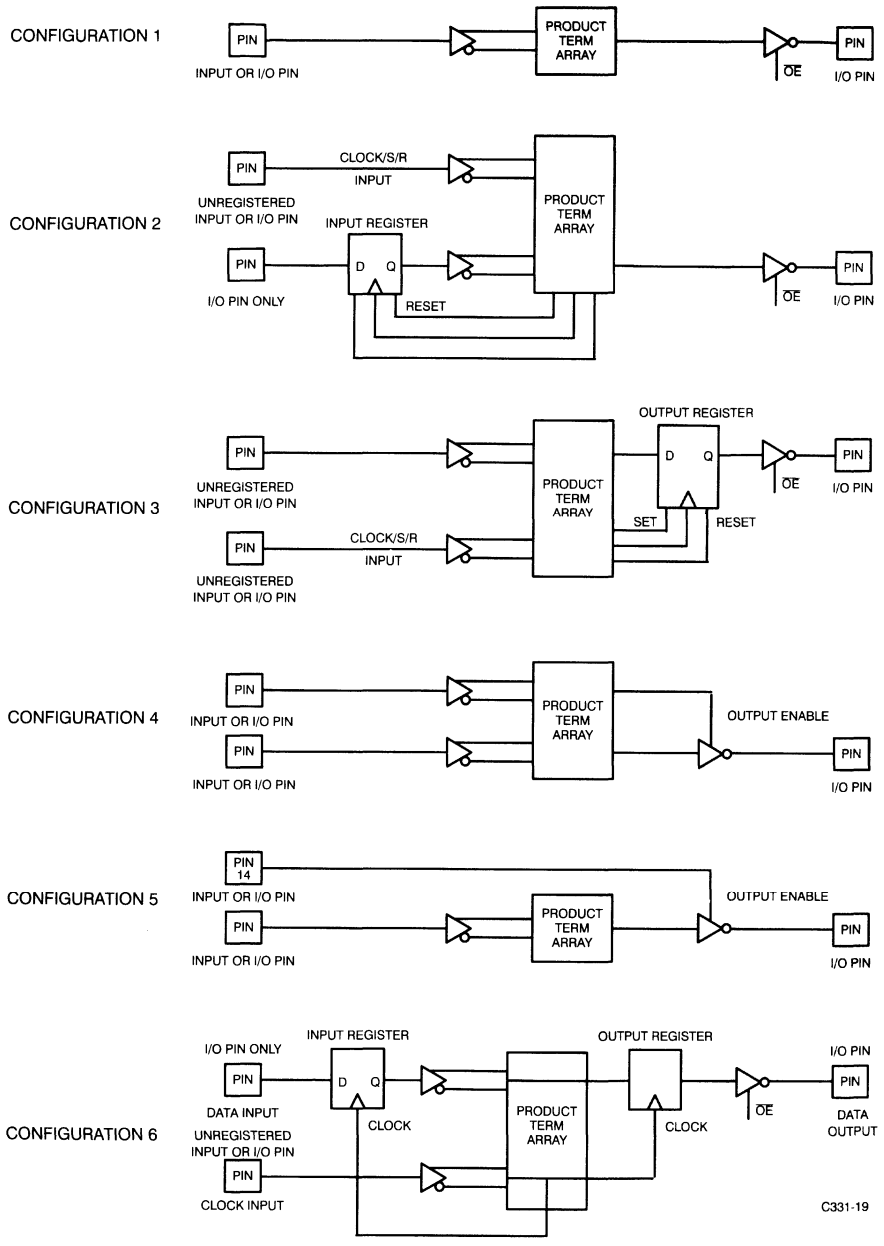
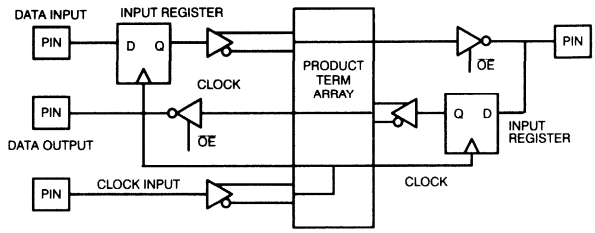
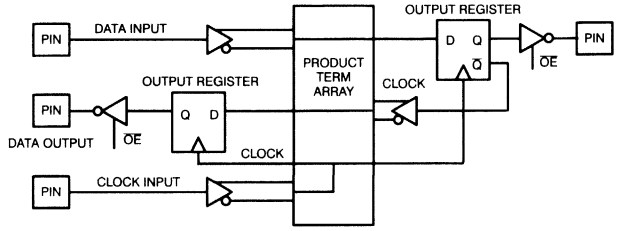


Figure 3. Timing Configurations

CONFIGURATION 7

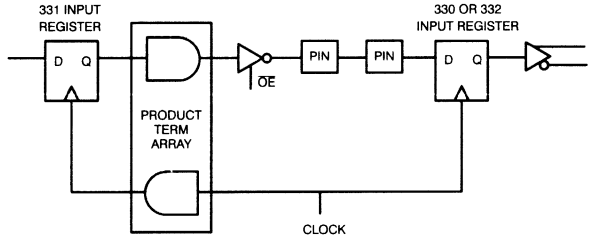


CONFIGURATION 8

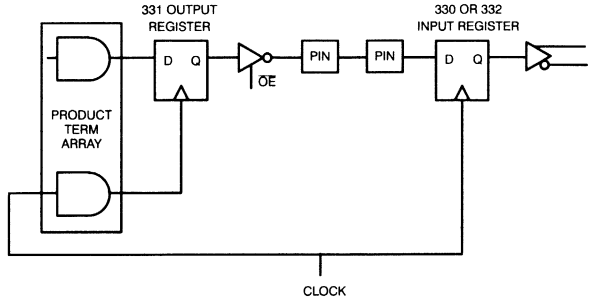


C331-20

CONFIGURATION 9



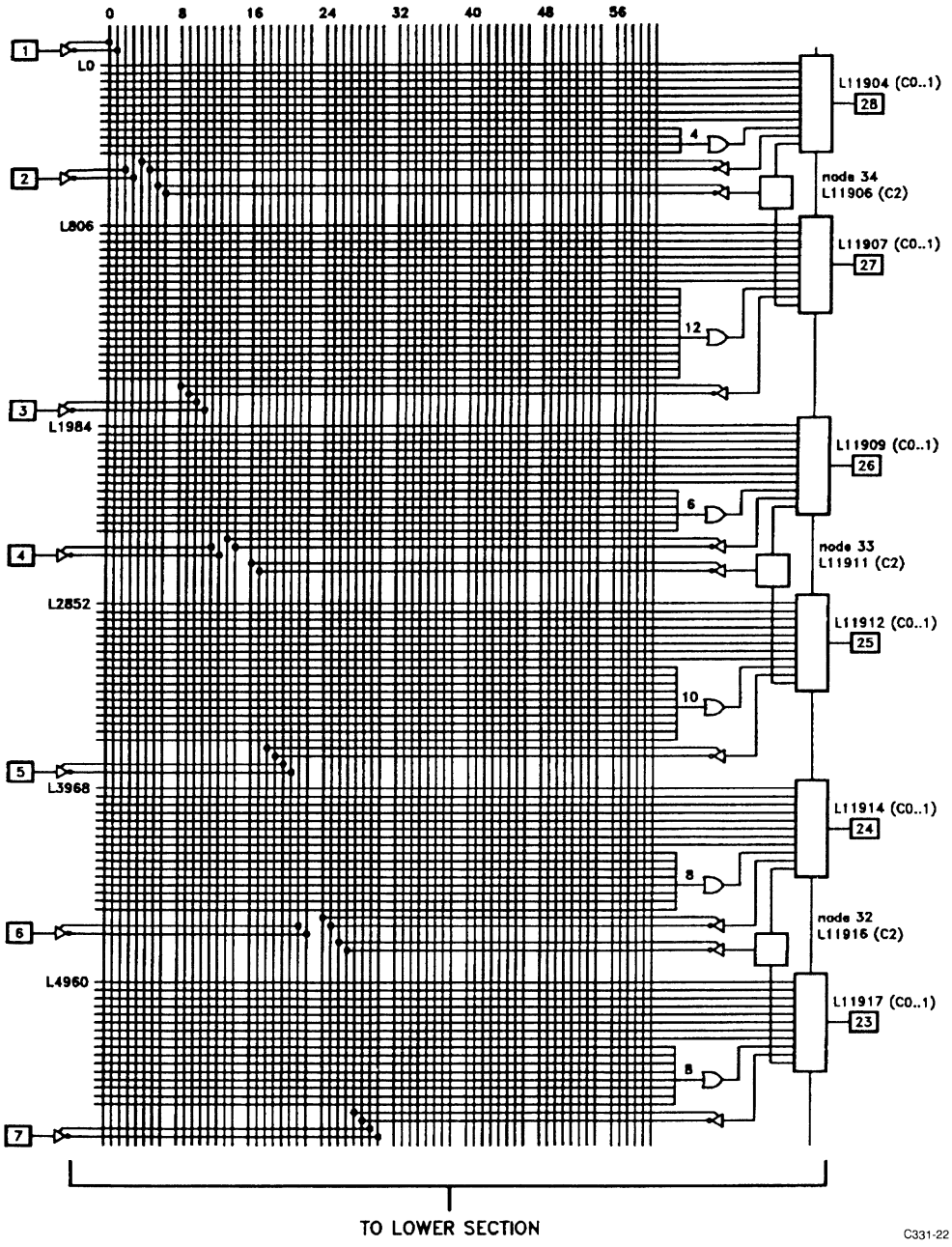
CONFIGURATION 10



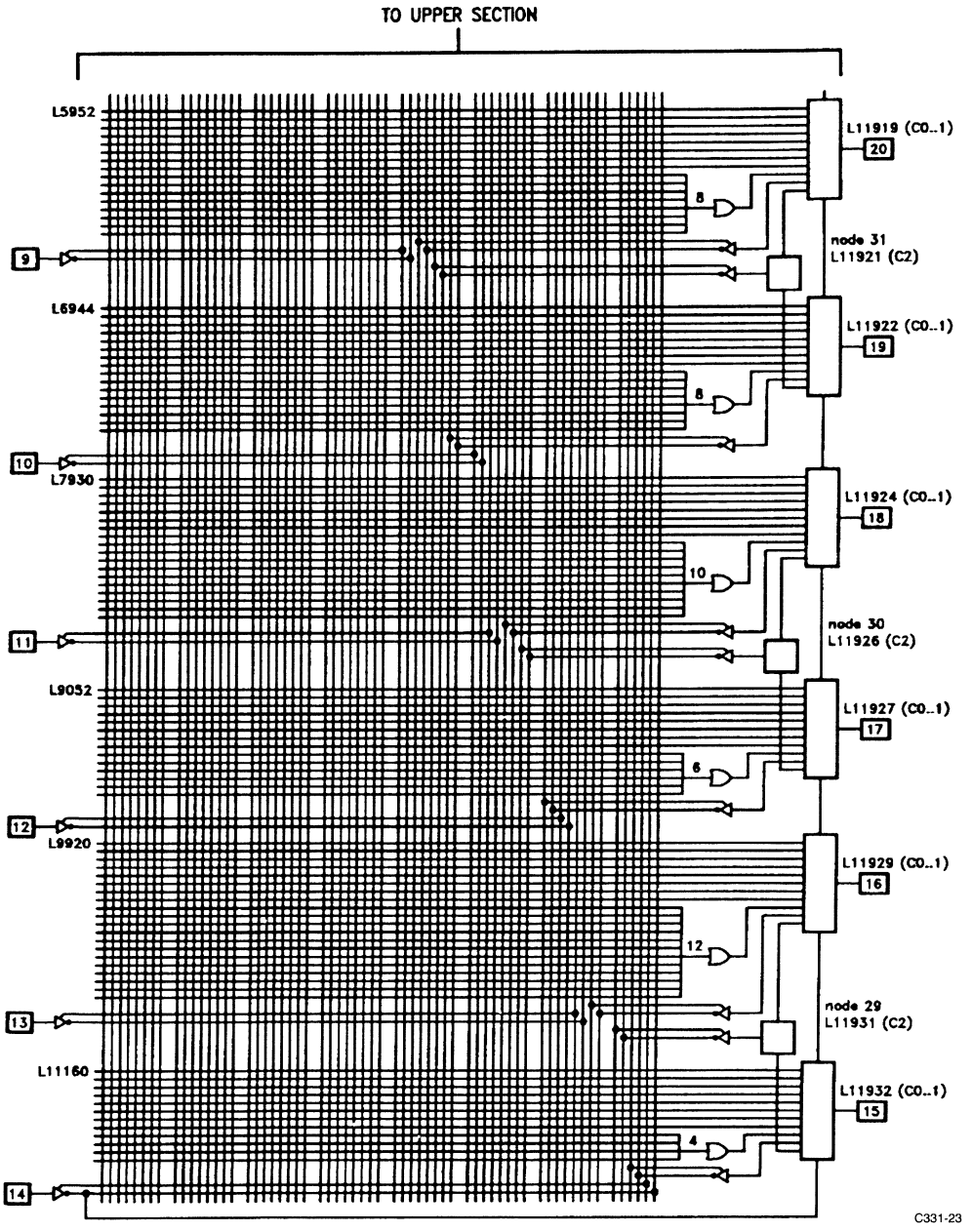
C331-21

Figure 3. Timing Configurations (continued)

CY7C331 Logic Diagram (Upper Half)



CY7C331 Logic Diagram (Lower Half)



Ordering Information

I_{CC1} (mA)	t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package Name	Package Type	Operating Range
130	20	12	20	CY7C331–20HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
				CY7C331–20JC	J64	28-Lead Plastic Leaded Chip Carrier	
				CY7C331–20PC	P21	28-Lead (300-Mil) Molded DIP	
				CY7C331–20WC	W22	28-Lead (300-Mil) Windowed CerDIP	
160	25	15	25	CY7C331–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
				CY7C331–25HMB	H64	28-Pin Windowed Leaded Chip Carrier	
				CY7C331–25LMB	L64	28-Square Leadless Chip Carrier	
				CY7C331–25QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
				CY7C331–25TMB	T74	28-Lead Windowed Cerpack	
				CY7C331–25WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
120	25	12	25	CY7C331–25HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
				CY7C331–25JC	J64	28-Lead Plastic Leaded Chip Carrier	
				CY7C331–25PC	P21	28-Lead (300-Mil) Molded DIP	
				CY7C331–25WC	W22	28-Lead (300-Mil) Windowed CerDIP	
150	30	15	30	CY7C331–30DMB	D22	28-Lead (300-Mil) CerDIP	Military
				CY7C331–30HMB	H64	28-Pin Windowed Leaded Chip Carrier	
				CY7C331–30LMB	L64	28-Square Leadless Chip Carrier	
				CY7C331–30QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
				CY7C331–30TMB	T74	28-Lead Windowed Cerpack	
				CY7C331–30WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
150	40	20	40	CY7C331–40DMB	D22	28-Lead (300-Mil) CerDIP	Military
				CY7C331–40HMB	H64	28-Pin Windowed Leaded Chip Carrier	
				CY7C331–40LMB	L64	28-Square Leadless Chip Carrier	
				CY7C331–40QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
				CY7C331–40TMB	T74	28-Lead Windowed Cerpack	
				CY7C331–40WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{IS}	9, 10, 11
t_{IH}	9, 10, 11
t_{WH}	9, 10, 11
t_{WL}	9, 10, 11
t_{CO}	9, 10, 11
t_{PD}	9, 10, 11
t_{IAR}	9, 10, 11
t_{IAS}	9, 10, 11
t_{PXZ}	9, 10, 11
t_{PZX}	9, 10, 11
t_{ER}	9, 10, 11
t_{EA}	9, 10, 11
t_{S}	9, 10, 11
t_{H}	9, 10, 11

Document #: 38-00066-D

CY7C332

Registered Combinatorial EPLD

Features

- 12 I/O macrocells each having:
  - Registered, latched, or transparent array input
  - A choice of two clock sources
  - Global or local output enable (OE)
  - Up to 19 product terms (PTs) per output
  - Product term (PT) output polarity control
- 192 product terms with variable distribution to macrocells
  - An average of 14 PTs per macrocell sum node
- Two clock inputs with configurable polarity control
- 13 input macrocells, each having:
  - Complementary input
  - Register, latch, or transparent access
  - Two clock sources
- 15 ns t_{PD} max.
- Low power
  - 120 mA typical I_{CC} quiescent
  - 180 mA max.
  - Power-saving "Miser Bit" feature
- Security fuse
- 28-pin slim-line package; also available in 28-pin PLCC
- UV-erasable and reprogrammable
- Programming and operation 100% testable

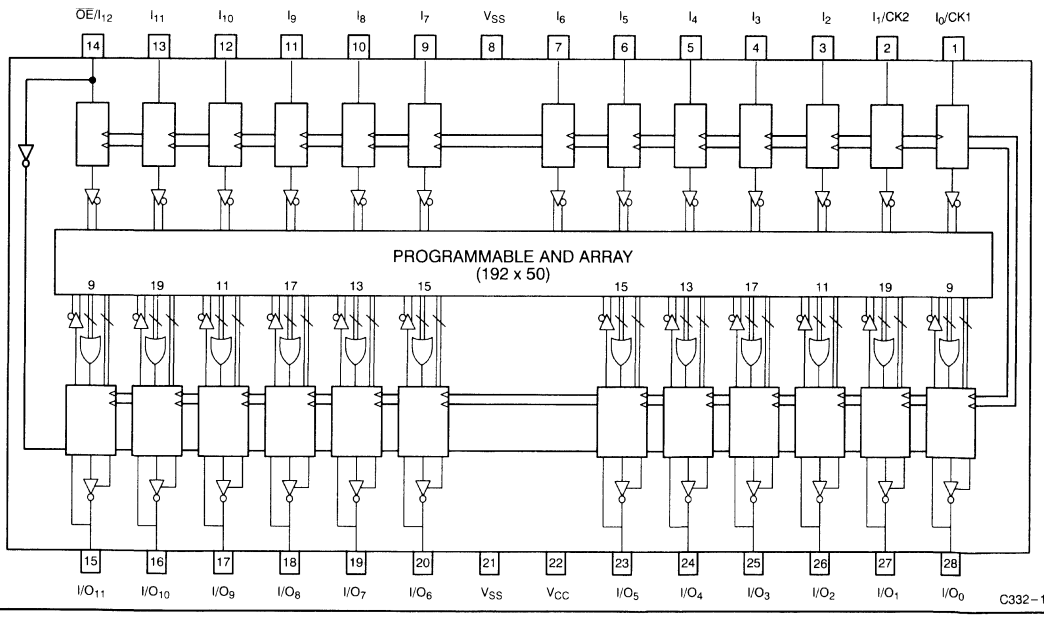
Functional Description

The CY7C332 is a versatile combinatorial PLD with I/O registers on-board. There are 25 array inputs; each has a macrocell that may be configured as a register, latch, or simple buffer. Outputs have polarity and three-state control product terms. The allocation of product terms to I/O macrocells is varied so that functions of up to 19 product terms can be accommodated.

I/O Resources

Pins 1 through 7 and 9 through 14 function as dedicated array inputs. Pins 1 and 2 function as input clocks as well as normal inputs. Pin 14 functions as a global output enable as well as a normal input.

Logic Block Diagram

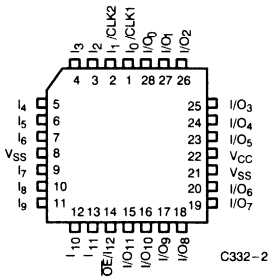


Selection Guide

Generic Part Number	I_{CC1} (mA)		t_{ICO}/t_{PD} (ns)		t_{IS} (ns)	
	Commercial	Military	Commercial	Military	Commercial	Military
7C332-15	130		18/15		3	
7C332-20	120	160	20	23/20	3	4
7C332-25	120	150	25	25	3	4
7C332-30		150		30		4

Pin Configuration

LCC/PLCC
Top View



I/O Resources (continued)

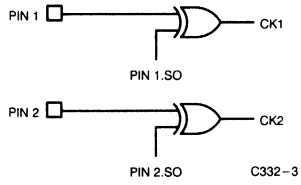
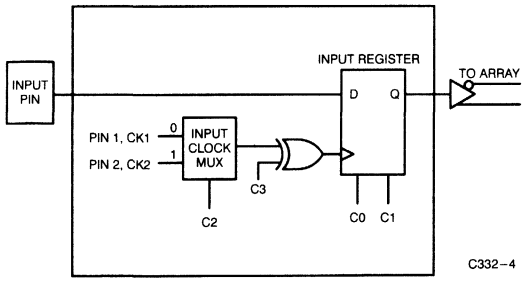


Figure 1. CK1 and CK2

Pins 15 through 20 and 23 through 28 are connected to I/O macrocells and may be combinatorial outputs as well as registered or direct inputs.

Input Macrocell



C3	C2	C1	C0	Input Register Option
X	X	0	0	Combinatorial
X	X	0	1	Illegal
0	0	1	1	Registered, CLK1, Rising Edge
0	1	1	1	Registered, CLK2, Rising Edge
1	0	1	1	Registered, CLK1, Falling Edge
1	1	1	1	Registered, CLK2, Falling Edge
0	0	1	0	Latched, CLK1, LOW Transparent
0	1	1	0	Latched, CLK2, LOW Transparent
1	0	1	0	Latched, CLK1, HIGH Transparent
1	1	1	0	Latched, CLK2, HIGH Transparent

Figure 2. Input Macrocell

There are 13 input macrocells, corresponding to pins 1 through 7 and 9 through 14. Each macrocell has a clock that is selected to come from either pin 1 or pin 2 by configuration bit C2. Pins 1 and 2 are clocks as well as normal inputs. There is no C2 configuration bit for either of these two input macrocells. Macrocells connected to pins 1 and 2 do not have a clock choice, but each has a clock coming from the other pin.

Each input macrocell can be configured as a register, latch, or simple buffer (transparent path) to the product term array. For a register the configuration bit, C0, is 1 (programmed) and C1 is 1. For a latch, C0 is 0 and C1 is 1. If both C0 and C1 are 0 (unprogrammed), then the macrocell is completely transparent.

Configuration bit C3 determines the clock edge on which the register is triggered or the polarity for which the latch is asserted. This clock polarity can be programmed independently for each input register. These confirmation options are available on all inputs, including those in the I/O macrocell.

If C3 is 0 (unprogrammed), the clock will be rising-edge triggered (register mode) or HIGH asserted (latch mode). If C3 is 1 (programmed), the clock will be falling-edge triggered (register mode) or LOW asserted (latch mode).

I/O Macrocell

There are 12 I/O macrocells corresponding to pins 15 through 20 and 23 through 28. Each macrocell has a three-state output control and XOR product term to dynamically control polarity, and a configurable feedback path.

For each I/O macrocell, the three-state control for the output may be configured two ways. If the configuration bit, C4, is a 1 (programmed), then the global OE signal is selected. Otherwise, the OE product term is used.

For each I/O macrocell, the input/feedback path may be configured as a register, latch, or shunt. There are two configuration bits per I/O macrocell that configure the feedback path. These are programmed in the same way as for the input macrocells.

For each I/O macrocell, the input register clock (or Latch Enable) that is used for the input/feedback path may be selected as pin 1 (select bit, C2, not programmed) or pin 2 (select bit, C2, programmed).

Array Allocation to Output Macrocell

The number of product terms in each output macrocell sum is position dependent. *Table 1* summarizes the allocation.

Table 1. Product Term Allocation in Output Macrocell

Macrocell	Pin Number	Product Term
0	28	9
1	27	19
2	26	11
3	25	17
4	24	13
5	23	15
6	20	15
7	19	13
8	18	17
9	17	11
10	16	19
11	15	9

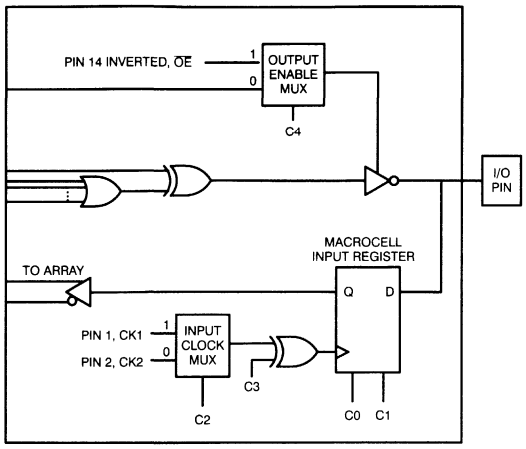


Figure 3. I/O Macrocell

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 22 to Pins 8 and 21) ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (LOW) ..... 12 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

DC Programming Voltage 13.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = − 3.2 mA	Commercial	2.4		V
			I_{OH} = − 2 mA	Military			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12 mA	Commercial		0.5	V
			I_{OL} = 8 mA	Military			
V_{IH}	Input HIGH Voltage	Guaranteed HIGH Input, all Inputs[2]			2.2		V
V_{IL}	Input LOW Voltage	Guaranteed LOW Input, all Inputs[2]				0.8	V
I_{IX}	Input Leakage Current	V_{SS} < V_{IN} < V_{CC}, V_{CC} = Max.			−10	+10	μA
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{SS} < V_{OUT} < V_{CC},			−40	+40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[3]			−30	−90	mA
I_{CC1}	Standby Power Supply Current	V_{CC} = Max., V_{IN} = GND Outputs Open		Commercial		120	mA
				Commercial −15		130	
				Military		150	
				Military −20		160	
I_{CC2}	Power Supply Current at Frequency[4, 5]	V_{CC} = Max. Outputs Disabled (In High Z State) Device Operating at f_{MAX} External (f_{MAX1})		Commercial		180	mA
				Military		200	

Notes:

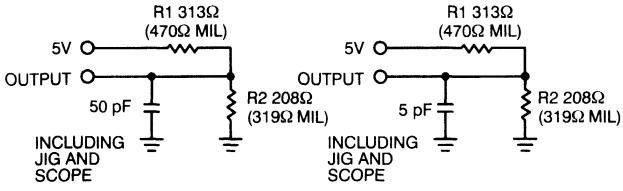
1. T_A is the "instant on" case temperature.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. Tested by periodic sampling of production product.
5. Refer to *Figure 4* configuration 2.

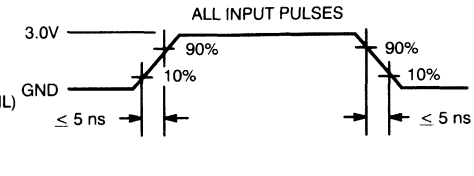
Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V at f = 1 MHz,	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V at f = 1 MHz,	10	pF

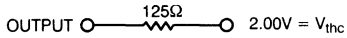
Note:
6. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

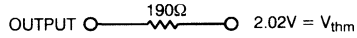


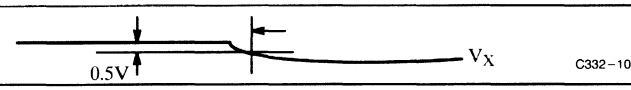
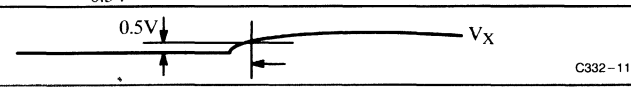
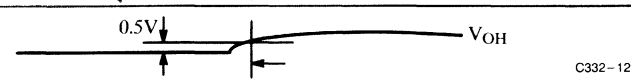
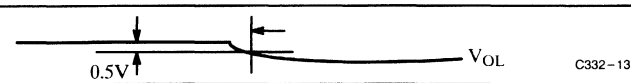
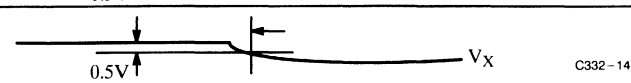
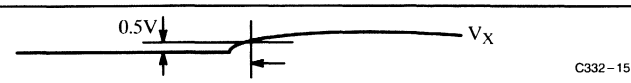
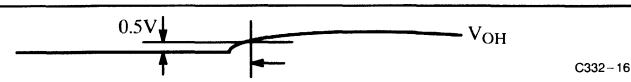
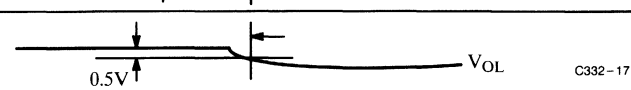


Equivalent to: THÉVENIN EQUIVALENT (Commercial)



Equivalent to: THÉVENIN EQUIVALENT (Military)



Parameter	V_X	Output Waveform—Measurement Level
$t_{PXZ(-)}$	1.5V	 C332-10
$t_{PXZ(+)}$	2.6V	 C332-11
$t_{PZX(+)}$	V_{thc}	 C332-12
$t_{PZX(-)}$	V_{thc}	 C332-13
$t_{ER(-)}$	1.5V	 C332-14
$t_{ER(+)}$	2.6V	 C332-15
$t_{EA(+)}$	V_{thc}	 C332-16
$t_{EA(-)}$	V_{thc}	 C332-17

(c) Test Waveforms and Measurement Levels

Switching Characteristics Over the Operating Range[2]

Parameter	Description	Commercial						Military						Unit
		−15[7]		−20		−25		−20[7]		−25		−30		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[8]		15		20		25		20		25		30	ns
t_{ICO}	Input Register Clock to Output Delay[9]		18		20		25		23		25		30	ns
t_{IS}	Input or Feedback Set-Up Time to Input Register Clock[9]	3		3		3		4		4		4		ns
t_{IH}	Input Register Hold Time[9]	3		3		3		4		4		4		ns
t_{EA}	Input to Output Enable Delay[10, 11]		20		20		25		25		25		30	ns
t_{ER}	Input to Output Disable Delay[10, 11]		20		20		25		25		25		30	ns
t_{PZX}	Pin 14 Enable to Output Enable Delay[8, 12]		15		15		20		20		20		25	ns
t_{PXZ}	Pin 14 Disable to Output Disable Delay[8, 12]		15		15		20		20		20		25	ns
t_{WH}	Input Clock Width High[4, 9]	9		10		10		10		10		12		ns
t_{WL}	Input Clock Width Low[4, 9]	9		10		10		10		10		12		ns
t_{IOH}	Output Data Stable Time from Input Register Clock Input[7, 9]	3		3		3		3		4		4		ns
$t_{IOH} - t_{IH}$	Output Data Stable Time This Device Minus I/P Reg Hold Time Same Device[7, 13, 14]	0		0		0		0		0		0		ns
$t_{IOH} - t_{IH}$ 33x	Output Data Stable Time Minus I/P Reg Hold Time 7C330 and 7C332 Device[9, 15]	0		0		0		0		0		0		ns
t_{PE}	External Clock Period ($t_{ICO} + t_{IS}$)[9]	21		23		28		27		29		34		ns
f_{MAX1}	Maximum External Operating Frequency ($1/(t_{ICO} + t_{IS})$)[9]	47.6		43.4		35.7		37		34.4		29.4		MHz
f_{MAX}	Maximum Frequency Data Path[9]	55.5		50.0		40.0		50.0		40.0		33.3		MHz

Notes:

7. Preliminary specifications.
8. Refer to *Figure 4* configuration 1.
9. Refer to *Figure 4* configuration 2.
10. Part (a) of AC Test Loads and Waveforms is used for all parameters except t_{EA}, t_{ER}, t_{PZX}, and t_{PXZ}, which use part (b). Part (c) shows test waveform and measurement reference levels.
11. Refer to *Figure 4* configuration 3.
12. Refer to *Figure 4* configuration 4.
13. Refer to *Figure 4* configuration 5.
14. This specification is intended to guarantee that configuration 5 of *Figure 4* with input registered feedback can be operated with all input register clocks controlled by the same source. These parameters are tested by periodic sampling of production product.
15. This specification is intended to guarantee interface compatibility of the other members of the CY7C330 family with the CY7C332. This specification is met for the devices noted operating at the same ambient temperature and at the same power supply voltage. These parameters are tested periodically by sampling of production product.

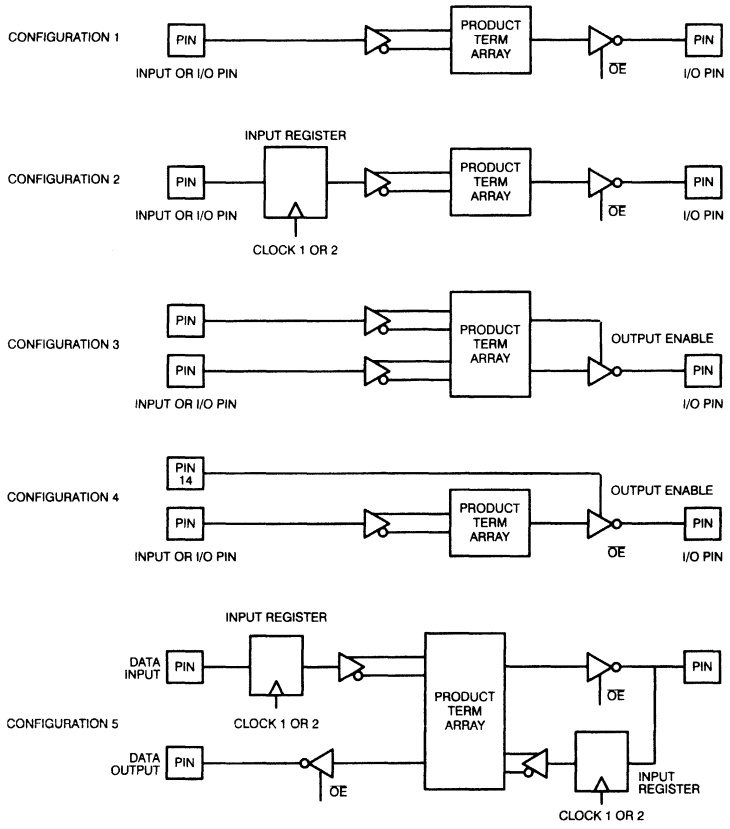
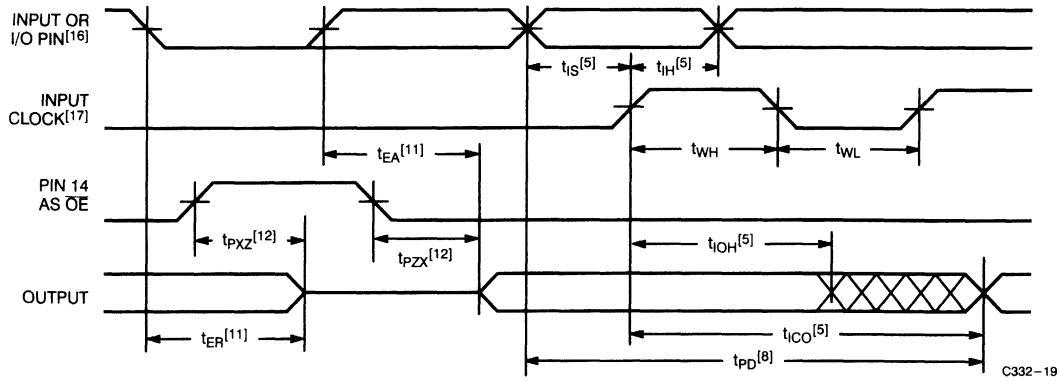


Figure 4. Timing Configurations

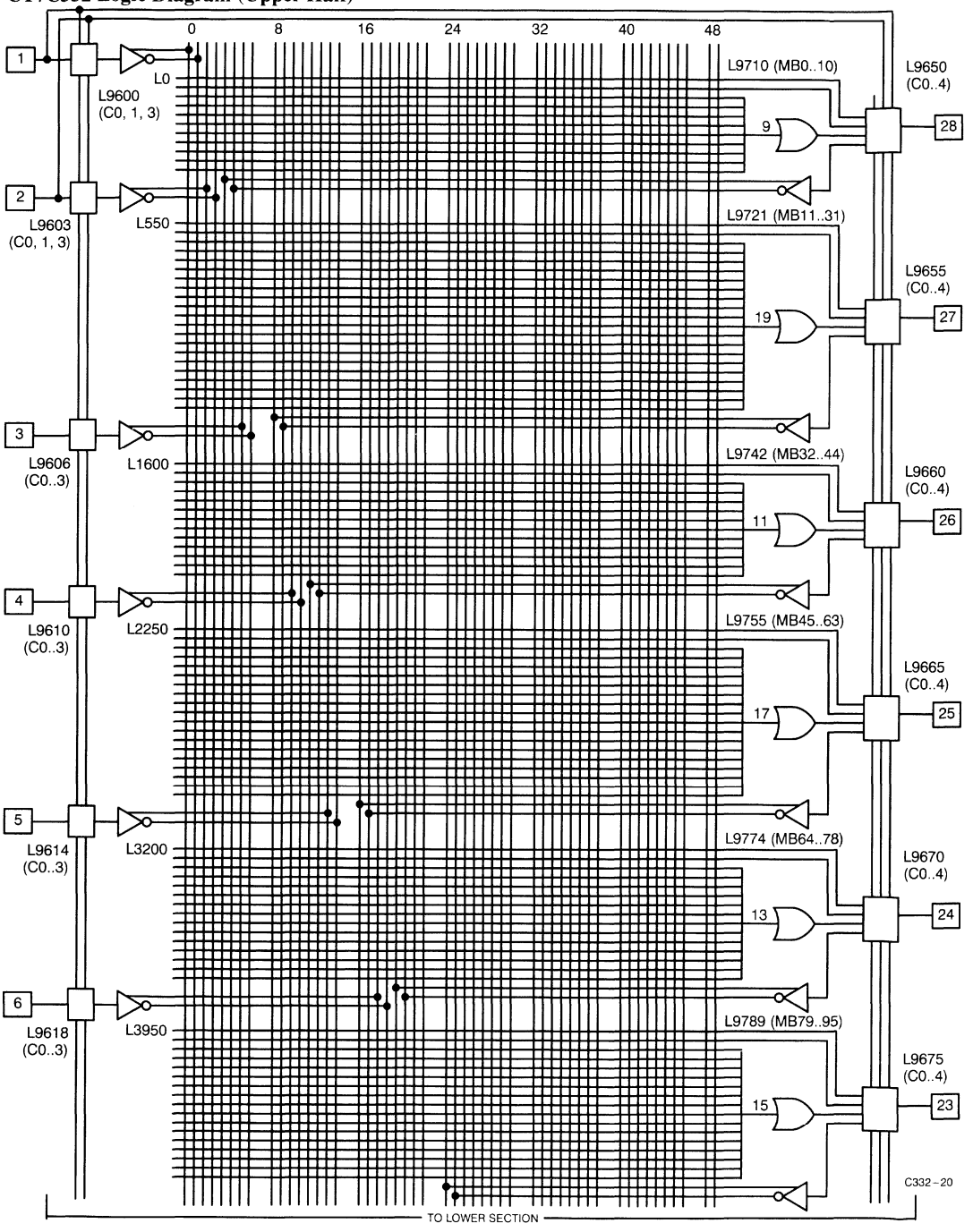
Switching Waveforms



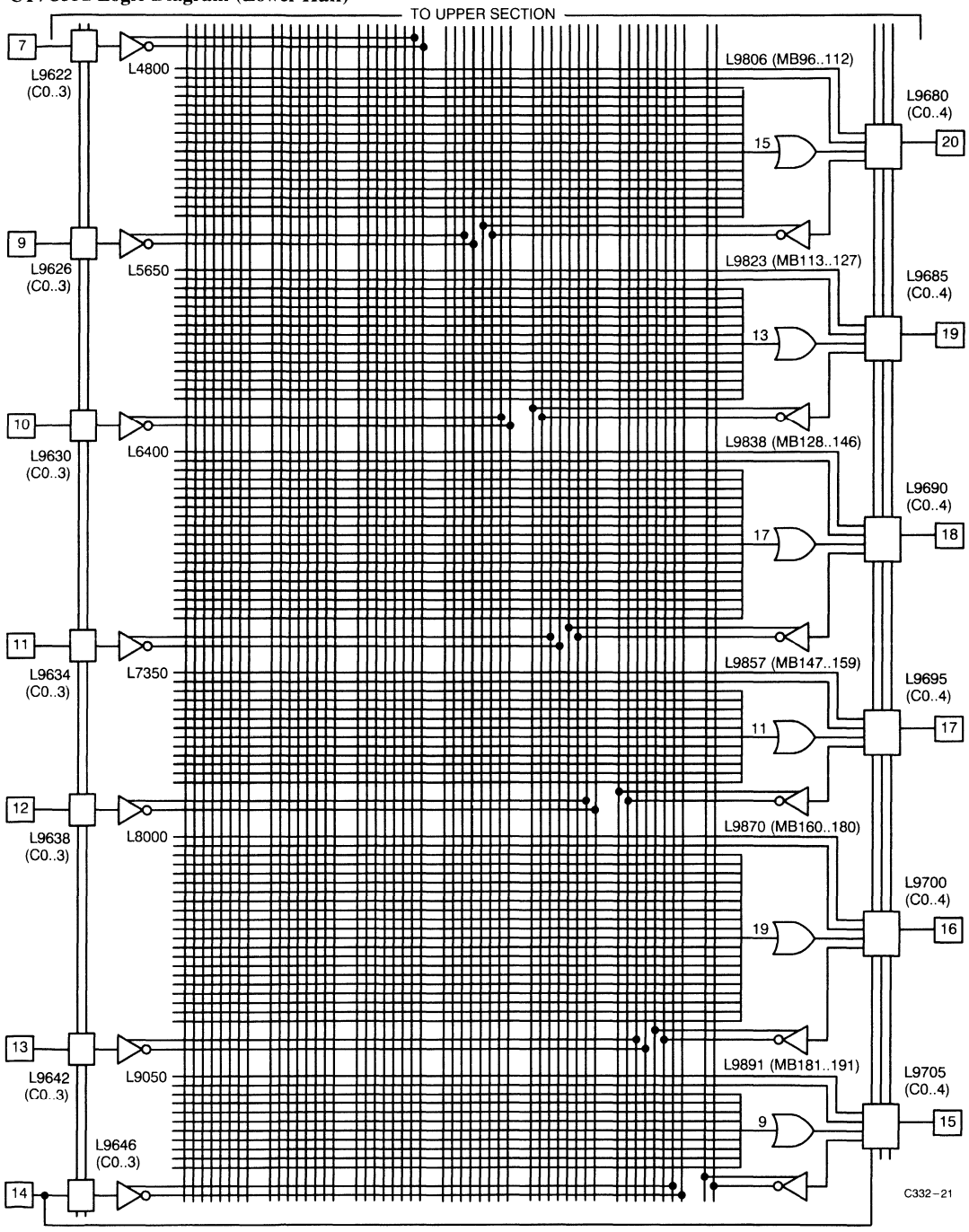
Notes:

16. Because OE can be controlled by the $\overline{OE}$ product term, input signal polarity for control of OE can be of either polarity. Internally the product term $\overline{OE}$ signal is active HIGH.
17. Since the input register clock polarity is programmable, the input clock may be rising- or falling-edge triggered.

CY7C332 Logic Diagram (Upper Half)



CY7C332 Logic Diagram (Lower Half)



Ordering Information

I_{CC1} (max)	t_{ICO}/t_{PD} (ns)	t_{IS} (ns)	t_{IH} (ns)	Ordering Code	Package Name	Package Type	Operating Range
120	18/15	3	3	CY7C332-15HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
				CY7C332-15JC	J64	28-Lead Plastic Leaded Chip Carrier	
				CY7C332-15PC	P21	28-Lead (300-Mil) Molded DIP	
				CY7C332-15WC	W22	28-Lead (300-Mil) Windowed CerDIP	
120	20	3	3	CY7C332-20HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
				CY7C332-20JC	J64	28-Lead Plastic Leaded Chip Carrier	
				CY7C332-20PC	P21	28-Lead (300-Mil) Molded DIP	
				CY7C332-20WC	W22	28-Lead (300-Mil) Windowed CerDIP	
160	23/20	4	4	CY7C332-20DMB	D22	28-Lead (300-Mil) CerDIP	Military
				CY7C332-20HMB	H64	28-Pin Windowed Leaded Chip Carrier	
				CY7C332-20LMB	L64	28-Square Leadless Chip Carrier	
				CY7C332-20TMB	T74	28-Lead Windowed Cerpack	
				CY7C332-20WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
120	25	3	3	CY7C332-25HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
				CY7C332-25JC	J64	28-Lead Plastic Leaded Chip Carrier	
				CY7C332-25PC	P21	28-Lead (300-Mil) Molded DIP	
				CY7C332-25WC	W22	28-Lead (300-Mil) Windowed CerDIP	
150	25	4	4	CY7C332-25DMB	D22	28-Lead (300-Mil) CerDIP	Military
				CY7C332-25HMB	H64	28-Pin Windowed Leaded Chip Carrier	
				CY7C332-25LMB	L64	28-Square Leadless Chip Carrier	
				CY7C332-25TMB	T74	28-Lead Windowed Cerpack	
				CY7C332-25WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
150	30	4	4	CY7C332-30DMB	D22	28-Lead (300-Mil) CerDIP	Military
				CY7C332-30HMB	H64	28-Pin Windowed Leaded Chip Carrier	
				CY7C332-30LMB	L64	28-Square Leadless Chip Carrier	
				CY7C332-30TMB	T74	28-Lead Windowed Cerpack	
				CY7C332-30WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{IS}	9, 10, 11
t_{IH}	9, 10, 11
t_{ICO}	9, 10, 11
t_{PD}	9, 10, 11
t_{PXZ}	9, 10, 11
t_{PZX}	9, 10, 11
t_{ER}	9, 10, 11
t_{EA}	9, 10, 11

Document #: 38–00067–D

CY7C335

Universal Synchronous EPLD

Features

- **100-MHz output registered operation**
- **Twelve I/O macrocells, each having:**
  - **— Registered, three-state I/O pins**
  - **— Input and output register clock select multiplexer**
  - **— Feed back multiplexer**
  - **— Output enable ($\overline{OE}$) multiplexer**
- **Bypass on input and output registers**
- **All twelve macrocell state registers can be hidden**
- **User configurable I/O macrocells to implement JK or RS flip-flops and T or D registers**
- **Input multiplexer per pair of I/O macrocells allows I/O pin associated with a hidden macrocell state register to be saved for use as an input**
- **Four dedicated hidden registers**
- **Twelve dedicated registered inputs with individually programmable bypass option**
- **Three separate clocks—two input clocks, two output clocks**
- **Common (pin 14—controlled) or product term—controlled output enable for each I/O pin**
- **256 product terms—32 per pair of macrocells, variable distribution**
- **Global, synchronous, product term—controlled, state register set and reset—inputs to product term are clocked by input clock**
  - **— 2-ns input set-up and 9-ns output register clock to output**
  - **— 10-ns input register clock to state register clock**
- **28-pin, 300-mil DIP, LCC, PLCC**
- **Erasable and reprogrammable**
- **Programmable security bit**

Functional Description

The CY7C335 is a high-performance, erasable, programmable logic device (EPLD) whose architecture has been optimized to enable the user to easily and efficiently construct very high performance state machines.

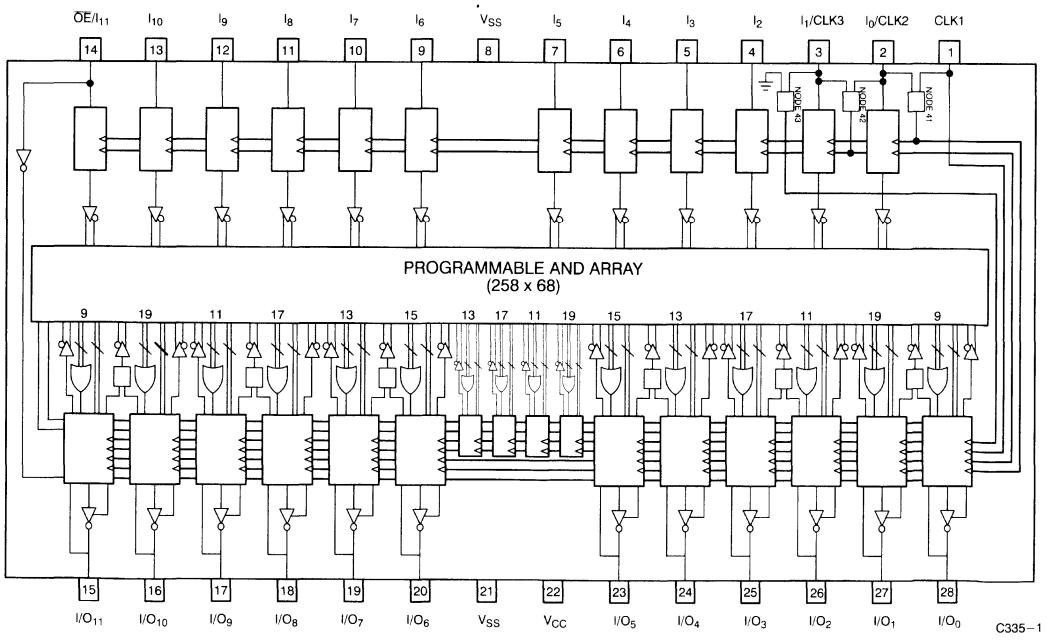
The architecture of the CY7C335, consisting of the user-configurable output macrocell, bidirectional I/O capability, input registers, and three separate clocks, enables the user to design high-performance state machines that can communicate either with each other or with microprocessors over bidirectional parallel buses of user-definable widths.

The four clocks permit independent, synchronous state machines to be synchronized to each other.

The user-configurable macrocells enable the designer to designate JK-, RS-, T-, or D-type devices so that the number of product terms required to implement the logic is minimized.

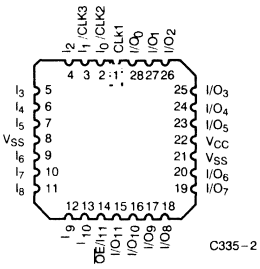
The CY7C335 is available in a wide variety of packages including 28-pin, 300-mil plastic and ceramic DIPs, PLCCs, and LCCs.

Logic Block Diagram



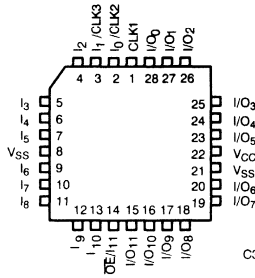
Pin Configurations

LCC
Top View



C335-2

PLCC
Top View



C335-3

Selection Guide

		CY7C335-100	CY7C335-83	CY7C335-66	CY7C335-50	CY7C335-40
Maximum Operating Frequency (MHz)	Commercial	100	83.3	66.6	50	
	Military		83.3	66.6	50	40.0
I_{CC1} (mA)	Commercial	140	140	140	140	
	Military		160	160	160	160

Architecture Configuration Bits

The architecture configuration bits are used to program the multiplexers. The function of the architecture bits is outlined in *Table 1.*

Table 1. Architecture Configuration Bits

Architecture Configuration Bit		Number of Bits	Value	Function
C0	Output Enable Select MUX	12 Bits, 1 Per I/O Macrocell	0—Virgin State	Output Enable Controlled by Product Term
			1—Programmed	Output Enable Controlled by Pin 14
C1	State Register Feed Back MUX	12 Bits, 1 Per I/O Macrocell	0—Virgin State	State Register Output is Fed Back to Input Array
			1—Programmed	I/O Macrocell is Configured as an Input and Output of Input Path is Fed to Array
C2	I/O Macrocell Input Register Clock Select MUX	12 Bits, 1 Per I/O Macrocell	0—Virgin State	ICLK1 Controls the Input Register I/O Macrocell Input Register Clock Input
			1—Programmed	ICLK2 Controls the Input Register I/O Macrocell Input Register Clock Input
C3	Input Register Bypass MUX—I/O Macrocell	12 Bits, 1 Per I/O Macrocell	0—Virgin State	Selects Input to Feedback MUX from Input Register
			1—Programmed	Selects Input to Feedback MUX from I/O pin
C4	Output Register Bypass MUX	12 Bits, 1 Per I/O Macrocell	0—Virgin State	Selects Output from the State Register
			1—Programmed	Selects Output from the Array, Bypassing the State Register
C5	State Clock MUX	16 Bits, 1 Per I/O Macrocell and 1 Per Hidden Macrocell	0—Virgin State	State Clock 1 Controls the State Register
			1—Programmed	State Clock 2 Controls the State Register
C6	Dedicated Input Register Clock Select MUX	12 Bits, 1 Per Dedicated Input Cell	0—Virgin State	ICLK1 Controls the Input Register I/O Macrocell Dedicated Input Register Clock Input
			1—Programmed	ICLK2 Controls the Input Register I/O Macrocell Dedicated Input Register Clock Input

Table 1. Architecture Configuration Bits (continued)

Architecture Configuration Bit		Number of Bits	Value	Function
C7	Input Register Bypass MUX—Input Cell	12 Bits, 1 Per Dedicated Input Cell	0—Virgin State	Selects Input to Array from Input Register
			1—Programmed	Selects Input to Array from Input Pin
C8	ICLK2 Select MUX	1 Bit	0—Virgin State	Input Clock 2 Controlled by Pin 2
			1—Programmed	Input Clock 2 Controlled by Pin 3
C9	ICLK1 Select MUX	1 Bit	0—Virgin State	Input Clock 1 Controlled by Pin 2
			1—Programmed	Input Clock 1 Controlled by Pin 1
C10	SCLK2 Select MUX	1 Bit	0—Virgin State	State Clock 2 Grounded
			1—Programmed	State Clock 2 Controlled by Pin 3
CX (11–16)	I/O Macrocell Pair Input Select MUX	6 Bits, 1 Per I/O Macrocell Pair	0—Virgin State	Selects Data from I/O Macrocell Input Path of Macrocell A of Macrocell Pair
			1—Programmed	Selects Data from I/O Macrocell Input Path of Macrocell B of Macrocell Pair

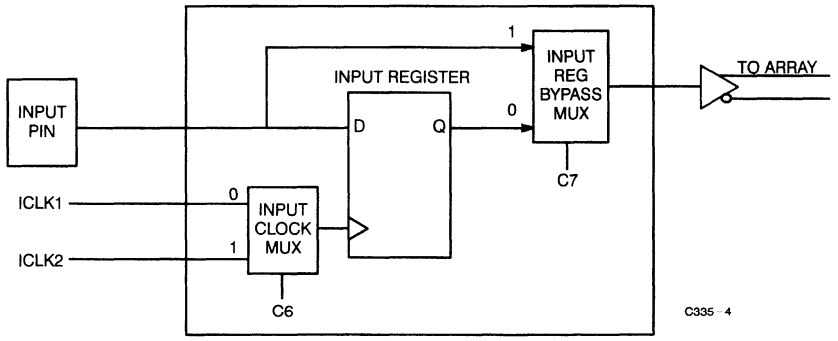


Figure 1. CY7C335 Input Macrocell

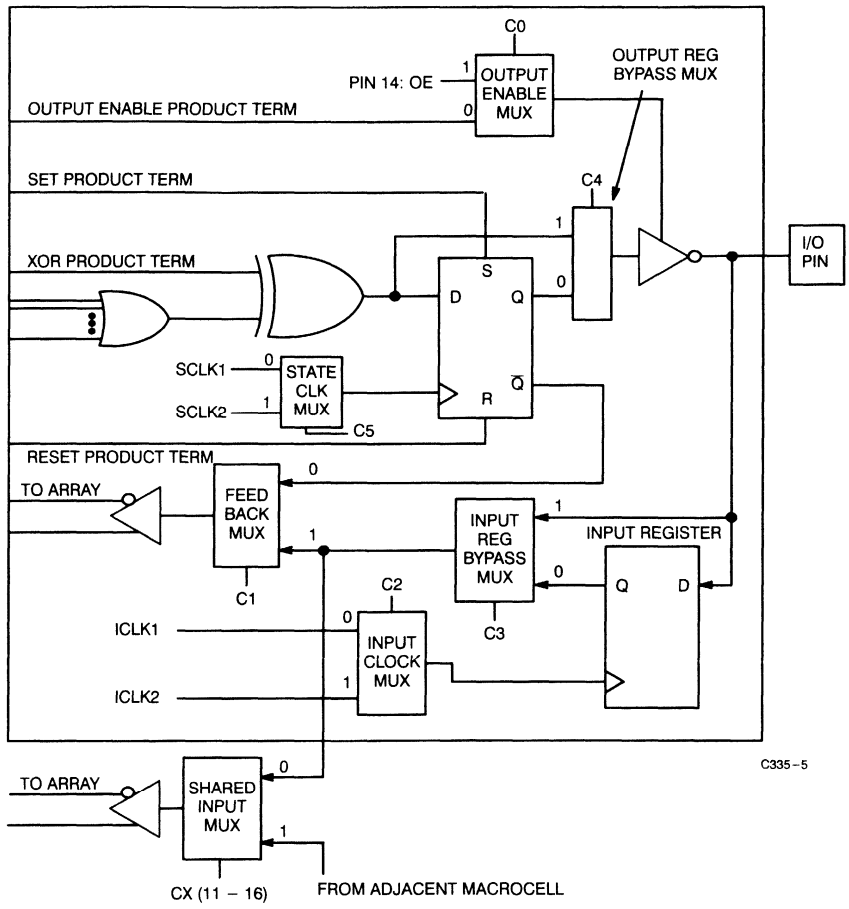


Figure 2. CY7C335 Input/Output Macrocell

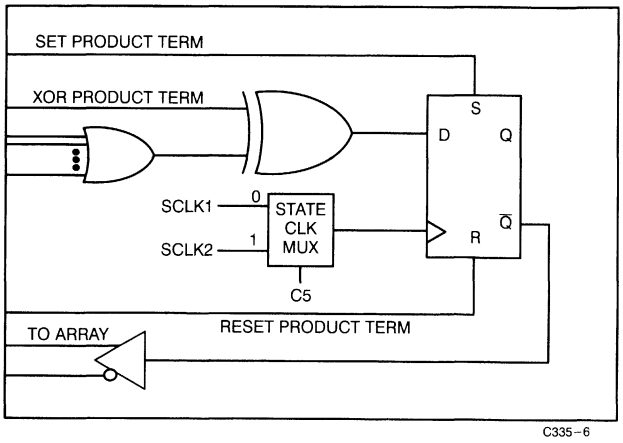


Figure 3. CY7C335 Hidden Macrocell

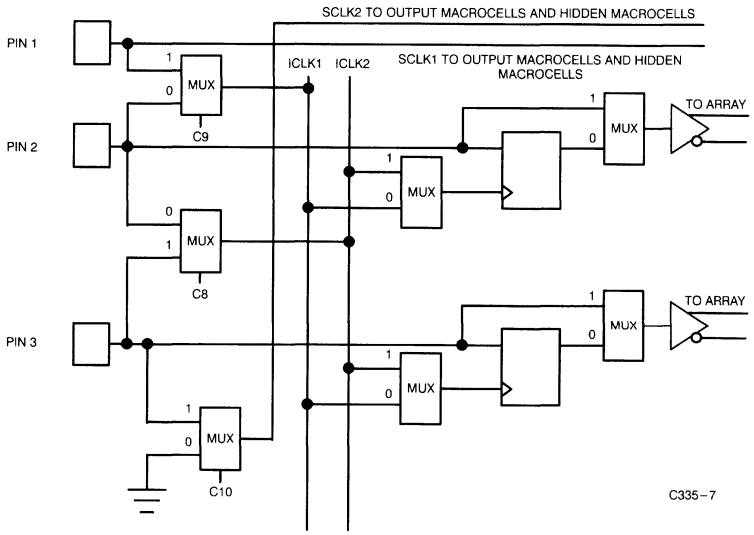


Figure 4. CY7C335 Input Clocking Scheme

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 22 to Pins 8 and 21) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (Low) ..... 12 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

DC Programming Voltage 13.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	Com'l	2.4		V
			I_{OH} = −2 mA	Mil/Ind			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12 mA	Com'l		0.5	V
			I_{OL} = 8 mA	Mil/Ind			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[3]			2.2		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[3]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$, V_{CC} = Max.			−10	10	μA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			−40	40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[4, 5]			−30	−90	mA
I_{CC1}	Standby Power Supply Current	V_{CC} = Max., V_{IN} = GND Outputs Open		Com'l		140	mA
				Mil/Ind		160	mA
I_{CC2}	Power Supply Current at Frequency[5]	V_{CC} = Max., Outputs Disabled (in High Z State), Device Operating at f_{MAX} External (f_{MAX5})		Com'l		180	mA
				Mil/Ind		200	mA

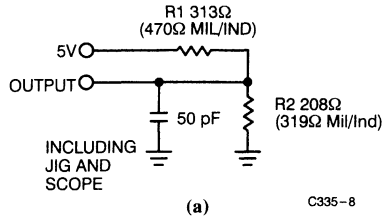
Capacitance[5]

Parameter	Description	Test Conditions	Min.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz		10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz		10	pF

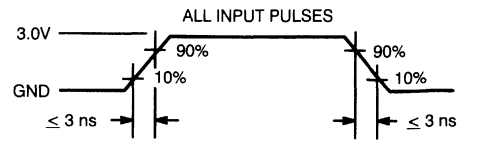
Notes:

1. t_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
4. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by ground degradation.
5. Tested initially and after any design or process changes that may affect these parameters.

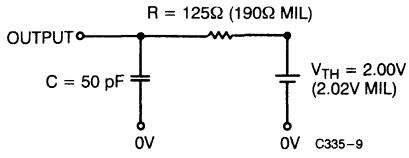
AC Test Loads and Waveforms (Commercial)



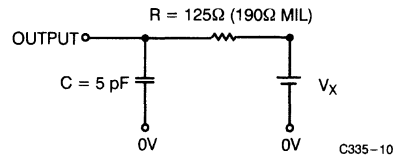
(a)



(b)



(c) Thévenin Equivalent (Load 1)



(d) Three-state Delay Load (Load 2)

Parameter	V_X	Output Waveform—Measurement Level
t_{PXZ} (−)	1.5V	V_{OH}, 0.5V, V_X C335-12
t_{PXZ} (+)	2.6V	V_{OL}, 0.5V, V_X C335-13
t_{PZX} (+)	V_{th}	V_X, 0.5V, V_{OH} C335-14
t_{PZX} (−)	V_{th}	V_X, 0.5V, V_{OL} C335-15
t_{CER} (−)	1.5V	V_{OH}, 0.5V, V_X C335-16
t_{CER} (+)	2.6V	V_{OL}, 0.5V, V_X C335-17
t_{CEA} (+)	V_{th}	V_X, 0.5V, V_{OH} C335-18
t_{CEA} (−)	V_{th}	V_X, 0.5V, V_{OL} C335-19

Figure 5. Test Waveforms

Commercial AC Characteristics

Parameter	Description	7C335–100		7C335–83		7C335–66		7C335–50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters										
t_{PD}	Input to Output Propagation Delay		15		15		20		25	ns
t_{EA}	Input to Output Enable		15		15		20		25	ns
t_{ER}	Input to Output Disable		15		15		20		25	ns
Input Registered Mode Parameters										
t_{WH}	Input and Output Clock Width HIGH[5]	4		5		6		8		ns
t_{WL}	Input and Output Clock Width LOW[5]	4		5		6		8		ns
t_{IS}	Input or Feedback Set-Up Time to Input Clock	2		2		2		3		ns
t_{IH}	Input Register Hold Time from Input Clock	2		2		2		3		ns
t_{ICO}	Input Register Clock to Output Delay		18		18		20		25	ns
t_{IOH}	Output Data Stable Time from Input Clock	3		3		3		3		ns
$t_{IOH} - t_{IH}$ 33x	Output Data Stable from Input Clock Minus Input Register Hold Time for 7C330, 7C332, and 7C335[6]	0		0		0		0		ns
t_{PZX}	Pin 14 Enable to Output Enabled		12		12		15		20	ns
t_{PXZ}	Pin 14 Disable to Output Disabled		12		12		15		20	ns
f_{MAX1}	Maximum Frequency of (2) CY7C335s in Input Registered Mode (Lowest of $1/(t_{ICO}+t_{IS})$ & $1/(t_{WL}+t_{WH})$)[5]	50		50		45.4		35.7		MHz
f_{MAX2}	Maximum Frequency Data Path in Input Registered Mode (Lowest of $(1/(t_{ICO})$, $1/(t_{WH}+t_{WL})$, $1/(t_{IS}+t_{IH})$)[5]	55.5		55.5		50		40		MHz
t_{ICEA}	Input Clock to Output Enabled		17		17		20		25	ns
t_{ICER}	Input Clock to Output Disabled		15		15		20		25	ns
Output Registered Mode Parameters										
t_{CEA}	Output Clock to Output Enabled[5]		17		17		20		25	ns
t_{CER}	Output Clock to Output Disabled[5]		15		15		20		25	ns
t_S	Output Register Input Set-Up Time from Output Clock	8		9		12		15		ns
t_H	Output Register Input Hold Time from Output Clock	0		0		0		0		ns
t_{CO}	Output Register Clock to Output Delay		9		10		12		15	ns
t_{CO2}	Input Output Register Clock or Latch Enable to Combinatorial Output Delay (Through Logic Array)[5]		17		18		23		30	ns
t_{OH}	Output Data Stable Time from Output Clock	2		2		2		2		ns
t_{OH2}	Output Data Stable Time From Output Clock (Through Memory Array)[5]	3		3		3		3		ns
$t_{OH2}-t_{IH}$	Output Data Clock Stable Time From Output Clock Minus Input Register Hold Time[5]	0		0		0		0		ns
f_{MAX3}	Maximum Frequency with Internal Feedback in Output Registered Mode[5]	100		83.3		66.6		50		MHz
f_{MAX4}	Maximum Frequency of (2) CY7C335s in Output Registered Mode (Lowest of $1/(t_{CO}+t_S)$ & $1/(t_{WL}+t_{WH})$)[5]	58.8		50		41.6		33.3		MHz
f_{MAX5}	Maximum Frequency Data Path in Output Registered Mode (Lowest of $1/(t_{CO})$, $1/(t_{WL}+t_{WH})$, $1/(t_S+t_H)$)[5]	111		100		83.3		62.5		MHz

Commercial AC Characteristics (continued)

Parameter	Description	7C335–100		7C335–83		7C335–66		7C335–50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{OH} - t_{IH}$ 33x	Output Data Stable from Output Clock Minus Input Register Hold Time for 7C330, 7C332, and 7C335[6]	0		0		0		0		ns
t_{COS}	Input Clock to Output Clock	10		12		15		20		ns
f_{MAX6}	Maximum Frequency Pipelined Mode (Lowest of $1/(t_{COS})$, $1/(t_{CO})$, $1/(t_{WL} + t_{WH})$), $1/(t_{IS} + t_{IH})$[5]	100		83.3		66.6		50		MHz
f_{MAX7}	Maximum Frequency of (2) CY7C335s in Pipelined Mode (Lowest of $1/(t_{CO} + t_{IS})$ or $1/t_{COS}$)	90.9		83.3		66.6		50		MHz
Power-Up Reset Parameters										
t_{POR}	Power-Up Reset Time[5, 7]		1		1		1		1	µs

Military/Industrial AC Characteristics

Parameter	Description	7C335–83		7C335–66		7C335–50		7C335–40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters										
t_{PD}	Input to Output Propagation Delay		20		20		25		30	ns
t_{EA}	Input to Output Enable		20		20		25		30	ns
t_{ER}	Input to Output Disable		20		20		25		30	ns
Input Registered Mode Parameters										
t_{WH}	Input and Output Clock Width HIGH[5]	5		6		8		10		ns
t_{WL}	Input and Output Clock Width LOW[5]	5		6		8		10		ns
t_{IS}	Input or Feedback Set-Up Time to Input Clock	3		3		3		4		ns
t_{IH}	Input Register Hold Time from Input Clock	3		3		3		4		ns
t_{ICO}	Input Register Clock to Output Delay		23		23		25		30	ns
t_{IOH}	Output Data Stable Time from Input Clock	3		3		3		3		ns
$t_{IOH} - t_{IH}$ 33x	Output Data Stable from Input Clock Minus Input Register Hold Time for 7C330, 7C332, and 7C335[6]	0		0		0		0		ns
t_{PZX}	Pin 14 Enable to Output Enabled		15		15		20		30	ns
t_{PXZ}	Pin 14 Disable to Output Disabled		15		15		20		30	ns
f_{MAX1}	Maximum Frequency of (2) CY7C335s in Input Registered Mode (Lowest of $1/(t_{ICO} + t_{IS})$ & $1/(t_{WL} + t_{WH})$)[5]	38.4		38.4		35.7		29.4		MHz
f_{MAX2}	Maximum Frequency Data Path in Input Registered Mode (Lowest of $(1/(t_{ICO})$, $1/(t_{WH} + t_{WL})$, $1/(t_{IS} + t_{IH}))$[5]	43.4		43.4		40		33.3		MHz
t_{ICEA}	Input Clock to Output Enabled		20		20		25		30	ns
t_{ICER}	Input Clock to Output Disabled		20		20		25		30	ns
Output Registered Mode Parameters										
t_{CEA}	Output Clock to Output Enabled [5]		20		20		25		30	ns
t_{CER}	Output Clock to Output Disabled [5]		20		20		25		30	ns
t_S	Output Register Input Set-Up Time to Output Clock	10		12		15		20		ns
t_H	Output Register Input Hold Time from Output Clock	0		0		0		0		ns
t_{CO}	Output Register Clock to Output Delay		11		12		15		20	ns

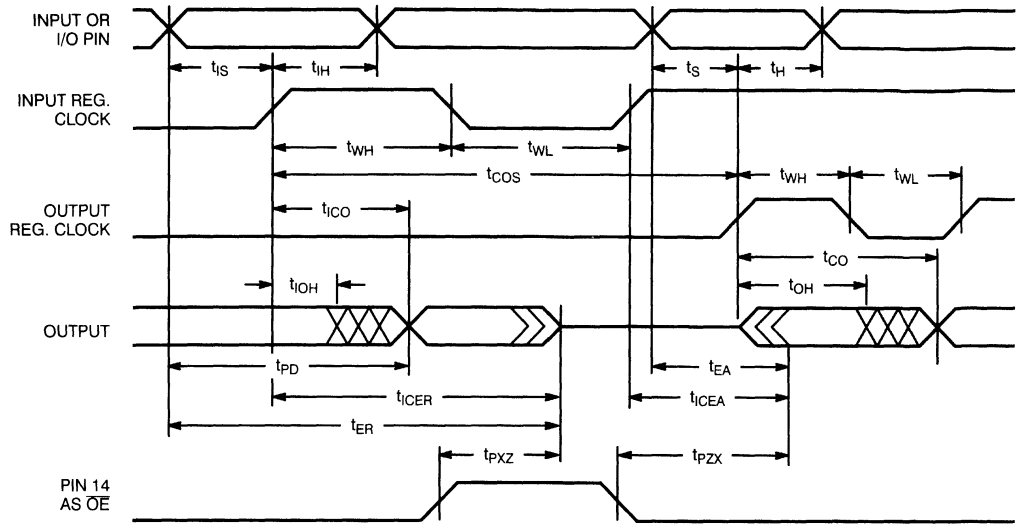
Notes:

6. This specification is intended to guarantee interface compatibility of the other members of the CY7C330 family with the CY7C335. This specification is met for the devices operating at the same ambient temperature and at the same power supply voltage.
7. This part has been designed with the capability to reset during system power-up. Following power-up, the input and output registers will be reset to a logic LOW state. The output state will depend on how the array is programmed.

Military/Industrial AC Characteristics (continued)

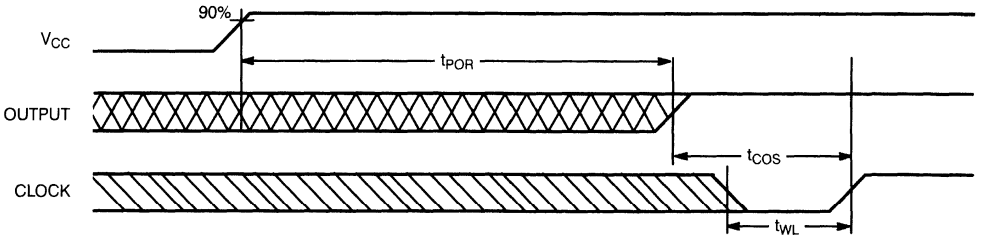
Parameter	Description	7C335–83		7C335–66		7C335–50		7C335–40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CO2}	Output Register Clock or Latch Enable to Combinatorial Output Delay (Through Logic Array)[5]		22		23		30		35	ns
t_{OH}	Output Data Stable Time from Output Clock	2		2		2		2		ns
t_{OH2}	Output Data Stable Time From Output Clock (Through Memory Array)[5]	3		3		3		3		ns
$t_{OH2}-t_{IH}$	Output Data Clock Stable Time From Output Clock Minus Input Register Hold Time[5]	0		0		0		0		ns
f_{MAX3}	Maximum Frequency with Internal Feedback in Output Registered Mode[5]	83.3		66.6		50		40		MHz
f_{MAX4}	Maximum Frequency of (2) CY7C335s in Output Registered Mode (Lower of $1/(t_{CO} + t_S)$ & $1/(t_{WL} + t_{WH})$)[5]	47.6		41.6		33.3		25		MHz
f_{MAX5}	Maximum Frequency Data Path in Output Registered Mode (Lowest of $1/(t_{CO})$, $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$)[5]	90.9		83.3		62.5		50		MHz
$t_{OH} - t_{IH}$ 33x	Output Data Stable from Output Clock Minus Input Register Hold Time for 7C330, 7C332, and 7C335[6]	0		0		0		0		ns
Pipelined Mode Parameters										
t_{COS}	Input Clock to Output Clock	12		15		20		25		ns
f_{MAX6}	Maximum Frequency Pipelined Mode (Lowest of $1/(t_{COS})$, $1/(t_{IS})$, or $1/(t_{CO})$), $1/(t_{IS} + t_{IH})$[5]	83.3		66.6		50		40		MHz
f_{MAX7}	Maximum Frequency of (2) CY7C335s in Pipelined Mode (Lowest of $1/(t_{CO} + t_{IS})$ or $1/t_{COS}$)	71.4		66.6		50		40		MHz
Power-Up Reset Parameters										
t_{POR}	Power-Up Reset Time[5, 7]		1		1		1		1	μs

Switching Waveform



C335-20

Power-Up Reset Waveform[7]



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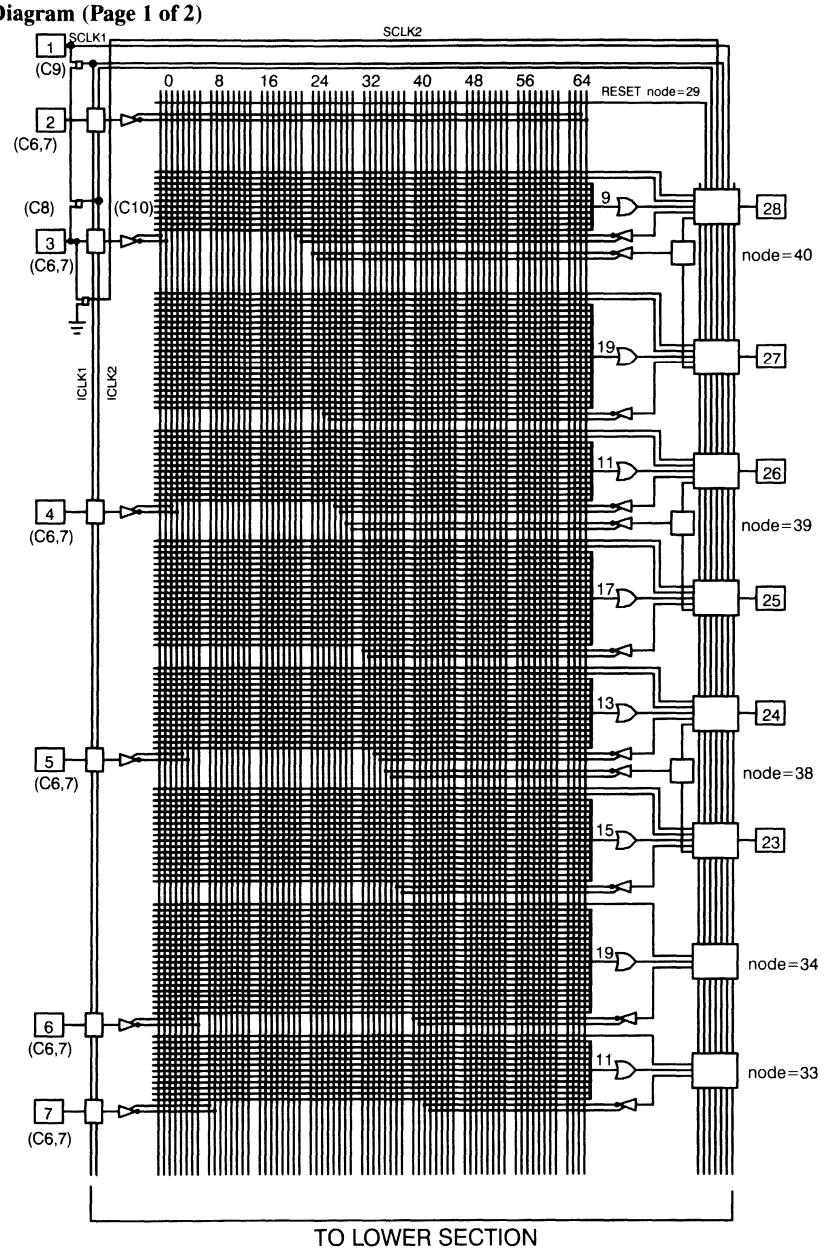
Block Diagram (Page 1 of 2)



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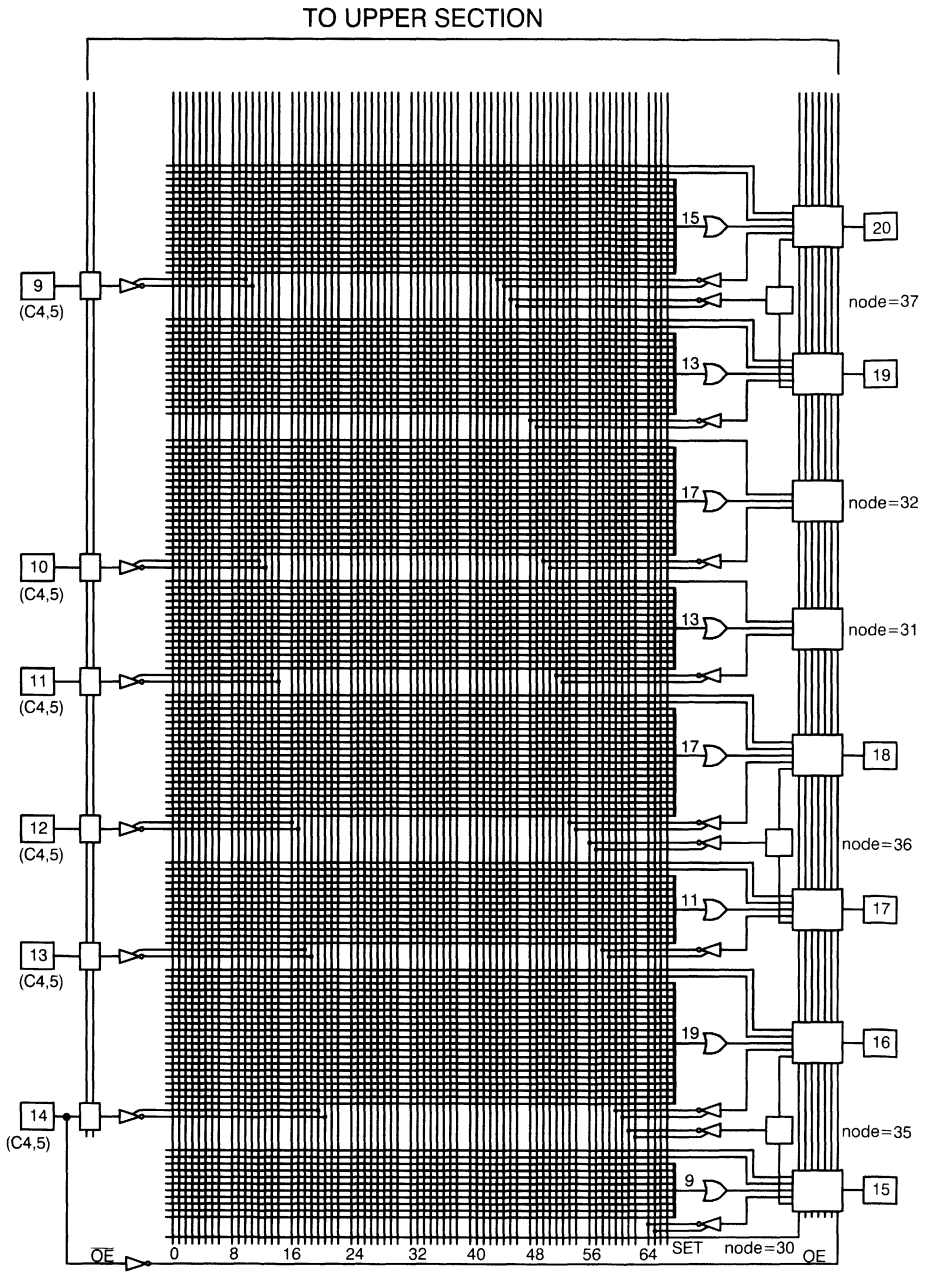
Block Diagram (Page 2 of 2)



C335-23

Ordering Information

f_{MAX} (MHz)	I_{CC1} (mA)	Ordering Code	Package Name	Package Type	Operating Range
100	140	CY7C335-100HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
		CY7C335-100JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C335-100PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C335-100WC	W22	28-Lead (300-Mil) Windowed CerDIP	
83.3	160	CY7C335-83DI	D22	28-Lead (300-Mil) CerDIP	Industrial
		CY7C335-83HI	H64	28-Pin Windowed Leaded Chip Carrier	
		CY7C335-83PI	P21	28-Lead (300-Mil) Molded DIP	
		CY7C335-83WI	W22	28-Lead (300-Mil) Windowed CerDIP	
		CY7C335-83DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C335-83HMB	H64	28-Pin Windowed Leaded Chip Carrier	
		CY7C335-83LMB	L64	28-Square Leadless Chip Carrier	
		CY7C335-83QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C335-83WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
83.3	140	CY7C335-83HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
		CY7C335-83JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C335-83PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C335-83WC	W22	28-Lead (300-Mil) Windowed CerDIP	
66.6	160	CY7C335-66DI	D22	28-Lead (300-Mil) CerDIP	Industrial
		CY7C335-66HI	H64	28-Pin Windowed Leaded Chip Carrier	
		CY7C335-66PI	P21	28-Lead (300-Mil) Molded DIP	
		CY7C335-66WI	W22	28-Lead (300-Mil) Windowed CerDIP	
		CY7C335-66DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C335-66HMB	H64	28-Pin Windowed Leaded Chip Carrier	
		CY7C335-66LMB	L64	28-Square Leadless Chip Carrier	
		CY7C335-66QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C335-66WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
66.6	140	CY7C335-66HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
		CY7C335-66JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C335-66PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C335-66WC	W22	28-Lead (300-Mil) Windowed CerDIP	
50	140	CY7C335-50HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
		CY7C335-50JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C335-50PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C335-50WC	W22	28-Lead (300-Mil) Windowed CerDIP	

Ordering Information (continued)

f_{MAX} (MHz)	I_{CC1} (mA)	Ordering Code	Package Name	Package Type	Operating Range
50	160	CY7C335–50DI	D22	28-Lead (300-Mil) CerDIP	Industrial
		CY7C335–50HI	H64	28-Pin Windowed Leaded Chip Carrier	
		CY7C335–50PI	P21	28-Lead (300-Mil) Molded DIP	
		CY7C335–50WI	W22	28-Lead (300-Mil) Windowed CerDIP	
		CY7C335–50DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C335–50HMB	H64	28-Pin Windowed Leaded Chip Carrier	
		CY7C335–50LMB	L64	28-Square Leadless Chip Carrier	
		CY7C335–50QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C335–50WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
40	160	CY7C335–40DI	D22	28-Lead (300-Mil) CerDIP	Industrial
		CY7C335–40HI	H64	28-Pin Windowed Leaded Chip Carrier	
		CY7C335–40PI	P21	28-Lead (300-Mil) Molded DIP	
		CY7C335–40WI	W22	28-Lead (300-Mil) Windowed CerDIP	
		CY7C335–40DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C335–40HMB	H64	28-Pin Windowed Leaded Chip Carrier	
		CY7C335–40LMB	L64	28-Square Leadless Chip Carrier	
		CY7C335–40QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C335–40WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	9, 10, 11
t_{ICO}	9, 10, 11
t_{IS}	9, 10, 11
t_{CO}	9, 10, 11
t_S	9, 10, 11
t_H	9, 10, 11
t_{COS}	9, 10, 11

Document #: 38-00186-C

CY7C258
CY7C259

2K x 16 Reprogrammable State Machine PROM

Features

- **High speed: 100-MHz operation**
  - **— t_{CP} = 10 ns**
  - **— t_{CKO} = 8 ns**
  - **— t_{AS} = 2 ns**
- **11-bit-wide state word**
- **Can be programmed as asynchronous PROM t_{AA} = 18 ns**
- **Optimum speed/ power**
- **Individually bypassable input and output registers**
- **Individually programmable address/ feedback muxes**
- **Synchronous and asynchronous chip select**
- **Synchronous and asynchronous $\overline{INIT}$ and programmable initialize word**
- **16 outputs (CY7C259)**
- **Software support**
- **CY7C258 available in 28-pin, 300-mil plastic and ceramic DIP, LCC, PLCC**
- **CY7C259 available in 44-pin LCC and PLCC**
- **Reprogrammable in windowed packages**
- **Capable of withstanding greater than 2001V static discharge**

Functional Description

The CY7C258 and CY7C259 are 2K x 16 CMOS PROMs specifically designed for use in state machine applications.

State machines are one of the most common applications for registered PROMs. The CY7C258 and CY7C259 feature internal state feedback and a variety of programmable features to support 100-MHz state machines with as many as 2,048 distinct states.

It is easy to use a PROM as a state machine. Each array location contains output data as well as information fed back to select the next state. Note that a PROM is only limited by the number of array inputs. If a given state machine can be implemented in the number of inputs/ feedbacks available (11 on the CY7C258/259), then it will always fit in the device. No software minimization is required.

Among the programmable features of the CY7C258/CY7C259 are individually bypassable input and output registers. The registers run off the same clock for pipeline capability. Each individual register can be programmed to capture data at the rising edge of the clock or to be transparent.

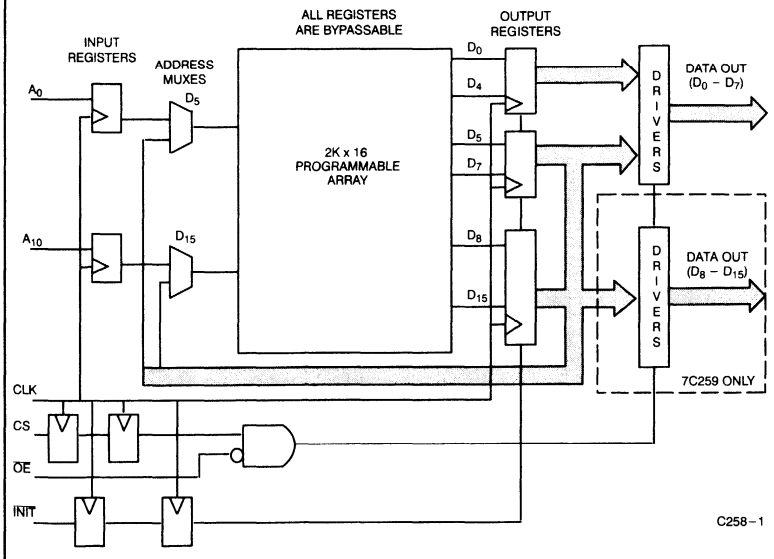
The registers at the inputs are useful for signals that require short set-up times (t_{AS} = 2 ns). The input register does introduce a cycle of latency, however. For signals that directly affect the next state of the machine, each input register can be bypassed. Note that the cycle time remains the same (10-ns min.), even if the inputs are bypassed.

Registers at the output are used to hold both state information and output data. These registers are also bypassable for maximum flexibility. Occasionally, an individual output cannot wait for the next clock edge. These outputs are sometimes called Mealy outputs, and can be created by bypassing the appropriate output register.

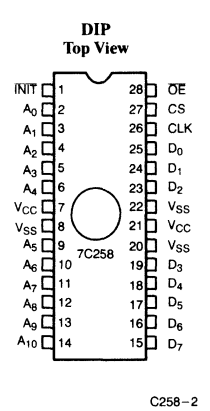
Since the CY7C258 and CY7C259 contain a 2K array, they each require 11 inputs. Each of these inputs can come from an input pin or from internal output register feedback. Eleven individually programmable address muxes allow the user to select the ratio of pin input and state feedback.

These devices have both an asynchronous output ($\overline{OE}$) and a synchronous chip select (CS). The CS input is polarity programmable and registered twice. Each of

Logic Block Diagram



Pin Configurations



Functional Description (continued)

the CS registers can be bypassed in the same manner as the address input and output registers.

A separately controllable $\overline{INIT}$ input is included for user resets. If $\overline{INIT}$ is sampled LOW on the rising edge of CLK, the user programmable initialization word will appear at the outputs after the next CLK cycle. Each of the $\overline{INIT}$ registers can be bypassed in the same manner as the address input and output registers.

The difference between the CY7C258 and CY7C259 is in the packaging. The CY7C258 has three different types of outputs. $D_4 - D_0$ are dedicated outputs that do not feed back to the input muxes. $D_5 - D_7$ appear on the output pins and are fed back to the input muxes. Finally, $D_8 - D_{15}$ are dedicated feedback lines that do not appear at the output pins. The dedicated feedback allows the CY7C258 to be packaged in 28-pin packages. The CY7C258 is available in 28-pin LCC, PLCC, and slim 300-mil DIP packages.

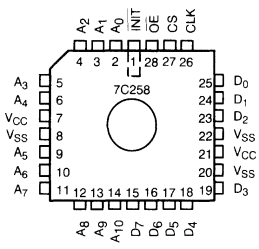
On the CY7C259, all 16 array outputs are available at the pins. Outputs $D_4 - D_0$ remain as dedicated outputs while $D_5 - D_{15}$ appear at the pins and are also fed back to the input muxes. This organization allows the user maximum flexibility in selecting the ratio of outputs to state feedback. The availability of state information at pins also improves testability. The CY7C259 is packaged in 44-pin LCC and PLCC packages.

Several third-party programmers feature support for PROMs as state machines, including Data I/O (ABEL), ISDATA (LOG/iC), and CUPL. The devices are also supported on the Cypress *Warp2* and *Warp3* development software.

The CY7C258 and CY7C259 offer the advantage of low power, superior performance, and programming yield. The EPROM cells allow for each memory location to be 100% tested, with each location being written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

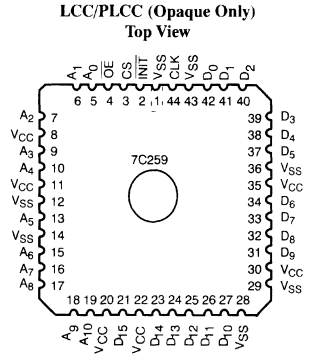
Pin Configurations (continued)

LCC/PLCC(Opaque Only)
Top View



C258-3

LCC/PLCC (Opaque Only)
Top View



C258-4

Selection Guide

	Commercial	Commercial and Military		
	7C258-10 7C259-10	**7C258-12 7C259-12**	**7C258-15 7C259-15**	**Unit**
Minimum Cycle Time	10	12	15	ns
Registered Input Set-Up/Hold[1]	2/2 or 5/0	3/3 or 7/0	4/4 or 8/1	ns
Bypassed Input Set-Up/Hold	10/0	12/0	15/0	ns
Clock-to-Output	8	9	11	ns

Note:
1. This parameter is programmable.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage 13.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

UV Exposure ..... 7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[2]	−40°C to +85°C	5V ± 10%
Military[3]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[4, 5]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA	Commercial		0.4	V
		V_{CC} = Min., I_{OL} = 6 mA	Military		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs		2.0	6.0	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs		−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		−40	+40	μA
I_{OS}	Output Short Circuit Current[6]	V_{CC} = Max., V_{OUT} = GND		−20	−90	mA
I_{CC}	Active Current[7]	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		70	mA
		V_{CC} = Max., I_{OUT} = 0 mA	Military		90	mA

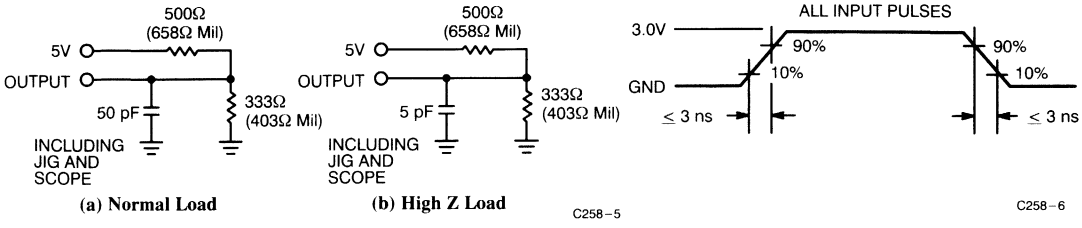
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

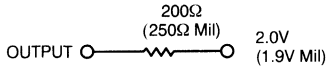
Notes:

2. Contact a Cypress representative for industrial temperature range specification.
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.
5. See Introduction to CMOS PROMs in this Data Book for general information on testing.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
7. Add 1 mA/MHz for AC power component.

AC Test Loads and Waveforms[4]



Equivalent to: THÉVENIN EQUIVALENT

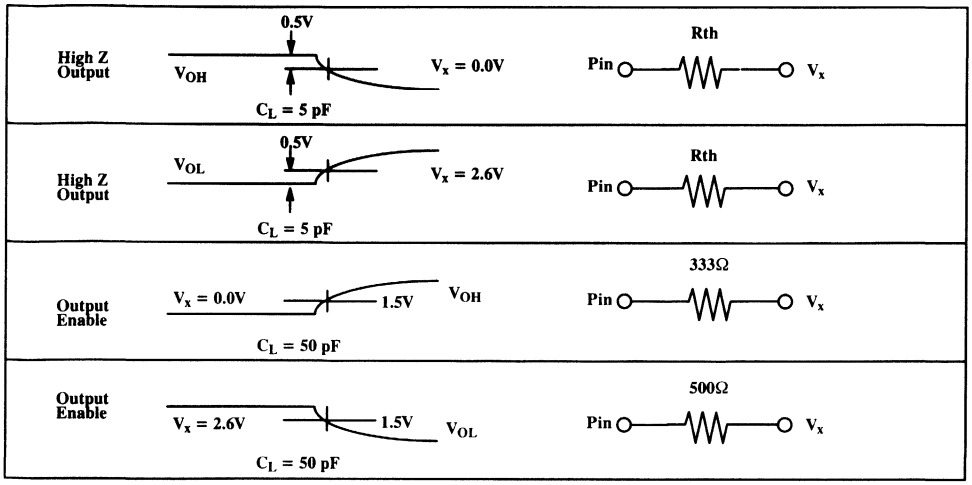


Switching Characteristics Over the Operating Range[3, 4]

Parameter	Description	Commercial		Commercial and Military				Unit
		7C258–10 7C259–10		7C258–12 7C259–12		7C258–15 7C259–15		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CP}	Clock Period	10		12		15		ns
t_{CH}	Clock HIGH	4		5		6.5		ns
t_{CL}	Clock LOW	4		5		6.5		ns
t_{AS}/t_{AH}	Register Input Set-Up/Hold	2/2 or 5/0		3/3 or 7/0		4/4 or 8/1		ns
t_{ABS}	Address Set-Up to CLK with Input Bypassed	10		12		15		ns
t_{ABH}	Address Hold from CLK with Input Bypassed	0		0		0		ns
t_{CSS}/t_{CSH}	Chip Select Set-Up/Hold	2/2 or 5/0		3/3 or 7/0		4/4 or 8/1		ns
t_{IPD}	Asynchronous $\overline{INIT}$ to Output Valid with Output Bypassed		21		21		25	ns
t_{CKO1}	Output CLK to Registered Output Valid		8		9		11	ns
t_{CKO2}	Output CLK to Output Valid with Output Bypassed		18		18		21	ns
t_{DH}	Data Hold from CLK	2		2		2		ns
t_{COV}	CLK to Output Valid[8]		8		9		11	ns
t_{COZ}	CLK to High Z Output[8]		8		9		11	ns
t_{CSV}	CS to Output Valid with Input Bypassed[8]		10		12		15	ns
t_{CSZ}	CS to High Z Output with Input Bypassed[8]		10		12		15	ns
t_{OEV}	$\overline{OE}$ to Output Valid[8]		8		9		11	ns
t_{OEZ}	$\overline{OE}$ to High Z Output[8]		8		9		11	ns
t_{IS}/t_{IH}	$\overline{INIT}$ Set-Up/Hold	2/2 or 5/0		3/3 or 7/0		4/4 or 8/1		ns
t_{IBS}	$\overline{INIT}$ Set-Up to CLK with Input Bypassed	10		12		15		ns
t_{IBH}	$\overline{INIT}$ Hold from CLK with Input Bypassed	0		0		0		ns
t_{PD}	Propagation Delay with Input and Output Bypassed		18		18		21	ns
t_{ICO}	CLK to Output Valid with Output Bypassed		18		18		21	ns
t_{IW}	Asynchronous $\overline{INIT}$ Pulse Width	10		12		15		ns
t_{IDV}	Asynchronous $\overline{INIT}$ to Data Valid		10		12		15	ns
t_{ICR}	Asynchronous $\overline{INIT}$ Recovery to Clock	10		12		15		ns

Note:
8. See Output Waveform—Measurement Level.

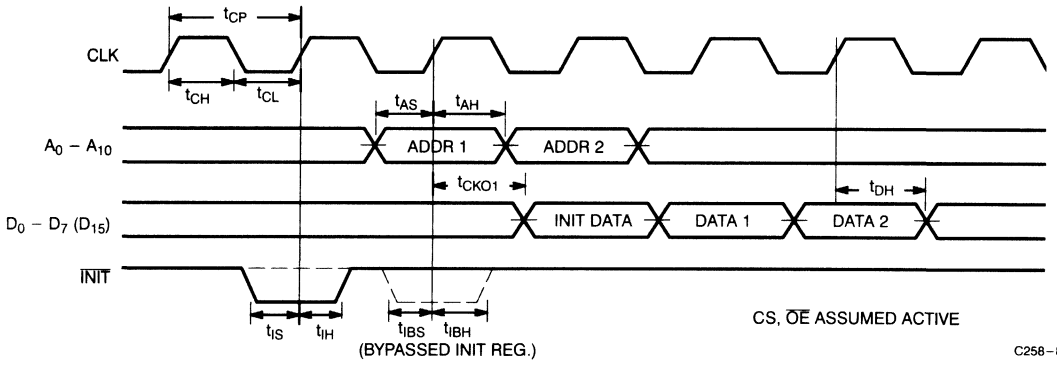
Output Waveform—Measurement Level



C258-7

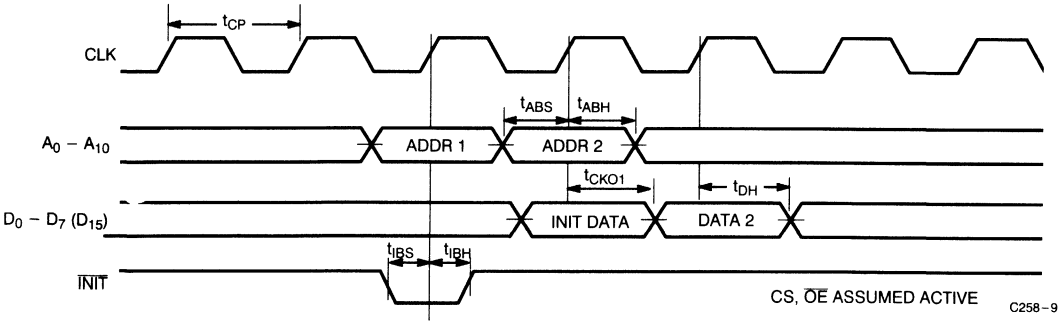
Switching Waveforms

Registered Input and Output (combined with $\overline{INIT}$)



C258-8

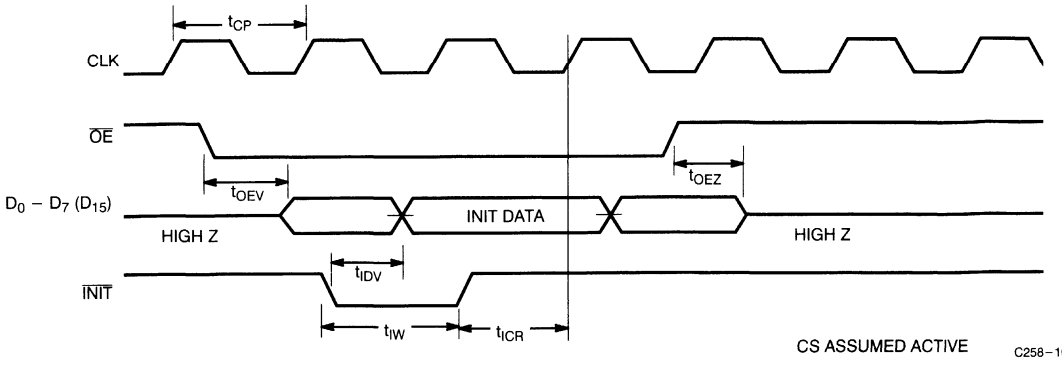
Bypassed Address and $\overline{INIT}$ Registers



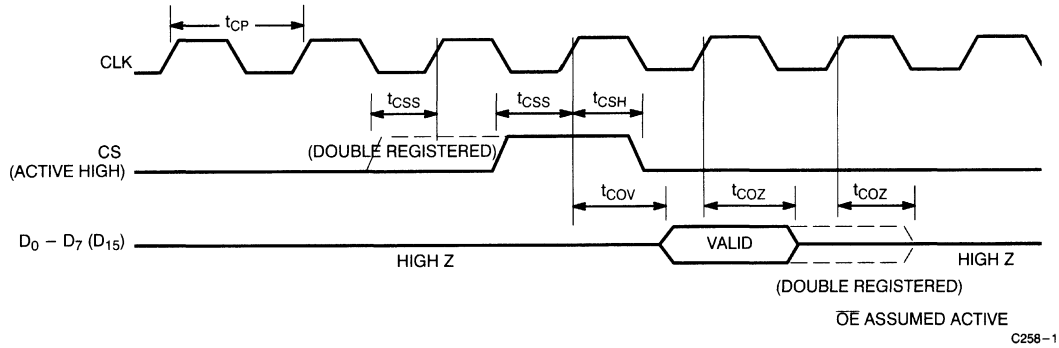
C258-9

Switching Waveforms (continued)

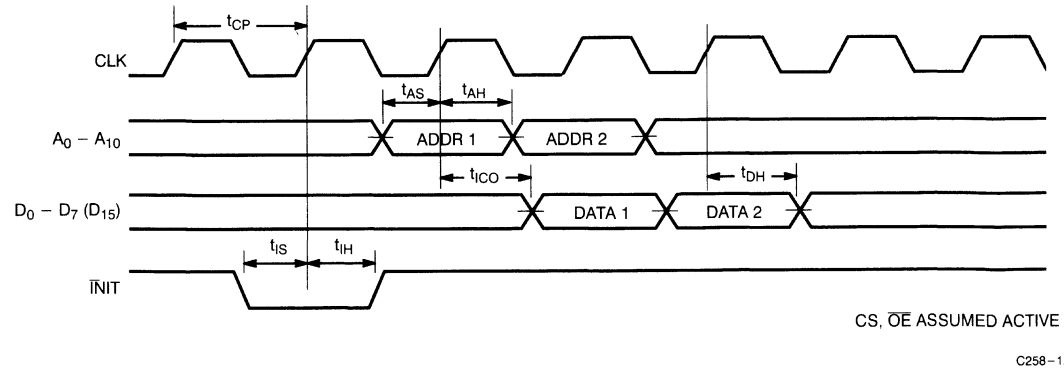
Asynchronous $\overline{INIT}$ and $\overline{OE}$



Single- and Double-Registered Chip Select



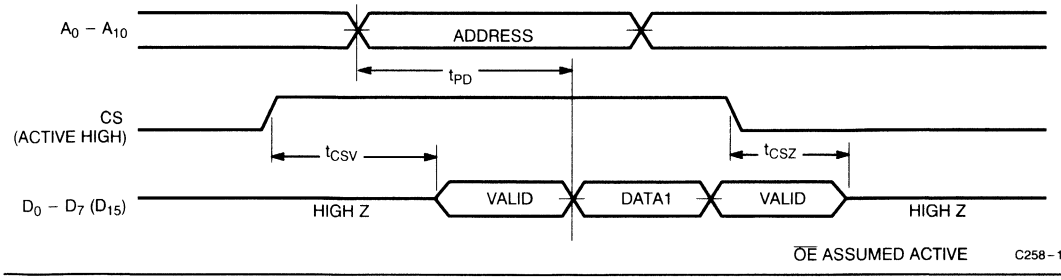
Bypassed Output Register[9]



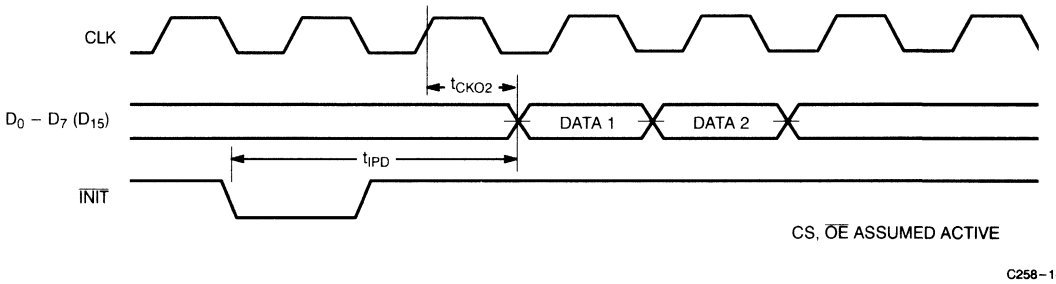
Note:
9. Even though the register is bypassed, $\overline{INIT}$ continues to set the output register (for feedback purposes).

Switching Waveforms

Bypassed Input and Output Register (CS and Address)



Asynchronous $\overline{INIT}$ and Bypassed Output Register[10]



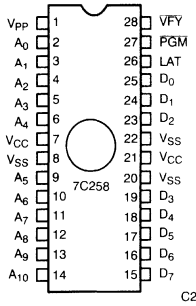
Note:
10. Output registers configured as feedback to the array and bypassed with respect to the output.

Mode Table

Mode	LAT (7C258–CLK)	VPP ($\overline{INIT}$)	$\overline{PGM}$ (CS)	$\overline{VFY}$ ($\overline{OE}$)	D_0–D_{15} (259) D_0–D_7 (258)
Latch High Byte	V_{IHP}	V_{PP}	V_{IHP}	V_{IHP}	V_{IHP}/V_{ILP}
Program Inhibit	V_{ILP}	V_{PP}	V_{IHP}	V_{IHP}	HI–Z
Program Enable	V_{ILP}	V_{PP}	V_{ILP}	V_{IHP}	V_{IHP}/V_{ILP}
Program Verify	V_{ILP}	V_{PP}	V_{IHP}	V_{ILP}	V_{OHP}/V_{OLP}

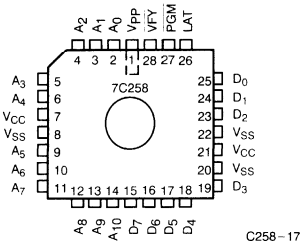
Programming Pinouts

DIP



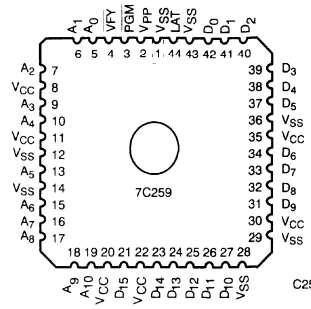
C258-15

LCC/PLCC (Opaque Only)



C258-17

LCC/PLCC (Opaque Only)



C258-16

Programming Information

This datasheet provides some but not all of the programming information necessary for on-board programming of the CY7C258 and CY7C259. For more information about on-board programming of Cypress PROMs contact your local Cypress Field Sales Engineer or Field Applications Engineer.

7C258 Bitmap[11]

Programmer Address Decimal	Programmer Address Hex	Programmer Memory 7C258	Bit Breakdown D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
0	0	Data	. . . Array Data . . .
.	.	.	
.	.	.	
.	.	.	
2047	7FF	Data	
2048	800	Address Register Select (1=Bypassed Register)	A_9 A_8 A_7 A_6 A_5 A_2 A_1 A_0 A_{10} X X X X X A_4 A_3
2049	801	Array Input Select (1= Feedback)	A_9 A_8 A_7 A_6 A_5 A_2 A_1 A_0 A_{10} X X X X X A_4 A_3
2050	802	Output Register Select (1= Bypassed Register)	X X X X X X X X D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
2051	803	INIT WORD (1= INIT Bit 1)	D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
2052	804	Architecture	X X X X X X X X SH C_1 C_2 CP IB IA X X

Note:
11. All configurable bits default to 0.

7C259 Bitmap[11]

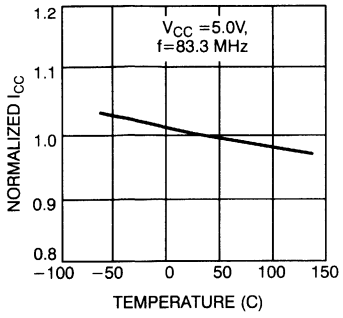
Programmer Address Decimal	Programmer Address Hex	Programmer Memory 7C259	Bit Breakdown D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
0	0	Data	Array Data
.	.	.	
.	.	.	
.	.	.	
2047	7FF	Data	
2048	800	Address Register Select (1 = Bypassed Register)	A_{10} A_9 A_8 A_7 A_6 A_5 X X X X X A_4 A_3 A_2 A_1 A_0
2049	801	Array Input Select (1 = Feedback)	A_{10} A_9 A_8 A_7 A_6 A_5 X X X X X A_4 A_3 A_2 A_1 A_0
2050	802	Output Register Select (1 = Bypassed Register)	D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
2051	803	INIT WORD (1 = INIT Bit 1)	D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
2052	804	Architecture	SH C_1 C_2 CP IB IA X X X X X X X X X X

Architecture Word

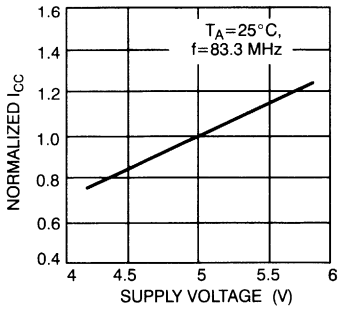
Control Option	Control Word			Function
	Bit (258)	Bit (259)	Programmed level	
IA (INIT Async)	D_2	D_{10}	0 = Default 1 = Programmed	Synchronous INIT Asynchronous INIT
IB (INIT Bypass)	D_3	D_{11}	0 = Default 1 = Programmed	INIT Registered Bypass INIT Register
CP (CS Polarity)	D_4	D_{12}	0 = Default 1 = Programmed	CS Active LOW CS Active HIGH
C2 (CS Bypass) (Buried Register)	D_5	D_{13}	0 = Default 1 = Programmed	CS Input Registered Bypass CS Register
C1 (CS Bypass) (Input Register)	D_6	D_{14}	0 = Default 1 = Programmed	CS Input Registered Bypass CS Register
SH (Set-Up/Hold)	D_7	D_{15}	0 = Default 1 = Programmed	Set-Up/Hold = 2/2 ns Set-Up/Hold = 5/0 ns

Typical DC and AC Characteristics

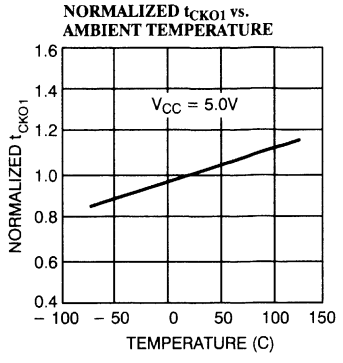
NORMALIZED I_{CC} vs. AMBIENT TEMPERATURE



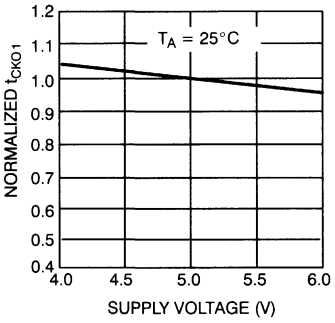
NORMALIZED I_{CC} vs. SUPPLY VOLTAGE



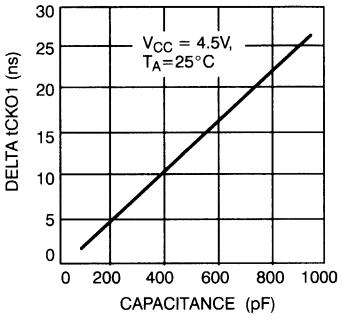
NORMALIZED t_{CKO1} vs. AMBIENT TEMPERATURE



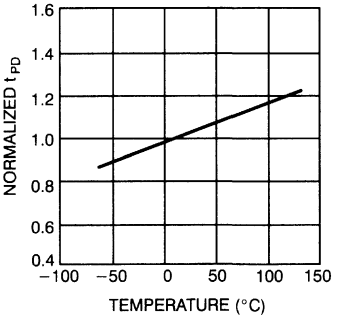
NORMALIZED t_{CKO1} vs. SUPPLY VOLTAGE



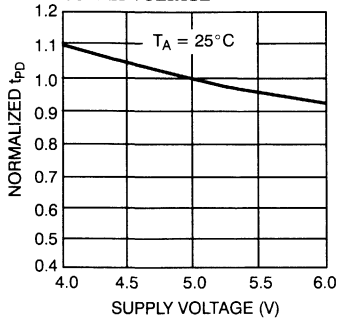
TYPICAL t_{CKO1} CHANGE vs. OUTPUT LOADING



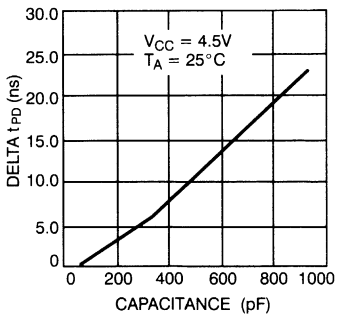
NORMALIZED t_{PD} vs. AMBIENT TEMPERATURE



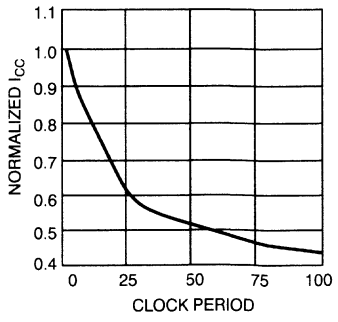
NORMALIZED t_{PD} vs. SUPPLY VOLTAGE



DELTA t_{PD} vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CLOCK PERIOD



Ordering Information[12]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C258–10HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C258–10JC	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C258–10PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C258–10WC	W22	28-Lead (300-Mil) Windowed CerDIP	
12	CY7C258–12HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C258–12JC	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C258–12PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C258–12WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C258–12HMB	H64	28-Pin Windowed Leaded Chip Carrier	Military
	CY7C258–12LMB	L64	28-Square Leadless Chip Carrier	
	CY7C258–12QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C258–12WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
15	CY7C258–15HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C258–15JC	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C258–15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C258–15WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C258–15HMB	H64	28-Pin Windowed Leaded Chip Carrier	Military
	CY7C258–15LMB	L64	28-Square Leadless Chip Carrier	
	CY7C258–15QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
	CY7C258–15WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C259–10HC	H67	44-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C259–10JC	J67	44-Lead Plastic Leaded Chip Carrier	
12	CY7C259–12HC	H67	44-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C259–12JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C259–12HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C259–12LMB	L67	44-Square Leadless Chip Carrier	
	CY7C259–12QMB	Q67	44-Pin Windowed Leadless Chip Carrier	
15	CY7C259–15HC	H67	44-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C259–15JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C259–15HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C259–15LMB	L67	44-Square Leadless Chip Carrier	
	CY7C259–15QMB	Q67	44-Pin Windowed Leadless Chip Carrier	

Note:
12. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3,
V_{OL}	1, 2, 3,
V_{IH}	1, 2, 3,
V_{IL}	1, 2, 3,
I_{IX}	1, 2, 3,
I_{OZ}	1, 2, 3,
I_{CC}	1, 2, 3,

Switching Characteristics

Parameter	Subgroups
t_{CP}	7, 8, 9, 10, 11
t_{CH}	7, 8, 9, 10, 11
t_{CL}	7, 8, 9, 10, 11
t_{AS}	7, 8, 9, 10, 11
t_{ABS}	7, 8, 9, 10, 11
t_{CSS}	7, 8, 9, 10, 11
t_{CSH}	7, 8, 9, 10, 11
t_{IPD}	7, 8, 9, 10, 11
t_{CKO1}	7, 8, 9, 10, 11
t_{CKO2}	7, 8, 9, 10, 11
t_{DH}	7, 8, 9, 10, 11
t_{COV}	7, 8, 9, 10, 11
t_{CSV}	7, 8, 9, 10, 11
t_{OEV}	7, 8, 9, 10, 11
t_{IS}	7, 8, 9, 10, 11
t_{IH}	7, 8, 9, 10, 11
t_{IBS}	7, 8, 9, 10, 11
t_{IBH}	7, 8, 9, 10, 11
t_{PD}	7, 8, 9, 10, 11
t_{ICO}	7, 8, 9, 10, 11
t_{IW}	7, 8, 9, 10, 11
t_{IDV}	7, 8, 9, 10, 11
t_{ICR}	7, 8, 9, 10, 11

Document #: 38-00173-E

CPLDs 3

Section Contents

CPLDs (Complex PLDs)

CY7C340 EPLD Family

Multiple Array Matrix High-Density EPLDs

Features

- **Erasable, user-configurable CMOS EPLDs capable of implementing high-density custom logic functions**
- **0.8-micron double-metal CMOS EPROM technology (CY7C34X)**
- **Advanced 0.65-micron CMOS technology to increase performance (CY7C34XB)**
- **Multiple Array MatriX architecture optimized for speed, density, and straightforward design implementation**
  - **Programmable Interconnect Array (PIA) simplifies routing**
  - **Flexible macrocells increase utilization**
  - **Programmable clock control**
  - **Expander product terms implement complex logic functions**
- ***Warp2*™**
  - **Low-cost VHDL compiler for PLDs**
  - **IEEE 1076-compliant VHDL**
  - **Available on PC and Sun platforms**
- ***Warp3*™**
  - **VHDL synthesis**
  - **ViewLogic graphical user interface**
  - **Schematic capture (ViewDraw™)**
  - **VHDL simulation (ViewSim™)**
  - **Available on PC and Sun platforms**

General Description

The Cypress Multiple Array Matrix (MAX®) family of EPLDs provides a user-configurable, high-density solution to general-purpose logic integration requirements. With the combination of innovative architecture and state-of-the-art process, the MAX EPLDs offer LSI density without sacrificing speed.

The MAX architecture makes it ideal for replacing large amounts of TTL SSI and MSI logic. For example, a 74161 counter utilizes only 3% of the 128 macrocells available in the CY7C342. Similarly, a 74151 8-to-1 multiplexer consumes less than 1% of the over 1,000 product terms in the CY7C342. This allows the designer to replace 50 or more TTL packages with just one MAX EPLD. The family comes in a range of densities, shown below. By standardizing on a few MAX building blocks, the designer can replace hundreds of different 7400 series part numbers currently used in most digital systems.

The family is based on an architecture of flexible macrocells grouped together into Logic Array Blocks (LABs). Within the LAB is a group of additional product terms called expander product terms. These expanders are used and shared by the macrocells, allowing complex functions of up to 35 product terms to be easily implemented in a single macrocell. A Programmable Interconnect Array (PIA) globally routes all signals within devices containing more than one LAB. This architecture is fabricated on the Cypress 0.8-micron, double-layer-metal CMOS EPROM process, yielding devices with significantly higher integration, density and system clock speed than the largest of previous generation EPLDs. The CY7C34XB devices are 0.65-micron shrinks of the original 0.8-micron family. The CY7C34XBs offer faster speed bins for each device in the Cypress MAX family.

The density and performance of the CY7C340 family is accessed using Cypress's *Warp2* and *Warp3* design software. *Warp2* provides state-of-the-art VHDL synthesis for MAX at a very low cost. *Warp3* is a sophisticated CAE tool that includes schematic capture (ViewDraw) and timing simulation (ViewSim) in addition to VHDL synthesis. Consult the *Warp2* and *Warp3* datasheets for more information about the development tools.

3

Max Family Members

Feature	CY7C344(B)	CY7C343(B)	CY7C342(B)	CY7C346(B)	CY7C341(B)
Macrocells	32	64	128	128	192
MAX Flip-Flops	32	64	128	128	192
MAX Latches[1]	64	128	256	256	384
MAX Inputs[2]	23	35	59	84	71
MAX Outputs	16	28	52	64	64
Packages	28H,J,W,P	44H,J	68H,J,R	84H,J/100R,N	84H,J,R

Key: P—Plastic DIP; H—Windowed Ceramic Leaded Chip Carrier; J—Plastic J-Lead Chip Carrier; R—Windowed Pin Grid Array; W—Windowed Ceramic DIP; N—Plastic Quad Flatpack

Notes:
1. When all expander product terms are used to implement latches.
2. With one output.

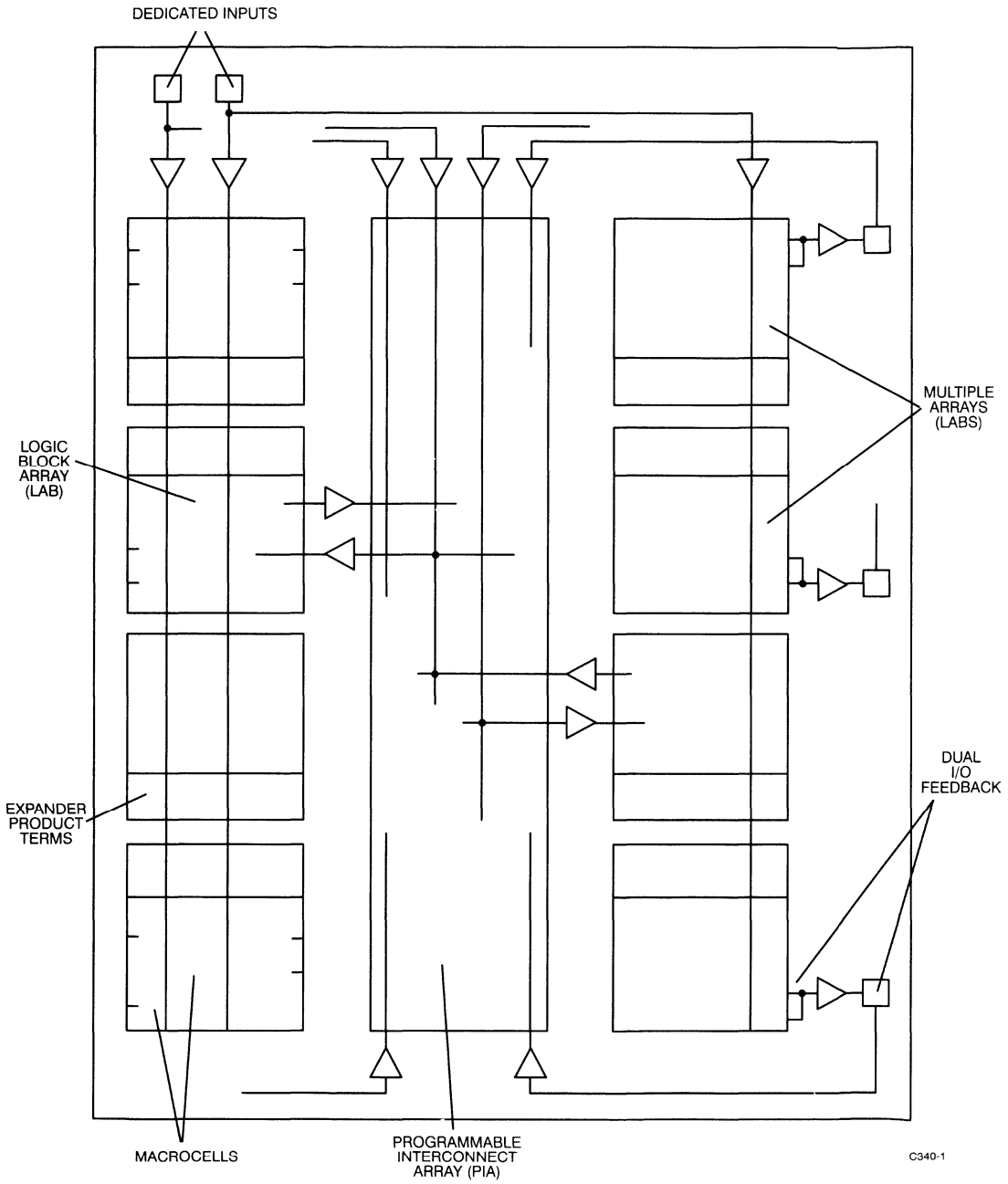


Figure 1. Key MAX Features

Functional Description

The Logic Array Block

The logic array block, shown in *Figure 2*, is the heart of the MAX architecture. It consists of a macrocell array, expander product term array, and an I/O block. The number of macrocells, expanders, and I/O vary, depending upon the device used. Global feedback of all signals is provided within a LAB, giving each functional block complete access to the LAB resources. The LAB itself is fed by the programmable interconnect array and dedicated input bus. The feedbacks of the macrocells and I/O pins feed the PIA, providing access to them through other LABs in the device. The members of the CY7C340 family of EPLDs that have a single LAB use a global bus, so a PIA is not needed (see *Figure 3*).

The MAX Macrocell

Traditionally, PLDs have been divided into either PLA (programmable AND, programmable OR), or PAL® (programmable AND, fixed OR) architectures. PLDs of the latter type provide faster input-to-output delays, but can be inefficient due to fixed allocation of product terms. Statistical analysis of PLD logic designs has shown that 70% of all logic functions (per macrocell) require three product terms or less.

The macrocell structure of MAX has been optimized to handle variable product term requirements. As shown in *Figure 4*, each macrocell consists of a product term array and a configurable register. In the macrocell, combinatorial logic is implemented with three product terms ORed together, which then feeds an XOR gate. The second input to the XOR gate is also controlled by a product term, providing the ability to control active HIGH or active LOW logic and to implement T- and JK-type flip-flops.

If more product terms are required to implement a given function, they may be added to the macrocell from the expander product term array. These additional product terms may be added to any macrocell, allowing the designer to build gate-intensive logic, such as address decoders, adders, comparators, and complex state machines, without using extra macrocells.

The register within the macrocell may be programmed for either D, T, JK, or RS operation. It may alternately be configured as a flow-through latch for minimum input-to-output delays, or bypassed entirely for purely combinatorial logic. In addition, each register supports both asynchronous preset and clear, allowing asynchronous loading of counters of shift registers, as found in many standard TTL functions. These registers may be clocked with a synchronous system clock, or clocked independently from the logic array.

Expander Product Terms

The expander product terms, as shown in *Figure 5*, are fed by the dedicated input bus, the programmable interconnect array, the macrocell feedback, the expanders themselves, and the I/O pin feedbacks. The outputs of the expanders then go to each and every product term in the macrocell array. This allows expanders to be "shared" by the product terms in the logic array block. One expander may feed all macrocells in the LAB, or even multiple product terms in the same macrocell. Since these expanders feed the secondary product terms (preset, clear, clock, and output enable) of each macrocell, complex logic functions may be implemented without utilizing another macrocell. Likewise, expanders may feed and be shared by other expanders, to implement complex multilevel logic and input latches.

I/O Block

Separate from the macrocell array is the I/O control block of the LAB. *Figure 6* shows the I/O block diagram. The three-state buffer is controlled by a macrocell product term and the drives the I/O pad. The input of this buffer comes from a macrocell within the

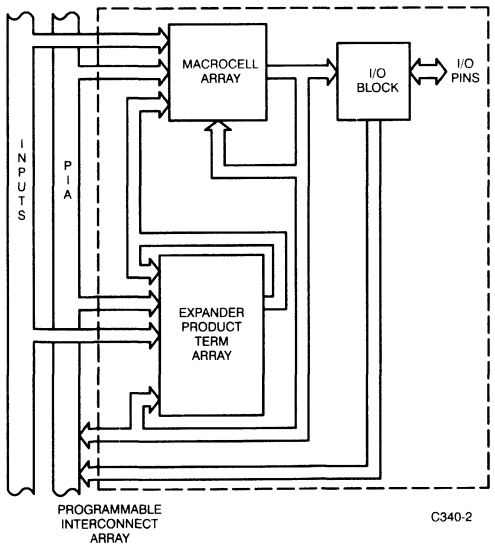


Figure 2. Typical LAB Block Diagram

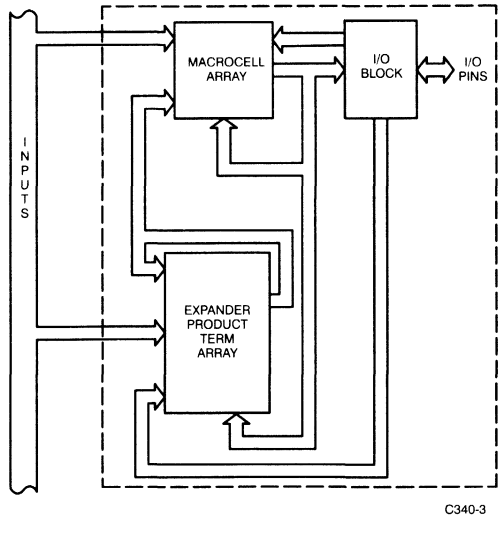


Figure 3. 7C344 LAB Block Diagram

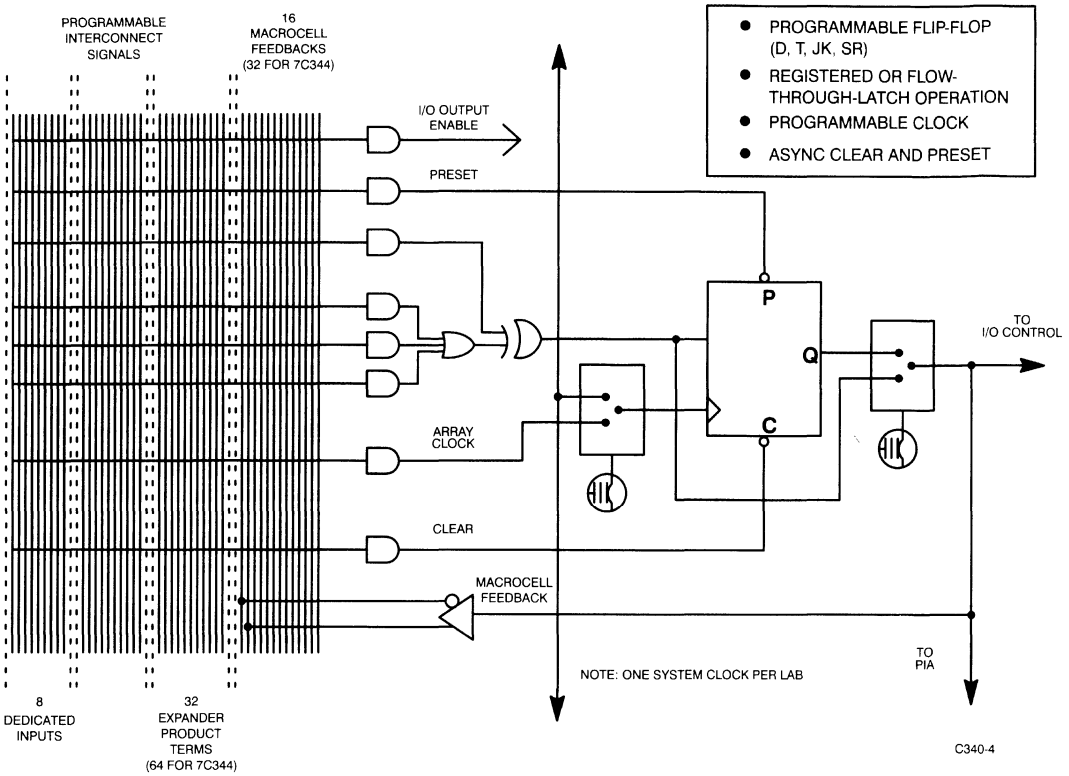


Figure 4. Macrocell Block Diagram

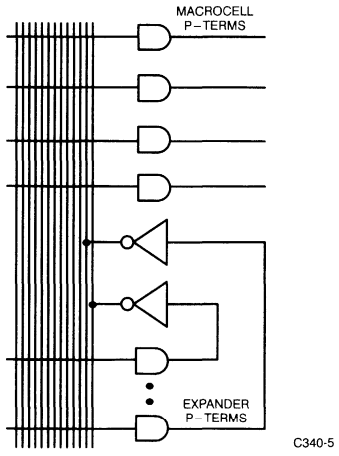


Figure 5. Expander Product Terms

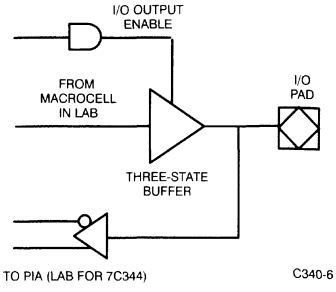


Figure 6. I/O Block Diagram

Functional Description (continued)

associated LAB. The feedback path from the I/O pin may feed other blocks within the LAB, as well as the PIA. By decoupling the I/O pins from the flip-flops, all the registers in the LAB are "buried," allowing the I/O pins to be used as dedicated outputs, bidirectional outputs, or as additional dedicated inputs. Therefore, applications requiring many buried flip-flops, such as counters, shift registers, and state machines, no longer consume both the macrocell register and the associated I/O pin, as in earlier devices.

The Programmable Interconnect Array

PLD density and speed has traditionally been limited by signal routing; i.e., getting signals from one macrocell to another. For smaller devices, a single array is used and all signals are available to all macrocells. But as the devices increase in density, the number of signals being routed becomes very large, increasing the amount of silicon used for interconnections. Also, because the signal must be global, the added loading on the internal connection path reduces the overall speed performance of the device. The MAX architecture solves these problems. It is based on the concept of small, flexible logic array blocks that, in the larger devices, are interconnected by a PIA.

The PIA solves interconnect limitations by routing only the signals needed by each LAB. The architecture is designed so that every signal on the chip is within the PIA. The PIA is then programmed to give each LAB access to the signals that it requires. Consequently, each LAB receives only the signals needed. This effectively solves any routing problems that may arise in a design without degrading the performance of the device. Unlike masked or programmable gate arrays, which induce variable delays dependent on routing, the PIA has a fixed delay from point to point. This eliminates undesired skews among logic signals, which may cause glitches in internal or external logic.

Development Software Support

Warp2

Warp2 is a state-of-the-art VHDL compiler for designing with Cypress PLDs and PROMs. *Warp2* utilizes a proper subset of IEEE 1076 VHDL as its Hardware Description Language (HDL) for design entry. VHDL provides a number of significant benefits for the design entry process. *Warp2* accepts VHDL input, synthesizes and optimizes the entered design, and outputs a JEDEC map for the desired device. For simulation, *Warp2* provides the graphical waveform simulator from the PLD ToolKit.

VHDL (VHSIC Hardware Description Language) is an open, powerful, non-proprietary language that is a standard for behavioral design entry and simulation. It is already mandated for use by the Department of Defense, and supported by every major vendor of CAE tools. VHDL allows designers to learn a single language that is useful for all facets of the design process.

Warp3

Warp3 is a sophisticated design tool that is based on the latest version of ViewLogic's CAE design environment. *Warp3* features schematic capture (ViewDraw™), VHDL waveform simulation (ViewSim™), a VHDL debugger, and VHDL synthesis, all integrated in a graphical design environment. *Warp3* is available on PCs using Windows® 3.1 or subsequent versions, and on Sun workstations.

For further information on *Warp* software, see the *Warp2* and *Warp3* datasheets contained in this data book.

Ordering Information

Device Adapters

CY3340	Adapter for CY7C341 in PLCC packages.
CY3340R	Adapter for CY7C341 in PGA packages.
CY3342	Adapter for CY7C342 in PLCC packages.
CY3342F	Adapter for CY7C342 in Flatpack packages.
CY3342R	Adapter for CY7C342 in PGA packages.
CY3342B	Adapter for CY7C342B in PLCC packages
CY3342BR	Adapter for CY7C342B in PGA packages.
CY33435	Adapter for CY7C343 in PLCC packages.
CY3344	Adapter for CY7C344 in DIP and PLCC packages.
CY3346	Adapter for CY7C346 in PLCC packages
CY3346N	Adapter for CY7C346 in PQFP packages
CY3346R	Adapter for CY7C346 in PGA packages

3

Cross Reference

ALTERA	CYPRESS
PREFIX:EPM	PREFIX:CY
5032DC	7C344-25WC
5032DC-2	7C344-20WC
5032DC-15	7C344-15WC
5032DC-17	Call Factory
5032DC-20	7C344-20WC
5032DC-25	7C344-25WC
5032DM	7C344-25WMB
5032DM-25	7C344-25WMB
5032JC	7C344-25HC
5032JC-2	7C344-20HC
5032JC-15	7C344-15HC
5032JC-17	Call Factory
5032JC-20	7C344-20HC
5032JC-25	7C344-25HC
5032JI-20	7C344-20HI
5032JM	7C344-25HMB
5032JM-25	7C344-25HMB
5032LC	7C344-25JC
5032LC-2	7C344-20JC
5032LC-15	7C344-15JC
5032LC-17	Call Factory
5032LC-20	7C344-20JC
5032LC-25	7C344-25JC
5032PC	7C344-25PC
5032PC-2	7C344-20PC
5032PC-15	7C344-15PC
5032PC-17	Call Factory
5032PC-20	7C344-20PC
5032PC-25	7C344-25PC
5064JC	7C343-35HC
5064JC-1	7C343-25HC
5064JC-2	7C343-30HC
5064JI	7C343-35HI
5064JM	7C343-35HMB
5064LC	7C343-35JC
5064LC-1	7C343-25JC
5064LC-2	7C343-30JC
5128AGC-1	7C342B-12RC
5128AGC-2	7C342B-15RC
5128AGC-3	7C342B-20RC
5128AJC-1	7C342B-12HC
5128AJC-2	7C342B-15HC
5128AJC-3	7C342B-20HC
5128ALC-1	7C342B-12JC
5128ALC-2	7C342B-15JC
5128ALC-3	7C342B-20JC
5128GC	7C342-35RC
5128GC-1	7C342-25RC
5128GC-2	7C342-30RC
5128GM	7C342-35RMB
5128JC	7C342-35HC
5128JC-1	7C342-25HC
5128JC-2	7C342-30HC
5128JI	7C342-35HI
5128JI-2	7C342-30HI
5128JM	7C342-35HMB
5128LC	7C342-35JC
5128LC-1	7C342-25JC
5128LC-2	7C342-30JC
5128LI	7C342-35JI
5128LI-2	7C342-30HI
5130GC	7C346-35RC
5130GC-1	7C346-25RC

ALTERA	CYPRESS
5130GC-2	7C346-30RC
5130GM	7C346-35RM
5130JC	7C346-35HC
5130JC-1	7C346-25HC
5130JC-2	7C346-30HC
5130JM	7C346-35HM
5130LC	7C346-35JC
5130LC-1	7C346-25JC
5130LC-2	7C346-30JC
5130LI	7C346-35JI
5130LI-2	7C346-30JI
5130QC	7C346-35NC
5130QC-1	7C346-25NC
5130QC-2	7C346-30NC
5130QI	7C346-35NI
5192AGC-1	7C341B-15RC
5192AGC-2	7C341B-20RC
5192AJC-1	7C341B-15HC
5192AJC-2	7C341B-20HC
5192ALC-1	7C341B-15JC
5192ALC-2	7C431B-20JC
5192GC	7C341-35RC
5192GC-1	7C341-25RC
5192GC-2	7C341-30RC
5192JC	7C341-35HC
5192JC-1	7C341-25HC
5192JC-2	7C341-30HC
5192JI	7C341-35HI
5192LC	7C341-35JC
5192LC-1	7C341-25JC
5192LC-2	7C341-30JC

Document #: 38-00087-D

CY7C341
CY7C341B

192-Macrocell MAX® EPLD

Features

- **192 macrocells in 12 LABs**
- **8 dedicated inputs, 64 bidirectional I/O pins**
- **0.8-micron double-metal CMOS EPROM technology (CY7C341)**
- **Advanced 0.65-micron CMOS technology to increase performance (CY7C341B)**
- **Programmable interconnect array**
- **384 expander product terms**
- **Available in 84-pin HLCC, PLCC, and PGA packages**

Functional Description

The CY7C341 and CY7C341B are Erasable Programmable Logic Devices (EPLD) in which CMOS EPROM cells are used to configure logic functions within the device. The MAX architecture is 100% user configurable allowing the devices to accommodate a variety of independent logic functions.

The 192 macrocells in the CY7C341/CY7C341B are divided into 12 Logic Array Blocks (LABs), 16 per LAB. There are 384 expander product terms, 32 per LAB, to be used and shared by the macrocells within each LAB. Each LAB is interconnected with a programmable interconnect array, allowing all signals to be routed throughout the chip.

The speed and density of the CY7C341/CY7C341B allows them to be used in a wide range of applications, from replacement of large amounts of 7400 series TTL logic, to complex controllers and multifunction chips. With greater than 37 times the functionality of 20-pin PLDs, the CY7C341/CY7C341B allows the replacement of over 75 TTL devices. By replacing large amounts of logic, the CY7C341 and CY7C341B reduces board space, part count, and increases system reliability.

Each LAB contains 16 macrocells. In LABs A, F, G, and L, 8 macrocells are connected to I/O pins and 8 are buried, while for LABs B, C, D, E, H, I, J, and K, 4 macrocells are connected to I/O pins and 12 are buried. Moreover, in addition to the I/O and buried macrocells, there are 32 single product term logic expanders in each LAB. Their use greatly enhances the capability of the macrocells without increasing the number of product terms in each macrocell.

Logic Array Blocks

There are 12 logic array blocks in the CY7C341/CY7C341B. Each LAB consists of a macrocell array containing 16 macrocells, an expander product term array containing 32 expanders, and an I/O block. The LAB is fed by the programmable interconnect array and the dedicated input bus. All macrocell feedbacks go to the macrocell array, the expander array, and the programmable interconnect array. Expanders feed themselves and the macrocell array. All I/O feedbacks go to the programmable interconnect array so that they may be accessed by macrocells in other LABs as well as the macrocells in the LAB in which they are situated.

Externally, the CY7C341/CY7C341B provide 8 dedicated inputs, one of which may be used as a system clock. There are 64 I/O pins that may be individually configured for input, output, or bidirectional data flow.

Programmable Interconnect Array

The Programmable Interconnect Array (PIA) solves interconnect limitations by routing only the signals needed by each logic array block. The inputs to the PIA are the outputs of every macrocell within the device and the I/O pin feedback of every pin on the device.

Unlike masked or programmable gate arrays, which induce variable delay dependent on routing, the PIA has a fixed delay. This eliminates undesired skews among logic signals, which may cause glitches in internal or external logic. The fixed delay, regardless of programmable interconnect array configuration, simplifies design by assuring that internal signal skews or races are avoided. The result is ease of design implementation, often in a single pass, without the multiple internal logic placement and routing iterations required for a programmable gate array to achieve design timing objectives.

Timing Delays

Timing delays within the CY7C341/CY7C341B may be easily determined using *Warp2*™, *Warp3*™, or MAX+PLUS® software or by the model shown in *Figure 1*. The CY7C341/CY7C341B have fixed internal delays, allowing the user to determine the worst case timing delays for any design. For complete timing information, the *Warp3* or MAX+PLUS software provides a timing simulator.

Design Recommendations

For proper operation, input and output pins must be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic level (either V_{CC} or GND). Each set of V_{CC} and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 µF must be connected between V_{CC} and GND. For the most effective decoupling, each V_{CC} pin should be separately decoupled to GND, directly at the device. Decoupling capacitors should have good frequency response, such as monolithic ceramic types.

Design Security

The CY7C341/CY7C341B contain a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the device.

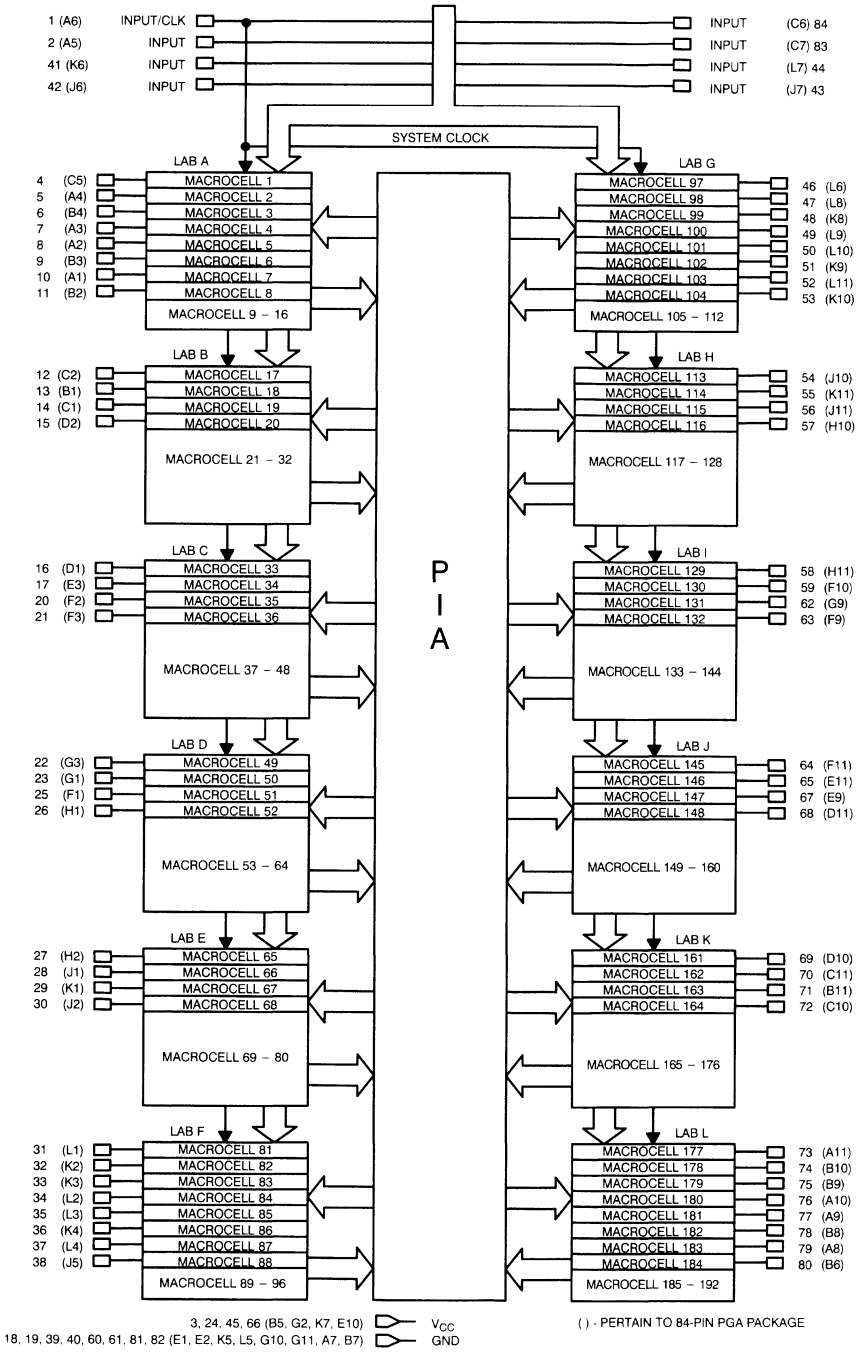
Selection Guide

		7C341B–15	7C341B–20	7C341–25 7C341B–25	7C341–30 7C341B–30	7C341–35 7C341B–35	7C341–40
Maximum Access Time (ns)		15	20	25	30	35	40
Maximum Operating Current (mA)	Commercial	380	380	380	380	380	
	Industrial	480	480	480	480	480	
	Military		480	480	480	480	480
Maximum Standby Current (mA)	Commercial	360	360	360	360	360	
	Industrial	435	435	435	435	435	
	Military		435	435	435	435	435

Shaded areas contain preliminary information.

MAX is a registered trademark of Altera Corporation. *Warp2* and *Warp3* are trademarks of Cypress Semiconductor Corporation.

Logic Block Diagram



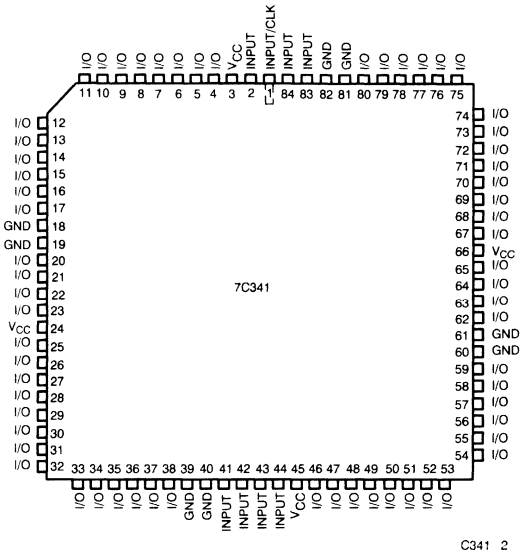
Design Security (continued)

The CY7C341/CY7C341B is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

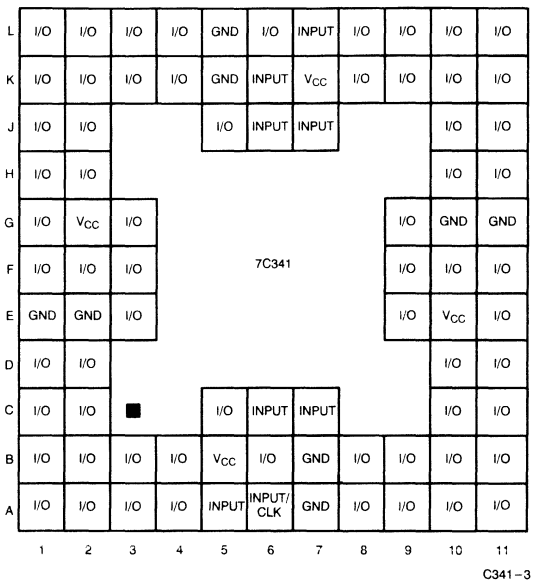
The erasable nature of these devices allows test programs to be used and erased during early stages of the production flow. The devices also contain on-board logic test circuitry to allow verification of function and AC specification once encapsulated in non-windowed packages.

Pin Configurations

PLCC/HLCC
Top View



PGA
Bottom View



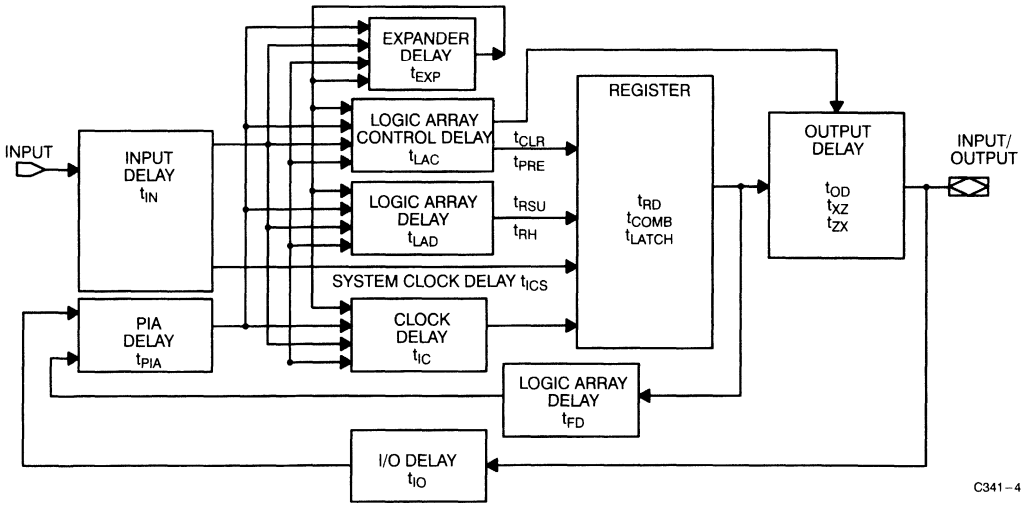


Figure 1. CY7C341 Internal Timing Model

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... 0°C to +70°C

Maximum Junction Temperature (Under Bias) ..... 150°C

Supply Voltage to Ground Potential ..... −2.0V to +7.0V

Maximum Power Dissipation ..... 2500 mW

DC V_{CC} or GND Current ..... 500 mA

DC Output Current, per Pin ..... −25 mA to +25 mA

DC Input Voltage[1] ..... −3.0V to +7.0V

DC Program Voltage 13.0V

Static Discharge Voltage ..... >1100V (per MIL-STD-883, method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	−40°C to +85°C	5V ± 10%
Military	−55°C to +125°C (Case)	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA			0.45	V
V_{IH}	Input HIGH Level			2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Level			−0.3	0.8	V
I_{IX}	Input Current	$GND \leq V_{IN} \leq V_{CC}$		−10	+10	μA
I_{OZ}	Output Leakage Current	$V_O = V_{CC}$ or GND		−40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND[3, 4]		−30	−90	mA
I_{CC1}	Power Supply Current (Standby)	$V_I = V_{CC}$ or GND (No Load)	Com'l		360	mA
			Mil/Ind		435	mA
I_{CC2}	Power Supply Current[5]	$V_I = V_{CC}$ or GND (No Load) f = 1.0 MHz[3, 5]	Com'l		380	mA
			Mil/Ind		480	mA
t_R (Recommended)	Input Rise Time				100	ns
t_F (Recommended)	Input Fall Time				100	ns

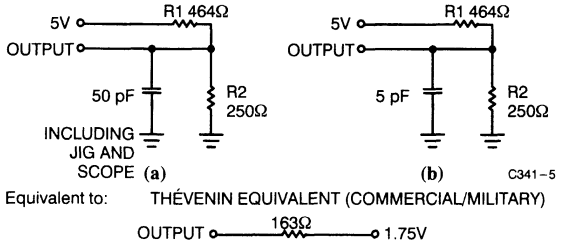
Capacitance[6]

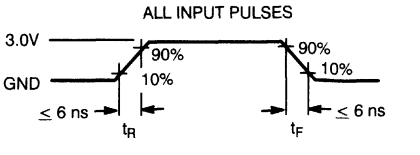
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		20	pF

Notes:

1. Minimum DC input is −0.3V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns.
2. Typical values are for T_A = 25°C and V_{CC} = 5V.
3. Guaranteed but not 100% tested.
4. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
5. This parameter is measured with device programmed as a 16-bit counter in each LAB and is tested periodically by sampling production material.
6. Part (a) in AC Test Load and Waveforms is used for all parameters except t_{ER} and t_{XZ}, which is used for part (b) in AC Test Load and Waveforms. All external timing parameters are measured referenced to external pins of the device.

AC Test Loads and Waveforms





External Synchronous Switching Characteristics Over the Operating Range[6]

Parameter	Description		7C341B–15		7C341B–20		7C341–25 7C341B–25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[7]	Com'l		15		20		25	ns
		Mil				20		25	
t_{PD2}	I/O Input to Combinatorial Output Delay[8]	Com'l		25		33		40	ns
		Mil				33		40	
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[9]	Com'l		23		30		37	ns
		Mil				30		37	
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[3, 10]	Com'l		33		43		52	ns
		Mil				43		52	
t_{EA}	Input to Output Enable Delay[3, 7]	Com'l		15		20		25	ns
		Mil				20		25	
t_{ER}	Input to Output Disable Delay[6]	Com'l		15		20		25	ns
		Mil				20		25	
t_{CO1}	Synchronous Clock Input to Output Delay	Com'l		7		8		14	ns
		Mil				8		14	
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[3, 11]	Com'l		17		20		30	ns
		Mil				20		30	
t_{S1}	Dedicated Input or Feedback Set-up Time to Synchronous Clock Output[6, 12]	Com'l	10		13		15		ns
		Mil			13		15		
t_{S2}	I/O Input Set-up Time to Synchronous Clock Input[8]	Com'l	20		24		30		ns
		Mil			24		30		
t_H	Input Hold Time from Synchronous Clock Input[6]	Com'l	0		0		0		ns
		Mil			0		0		
t_{WH}	Synchronous Clock Input High Time	Com'l	5		7		8		ns
		Mil			7		8		
t_{WL}	Synchronous Clock Input Low Time	Com'l	5		7		8		ns
		Mil			7		8		
t_{RW}	Asynchronous Clear Width[3, 6]	Com'l	16		22		25		ns
		Mil			22		25		
t_{RR}	Asynchronous Clear Recovery[3, 7]	Com'l	16		22		25		ns
		Mil			22		25		
t_{RO}	Asynchronous Clear to Registered Output Delay[5]	Com'l		15		20		25	ns
		Mil				20		25	
t_{PW}	Asynchronous Preset Width[3, 6]	Com'l	15		20		25		ns
		Mil			20		25		
t_{PR}	Asynchronous Preset Recovery Time[3, 6]	Com'l	15		20		25		ns
		Mil			20		25		

Shaded areas contain preliminary information.

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External Synchronous Switching Characteristics Over the Operating Range[6](continued)

Parameter	Description		7C341B–15 Min.	7C341B–15 Max.	7C341B–20 Min.	7C341B–20 Max.	7C341–25 7C341B–25 Min.	7C341–25 7C341B–25 Max.	Unit
t_{PO}	Asynchronous Preset to Registered Output Delay[6]	Com'l		15		20		25	ns
		Mil				20		25	
t_{CF}	Synchronous Clock to Local Feedback Input[3, 13]	Com'l		3		3		3	ns
		Mil				3		3	
t_P	External Synchronous Clock Period ($1/f_{MAX3}$)[3]	Com'l	12		14		16		ns
		Mil			14		16		
f_{MAX1}	External Feedback Maximum Frequency ($1/(t_{CO1} + t_{S1})$)[3, 14]	Com'l	58.8		50		34.5		MHz
		Mil			50		34.5		
f_{MAX2}	Internal Local Feedback Maximum Frequency, lesser of ($1/(t_{S1} + t_{CF})$) or ($1/t_{CO1}$)[3, 15]	Com'l	76.9		62.5		55.5		MHz
		Mil			62.5		55.5		
f_{MAX3}	Data Path Maximum Frequency, least of $1/(t_{WL} + t_{WH})$, $1/(t_{S1} + t_H)$, or ($1/t_{CO1}$)[3, 16]	Com'l	100		71.4		62.5		MHz
		Mil			71.4		62.5		
f_{MAX4}	Maximum Register Toggle Frequency ($1/(t_{WL} + t_{WH})$)[3, 17]	Com'l	100		71.4		62.5		MHz
		Mil			71.4		62.5		
t_{OH}	Output Data Stable Time from Synchronous Clock Input[3, 18]	Com'l	3		3		3		ns
		Mil			3		3		

Shaded areas contain preliminary information.

Notes:

7. This specification is a measure of the delay from input signal applied to a dedicated input to combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function.
   When this note is applied to any parameter specification it indicates that the signal (data, asynchronous clock, asynchronous clear, and/or asynchronous preset) is applied to a dedicated input only and no signal path (either clock or data) employs expander logic.
   If an input signal is applied to an I/O pin an additional delay equal to t_{PIA} should be added to the comparable delay for a dedicated input. If expanders are used, add the maximum expander delay t_{EXP} to the overall delay for the comparable delay without expanders.
8. This specification is a measure of the delay from input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.
9. This specification is a measure of the delay from an input signal applied to a dedicated input to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic functions and includes the worst-case expander logic delay for one pass through the expander logic.
10. This specification is a measure of the delay from an input signal applied to an I/O macrocell pin to any output. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
11. This specification is a measure of the delay from synchronous register clock to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used, register is synchronously clocked and all feedback is within the same LAB. This parameter is tested periodically by sampling production material.
12. If data is applied to an I/O input for capture by a macrocell register, the I/O pin set-up time minimums should be observed. These parameters are t_{S2} for synchronous operation and t_{AS2} for asynchronous operation.
13. This specification is a measure of the delay associated with the internal register feedback path. This is the delay from synchronous clock to LAB logic array input. This delay plus the register set-up time, t_{S1}, is the minimum internal period for an internal synchronous state machine configuration. This delay is for feedback within the same LAB. This parameter is tested periodically by sampling production material.
14. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which a state machine configuration with external feedback can operate. It is assumed that all data inputs and feedback signals are applied to dedicated inputs. All feedback is assumed to be local originating within the same LAB.
15. This specification indicates the guaranteed maximum frequency at which a state machine, with internal-only feedback, can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{CO1}$.
16. This frequency indicates the maximum frequency at which the device may operate in data path mode (dedicated input pin to output pin). This assumes data input signals are applied to dedicated input pins and no expander logic is used. If any of the data inputs are I/O pins, t_{S2} is the appropriate t_S for calculation.
17. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which an individual output or buried register can be cycle by a clock signal applied to the dedicated clock input pin.
18. This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.

External Synchronous Switching Characteristics Over the Operating Range[6] (continued)

Parameter	Description		7C341–30 7C341B–30 Min.	7C341–30 7C341B–30 Max.	7C341–35 7C341B–35 Min.	7C341–35 7C341B–35 Max.	7C341–40 Min.	7C341–40 Max.	Unit
t_{PD1}	Dedicated Input to Combinatorial Output Delay[7]	Com'l		30		35			ns
		Mil		30		35		40	
t_{PD2}	I/O Input to Combinatorial Output Delay[8]	Com'l		45		55			ns
		Mil		45		55		65	
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[9]	Com'l		44		55			ns
		Mil		44		55		65	
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[3, 10]	Com'l		59		75			ns
		Mil		59		75		90	
t_{EA}	Input to Output Enable Delay[3, 7]	Com'l		30		35			ns
		Mil		30		35		40	
t_{ER}	Input to Output Disable Delay[6]	Com'l		30		35			ns
		Mil		30		35		40	
t_{CO1}	Synchronous Clock Input to Output Delay	Com'l		16		20			ns
		Mil		16		20		23	
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[3, 11]	Com'l		35		42			ns
		Mil		35		42		48	
t_{S1}	Dedicated Input or Feedback Set-up Time to Synchronous Clock Output[6,12]	Com'l	20		25				ns
		Mil	20		25		28		
t_{S2}	I/O Input Set-up Time to Synchronous Clock Input[8]	Com'l	39		45				ns
		Mil	39		45		52		
t_H	Input Hold Time from Synchronous Clock Input[6]	Com'l	0		0				ns
		Mil	0		0		0		
t_{WH}	Synchronous Clock Input High Time	Com'l	10		12.5				ns
		Mil	10		12.5		15		
t_{WL}	Synchronous Clock Input Low Time	Com'l	10		12.5				ns
		Mil	10		12.5		15		
t_{RW}	Asynchronous Clear Width[3, 6]	Com'l	30		35				ns
		Mil	30		35		40		
t_{RR}	Asynchronous Clear Recovery[3, 7]	Com'l	30		35				ns
		Mil	30		35		40		
t_{RO}	Asynchronous Clear to Registered Output Delay[5]	Com'l		30		35			ns
		Mil		30		35		40	
t_{PW}	Asynchronous Preset Width[3, 6]	Com'l	30		35				ns
		Mil	30		35		40		
t_{PR}	Asynchronous Preset Recovery Time[3, 6]	Com'l	30		35				ns
		Mil	30		35		40		

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External Synchronous Switching Characteristics Over the Operating Range[6] (continued)

Parameter	Description		7C341–30 7C341B–30		7C341–35 7C341B–35		7C341–40		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PO}	Asynchronous Preset to Registered Output Delay[6]	Com'l		30		35			ns
		Mil		30		35		40	
t_{CF}	Synchronous Clock to Local Feedback Input[3, 13]	Com'l		3		5			ns
		Mil		3		5		7	
t_P	External Synchronous Clock Period ($1/f_{MAX3}$)[3]	Com'l	20		25				ns
		Mil	20		25		30		
f_{MAX1}	External Feedback Maximum Frequency ($1/(t_{CO1} + t_{S1})$)[3, 14]	Com'l	27.7		22.2				MHz
		Mil	27.7		22.2		19.6		
f_{MAX2}	Internal Local Feedback Maximum Frequency, lesser of ($1/(t_{S1} + t_{CF})$) or ($1/t_{CO1}$)[3, 15]	Com'l	43		33				MHz
		Mil	43		33		28.5		
f_{MAX3}	Data Path Maximum Frequency, least of $1/(t_{WL} + t_{WH})$, $1/(t_{S1} + t_H)$, or ($1/t_{CO1}$)[3, 16]	Com'l	50		40.0				MHz
		Mil	50		40.0		33.3		
f_{MAX4}	Maximum Register Toggle Frequency ($1/(t_{WL} + t_{WH})$)[3, 17]	Com'l	50		40.0				MHz
		Mil	50		40.0		33.3		
t_{OH}	Output Data Stable Time from Synchronous Clock Input[3, 18]	Com'l	3		3				ns
		Mil	3		3		3		

External Asynchronous Switching Characteristics Over the Operating Range[6]

Parameter	Description		7C341B–15 Min.	7C341B–15 Max.	7C341B–20 Min.	7C341B–20 Max.	7C341–25 7C341B–25 Min.	7C341–25 7C341B–25 Max.	Unit
t_{ACO1}	Dedicated Asynchronous Clock Input to Output Delay[6]	Com'l		15		20		25	ns
		Mil				20		25	
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output [19]	Com'l		25		32		40	ns
		Mil				32		40	
t_{AS1}	Dedicated Input or Feedback Set-up Time to Asynchronous Clock Input[6]	Com'l	5		5		5		ns
		Mil			5		5		
t_{AS2}	I/O Input Set-Up Time to Asynchronous Clock Input[6]	Com'l	14		18		20		ns
		Mil			18		20		
t_{AH}	Input Hold Time from Asynchronous Clock Input[6]	Com'l	5		6		6		ns
		Mil			6		6		
t_{AWH}	Asynchronous Clock Input HIGH Time[6]	Com'l	9		10		11		ns
		Mil			10		11		
t_{AWL}	Asynchronous Clock Input LOW Time[6, 20]	Com'l	7		8		9		ns
		Mil			8		9		
t_{ACF}	Asynchronous Clock to Local Feedback Input[21]	Com'l		11		13		15	ns
		Mil				13		15	
t_{AP}	External Asynchronous Clock Period ($1/f_{MAX4}$)	Com'l	16		18		20		ns
		Mil			18		20		
f_{MAXA1}	External Feedback Maximum Frequency in Asynchronous Mode $1/(t_{ACO1} + t_{AS1})$[22]	Com'l	50		40		33.3		MHz
		Mil			40		33.3		
f_{MAXA2}	Maximum Internal Asynchronous Frequency[23]	Com'l	62.5		55.5		50		MHz
		Mil			55.5		50		
f_{MAXA3}	Data Path Maximum Frequency in Asynchronous Mode[24]	Com'l	62.5		50		40		MHz
		Mil			50		40		
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[25]	Com'l	62.5		55.5		50		MHz
		Mil			55.5		50		
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[26]	Com'l	15		15		15		ns
		Mil			15		15		

Shaded areas contain preliminary information.

Notes:

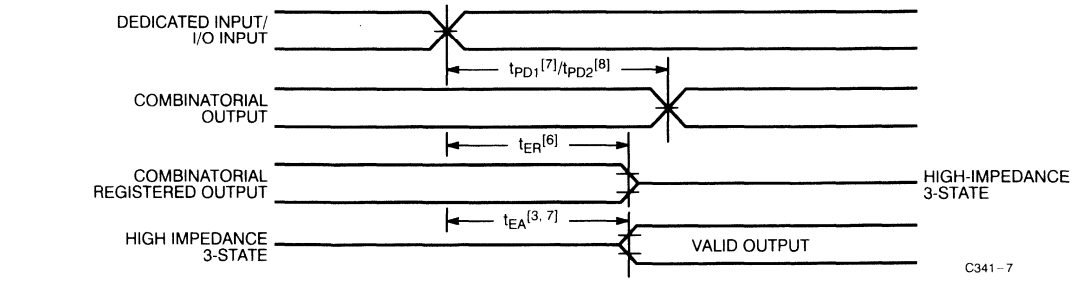
19. This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used in the logic of combinatorial output or the asynchronous clock input. The clock signal is applied to the dedicated clock input pin and all feedback is within a single LAB. This parameter is tested periodically by sampling production material.
20. This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge triggering, the t_{AWH} and t_{AWL} parameters must be swapped. If a given input is used to clock multiple registers with both positive and negative polarity, t_{AWH} should be used for both t_{AWH} and t_{AWL}.
21. This specification is a measure of the delay associated with the internal register feedback path for an asynchronous clock to LAB logic array input. This delay plus the asynchronous register set-up time, t_{AS1}, is the minimum internal period for an internal asynchronously clocked state machine configuration. This delay is for feedback within the same LAB, and assumes there is no expander logic in the clock path and the clock input signal is applied to a dedicated input pin. This parameter is tested periodically by sampling production material.
22. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that all data inputs, clock inputs, and feedback signals are applied to dedicated inputs, and that no expander logic is employed in the clock signal path or data path.
23. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal-only feedback can operate. This parameter is determined by the lesser of $(1/t_{ACF} + t_{AS1})$ or $(1/(t_{AWH} + t_{AWL}))$. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO1}$.
24. This frequency is the maximum frequency at which the device may operate in the asynchronously clocked data path mode. This specification is determined by the least of $1/(t_{AWH} + t_{AWL})$, $1/(t_{AS1} + t_{AH})$ or $1/t_{ACO1}$. It assumes data and clock input signals are applied to dedicated input pins and no expander logic is used.
25. This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to an external dedicated input pin.
26. This parameter indicates the minimum time that the previous register output data is maintained on the output after an asynchronous register clock input applied to an external dedicated input pin.

External Asynchronous Switching Characteristics Over the Operating Range[6] (continued)

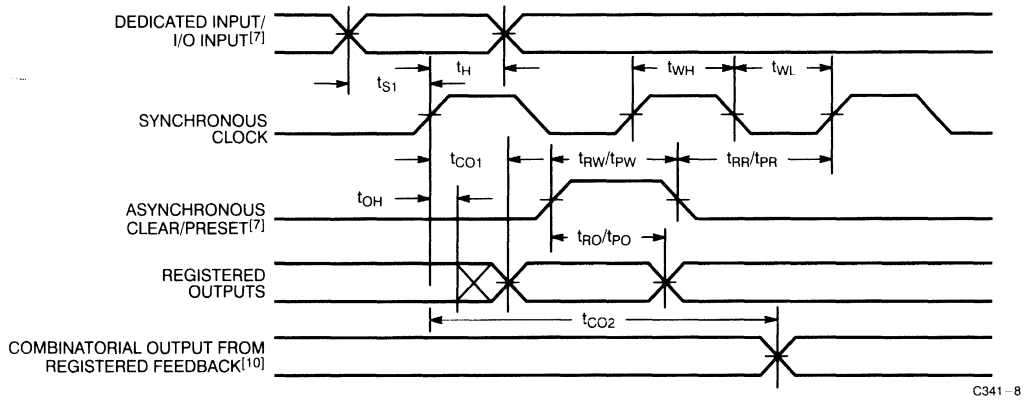
Parameter	Description		7C341–30 7C341B–30		7C341–35 7C341B–35		7C341–40		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACO1}	Dedicated Asynchronous Clock Input to Output Delay[6]	Com'l		30		35			ns
		Mil		30		35		45	
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output [19]	Com'l		46		55			ns
		Mil		46		55		64	
t_{AS1}	Dedicated Input or Feedback Set-up Time to Asynchronous Clock Input[6]	Com'l	6		8				ns
		Mil	6		8		10		
t_{AS2}	I/O Input Set-Up Time to Asynchronous Clock Input[6]	Com'l	27		30				ns
		Mil	27		30		33		
t_{AH}	Input Hold Time from Asynchronous Clock Input[6]	Com'l	8		10				ns
		Mil	8		10		12		
t_{AWH}	Asynchronous Clock Input HIGH Time[6]	Com'l	14		16				ns
		Mil	14		16		20		
t_{AWL}	Asynchronous Clock Input LOW Time[6, 20]	Com'l	11		14				ns
		Mil	11		14		20		
t_{ACF}	Asynchronous Clock to Local Feedback Input[21]	Com'l		18		22			ns
		Mil		18		22		26	
t_{AP}	External Asynchronous Clock Period ($1/f_{MAX4}$)	Com'l	25		30				ns
		Mil	25		30		40		
f_{MAXA1}	External Feedback Maximum Frequency in Asynchronous Mode $1/(t_{ACO1} + t_{AS1})$[22]	Com'l	27		23				MHz
		Mil	27		23		18		
f_{MAXA2}	Maximum Internal Asynchronous Frequency[23]	Com'l	40		33.3				MHz
		Mil	40		33.3		25		
f_{MAXA3}	Data Path Maximum Frequency in Asynchronous Mode[24]	Com'l	33.3		28.5				MHz
		Mil	33.3		28.5		22.2		
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[25]	Com'l	40		33.3				MHz
		Mil	40		33.3		25		
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[26]	Com'l	15		15				ns
		Mil	15		15		15		

Switching Waveforms

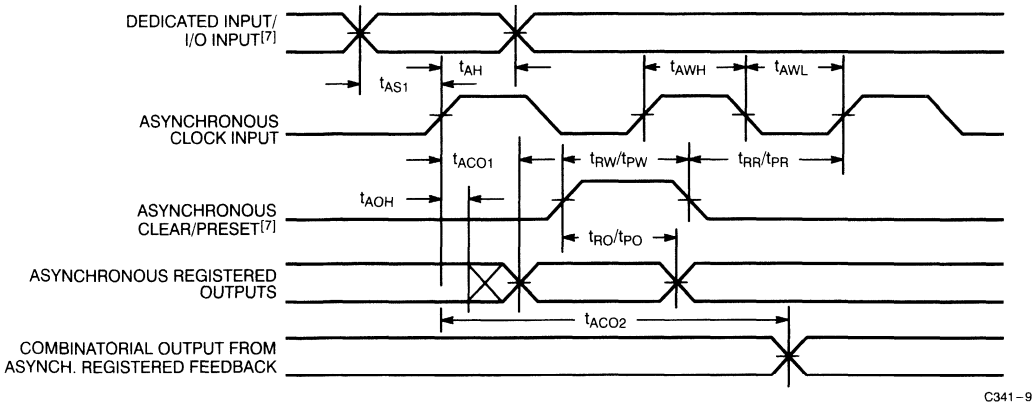
External Combinatorial



External Synchronous



External Asynchronous



Internal Switching Characteristics Over the Operating Range[1]

Parameter	Description		7C341B–15		7C341B–20		7C341–25 7C341B–25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay	Com'l		3		4		5	ns
		Mil				4		5	
t_{IO}	I/O Input Pad and Buffer Delay	Com'l		3		4		6	ns
		Mil				4		6	
t_{EXP}	Expander Array Delay	Com'l		8		10		12	ns
		Mil				10		12	
t_{LAD}	Logic Array Data Delay	Com'l		8		10		12	ns
		Mil				10		12	
t_{LAC}	Logic Array Control Delay	Com'l		5		7		10	ns
		Mil				7		10	
t_{OD}	Output Buffer and Pad Delay	Com'l		3		3		5	ns
		Mil				3		5	
t_{ZX}	Output Buffer Enable Delay[27]	Com'l		5		5		10	ns
		Mil				5		10	
t_{XZ}	Output Buffer Disable Delay	Com'l		5		5		10	ns
		Mil				5		10	
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	Com'l	4		5		6		ns
		Mil			5		6		
t_{RH}	Register Hold Time Relative to Clock Signal at Register	Com'l	4		5		6		ns
		Mil			5		6		
t_{LATCH}	Flow-Through Latch Delay	Com'l		1		2		3	ns
		Mil				2		3	
t_{RD}	Register Delay	Com'l		1		1		1	ns
		Mil				1		1	
t_{COMB}	Transparent Mode Delay[28]	Com'l		1		2		3	ns
		Mil				2		3	
t_{CH}	Clock High Time	Com'l	4		6		8		ns
		Mil			6		8		
t_{CL}	Clock Low Time	Com'l	4		6		8		ns
		Mil			6		8		
t_{IC}	Asynchronous Clock Logic Delay	Com'l		6		8		14	ns
		Mil				8		14	
t_{ICS}	Synchronous Clock Delay	Com'l		0.5		0.5		2	ns
		Mil				0.5		2	
t_{FD}	Feedback Delay	Com'l		1		1		1	ns
		Mil				1		1	
t_{PRE}	Asynchronous Register Preset Time	Com'l		3		3		5	ns
		Mil				3		5	
t_{CLR}	Asynchronous Register Clear Time	Com'l		3		3		5	ns
		Mil				3		5	
t_{PCW}	Asynchronous Preset and Clear Pulse Width	Com'l	3		4		5		ns
		Mil			4		5		
t_{PCR}	Asynchronous Preset and Clear Recovery Time	Com'l	3		4		5		ns
		Mil			4		5		
t_{PIA}	Programmable Interconnect Array Delay Time	Com'l		10		12		14	ns
		Mil				12		14	

Shaded areas contain preliminary information

Notes:

27. Sample tested only for an output change of 500 mV.
28. This specification guarantees the maximum combinatorial delay associated with the macrocell register bypass when the macrocell is configured for combinatorial operation.

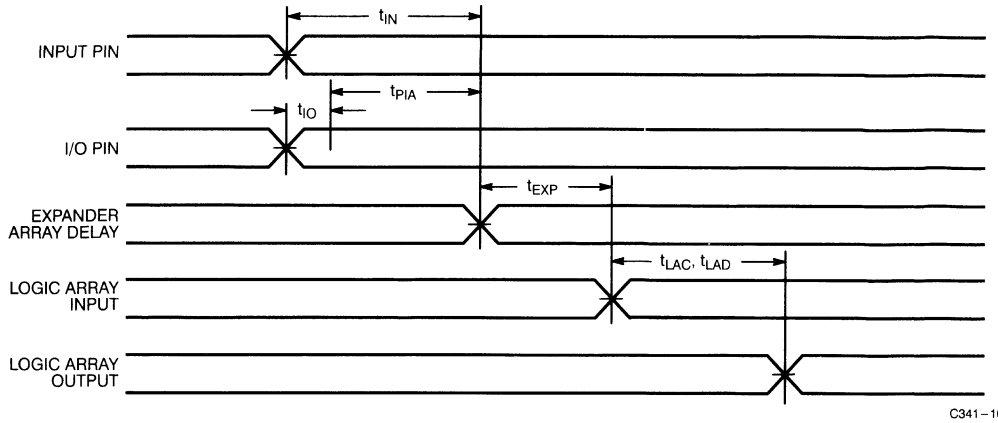
Internal Switching Characteristics Over the Operating Range[1] (continued)

Parameter	Description		7C341–30 7C341B–30		7C341–35 7C341B–35		7C341–40		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay	Com'l		7		9			ns
		Mil		7		9		11	
t_{IO}	I/O Input Pad and Buffer Delay	Com'l		6		9			ns
		Mil		6		9		12	
t_{EXP}	Expander Array Delay	Com'l		14		20			ns
		Mil		14		20		25	
t_{LAD}	Logic Array Data Delay	Com'l		14		16			ns
		Mil		14		16		18	
t_{LAC}	Logic Array Control Delay	Com'l		12		13			ns
		Mil		12		13		14	
t_{OD}	Output Buffer and Pad Delay	Com'l		5		6			ns
		Mil		5		6		7	
t_{ZX}	Output Buffer Enable Delay[27]	Com'l		11		13			ns
		Mil		11		13		15	
t_{XZ}	Output Buffer Disable Delay	Com'l		11		13			ns
		Mil		11		13		15	
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	Com'l	8		10				ns
		Mil	8		10		12		
t_{RH}	Register Hold Time Relative to Clock Signal at Register	Com'l	8		10				ns
		Mil	8		10		12		
t_{LATCH}	Flow-Through Latch Delay	Com'l		4		4			ns
		Mil		4		4		4	
t_{RD}	Register Delay	Com'l		2		2			ns
		Mil		2		2		2	
t_{COMB}	Transparent Mode Delay[28]	Com'l		4		4			ns
		Mil		4		4		4	
t_{CH}	Clock High Time	Com'l	10		12.5				ns
		Mil	10		12.5		15		
t_{CL}	Clock Low Time	Com'l	10		12.5				ns
		Mil	10		12.5		15		
t_{IC}	Asynchronous Clock Logic Delay	Com'l		16		18			ns
		Mil		16		18		20	
t_{ICS}	Synchronous Clock Delay	Com'l		2		3			ns
		Mil		2		3		4	
t_{FD}	Feedback Delay	Com'l		1		2			ns
		Mil		1		2		3	
t_{PRE}	Asynchronous Register Preset Time	Com'l		6		7			ns
		Mil		6		7		8	
t_{CLR}	Asynchronous Register Clear Time	Com'l		6		7			ns
		Mil		6		7		8	
t_{PCW}	Asynchronous Preset and Clear Pulse Width	Com'l	6		7				ns
		Mil	6		7		8		
t_{PCR}	Asynchronous Preset and Clear Recovery Time	Com'l	6		7				ns
		Mil	6		7		8		
t_{PIA}	Programmable Interconnect Array Delay Time	Com'l		16		20			ns
		Mil		16		20		24	

3

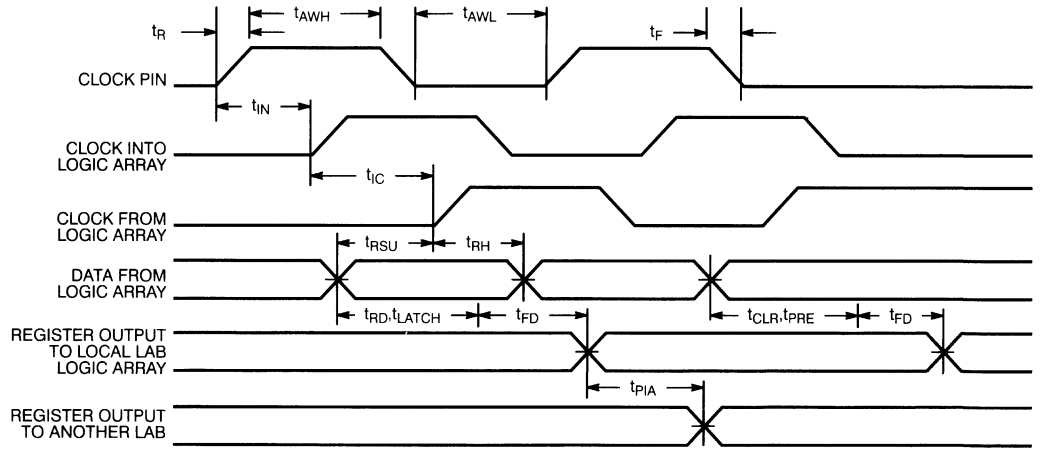
Switching Waveforms (continued)

Internal Combinatorial



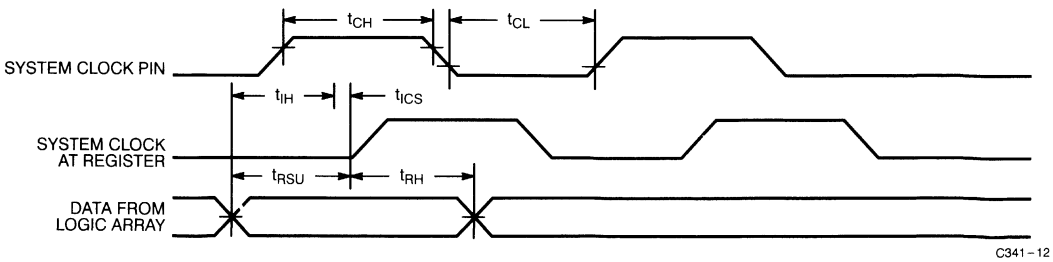
C341-10

Internal Asynchronous



C341-11

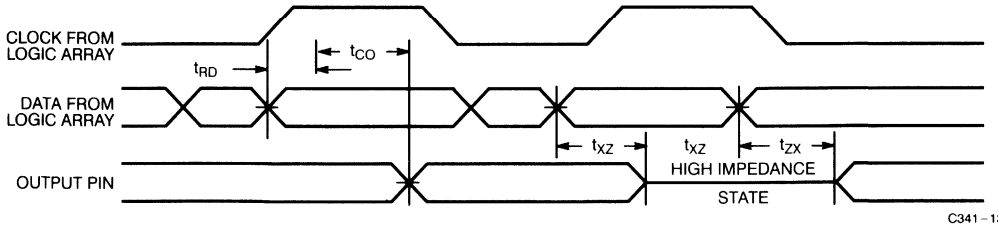
Internal Synchronous



C341-12

Switching Waveforms (continued)

Internal Synchronous



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C341B–15HC/HI	H84	84-Lead Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C341B–15JC/JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C341B–15RC/RI	R84	84-Lead Windowed Pin Grid Array	
20	CY7C341B–20HC/HI	H84	84-Lead Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C341B–20JC/JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C341B–20RC/RI	R84	84-Lead Windowed Pin Grid Array	
	CY7C341B–20HMB	H84	84-Lead Windowed Leaded Chip Carrier	Military
	CY7C341B–20RMB	R84	84-Lead Windowed Pin Grid Array	
25	CY7C341–25HC/HI	H84	84-Lead Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C341–25JC/JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C341–25RC/RI	R84	84-Lead Windowed Pin Grid Array	
	CY7C341B–25HC/HI	H84	84-Lead Windowed Leaded Chip Carrier	
	CY7C341B–25JC/JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C341B–25RC/RI	R84	84-Lead Windowed Pin Grid Array	
	CY7C341B–25HMB	H84	84-Lead Windowed Leaded Chip Carrier	Military
	CY7C341B–25RMB	R84	84-Lead Windowed Pin Grid Array	
30	CY7C341–30HC/HI	H84	84-Lead Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C341–30JC/JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C341–30RC/RI	R84	84-Lead Windowed Pin Grid Array	
	CY7C341B–30HC/HI	H84	84-Lead Windowed Leaded Chip Carrier	
	CY7C341B–30JC/JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C341B–30RC/RI	R84	84-Lead Windowed Pin Grid Array	
	CY7C341–30HMB	H84	84-Lead Windowed Leaded Chip Carrier	Military
	CY7C341–30RMB	R84	84-Lead Windowed Pin Grid Array	
	CY7C341B–30HMB	H84	84-Lead Windowed Leaded Chip Carrier	
	CY7C341B–30RMB	R84	84-Lead Windowed Pin Grid Array	
35	CY7C341–35HC/HI	H84	84-Lead Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C341–35JC/JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C341–35RC/RI	R84	84-Lead Windowed Pin Grid Array	
	CY7C341B–35HC/HI	H84	84-Lead Windowed Leaded Chip Carrier	
	CY7C341B–35JC/JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C341B–35RC/RI	R84	84-Lead Windowed Pin Grid Array	
	CY7C341–35HMB	H84	84-Lead Windowed Leaded Chip Carrier	Military
	CY7C341–35RMB	R84	84-Lead Windowed Pin Grid Array	
	CY7C341B–35HMB	H84	84-Lead Windowed Leaded Chip Carrier	
	CY7C341B–35RMB	R84	84-Lead Windowed Pin Grid Array	
40	CY7C341–40HMB	H84	84-Lead Windowed Leaded Chip Carrier	Military
	CY7C341–40RMB	R84	84-Lead Windowed Pin Grid Array	

Shaded areas contain preliminary information

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD1}	7, 8, 9, 10, 11
t_{PD2}	7, 8, 9, 10, 11
t_{PD3}	7, 8, 9, 10, 11
t_{CO1}	7, 8, 9, 10, 11
t_{S1}	7, 8, 9, 10, 11
t_{H}	7, 8, 9, 10, 11
t_{ACO1}	7, 8, 9, 10, 11
t_{ACO2}	7, 8, 9, 10, 11
t_{AS1}	7, 8, 9, 10, 11
t_{AH}	7, 8, 9, 10, 11

Document #: 38-00137-F

CY7C342
CY7C342B

128-Macrocell MAX® EPLD

Features

- **128 macrocells in 8 LABs**
- **8 dedicated inputs, 52 bidirectional I/O pins**
- **Programmable interconnect array**
- **0.8-micron double-metal CMOS EPROM technology (CY7C342)**
- **Advanced 0.65-micron CMOS technology to increase performance (CY7C342B)**
- **Available in 68-pin HLCC, PLCC, and PGA**

Functional Description

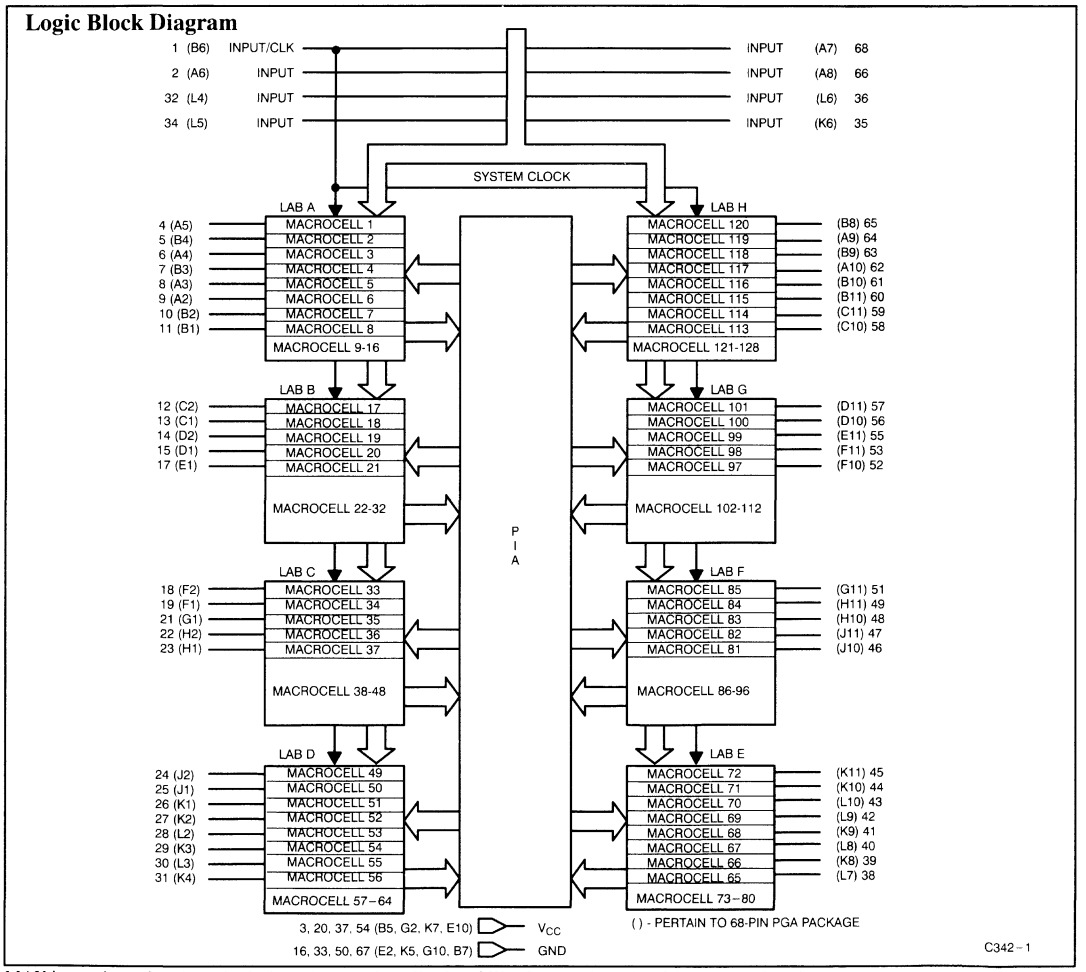
The CY7C342/CY7C342B is an Erasable Programmable Logic Device (EPLD) in which CMOS EPROM cells are used to configure logic functions within the device. The MAX architecture is 100% user configurable, allowing the devices to accommodate a variety of independent logic functions.

The 128 macrocells in the CY7C342/CY7C342B are divided into 8 Logic Array Blocks (LABs), 16 per LAB. There are 256 expander product terms, 32 per LAB, to be used and shared by the macrocells within each LAB.

Each LAB is interconnected with a programmable interconnect array, allowing all signals to be routed throughout the chip.

The speed and density of the CY7C342/CY7C342B allows it to be used in a wide range of applications, from replacement of large amounts of 7400-series TTL logic, to complex controllers and multifunction chips. With greater than 25 times the functionality of 20-pin PLDs, the CY7C342/CY7C342B allows the replacement of over 50 TTL devices. By replacing large amounts of logic, the CY7C342/CY7C342B reduces board space, part count, and increases system reliability.

Logic Block Diagram



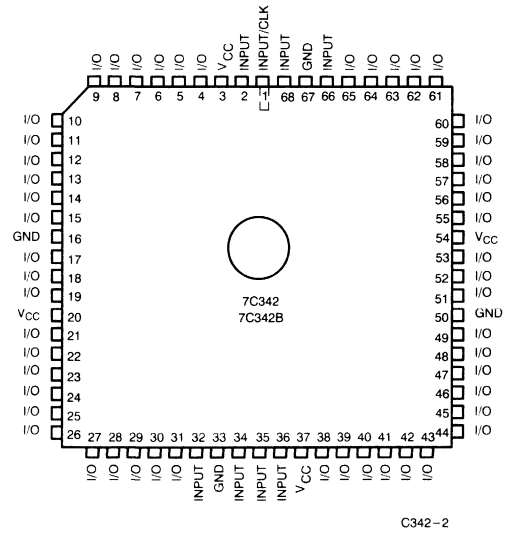
Selection Guide

		7C342B–12	7C342B–15	7C342B–20	7C342–25 7C342B–25	7C342–30 7C342B–30	7C342–35 7C342B–35
Maximum Access Time (ns)		12	15	20	25	30	35
Maximum Operating Current (mA)	Commercial	250	250	250	250	250	250
	Military		320	320	320	320	320
	Industrial		320	320	320	320	320
Maximum Static Current (mA)	Commercial	225	225	225	225	225	225
	Military		275	275	275	275	275
	Industrial		275	275	275	275	275

Shaded area contains preliminary information.

Pin Configurations

PLCC
Top View



C342–2

PGA
Bottom View

	1	2	3	4	5	6	7	8	9	10	11
L		I/O	I/O	INPUT	INPUT	INPUT	I/O	I/O	I/O	I/O	
K	I/O	I/O	I/O	I/O	GND	INPUT	VCC	I/O	I/O	I/O	I/O
J	I/O	I/O								I/O	I/O
H	I/O	I/O								I/O	I/O
G	I/O	VCC								GND	I/O
F	I/O	I/O				7C342 7C342B				I/O	I/O
E	I/O	GND								VCC	I/O
D	I/O	I/O								I/O	I/O
C	I/O	I/O								I/O	I/O
B	I/O	I/O	I/O	I/O	VCC	INPUT/ CLK	GND	I/O	I/O	I/O	I/O
A	■	I/O	I/O	I/O	I/O	INPUT	INPUT	INPUT	I/O	I/O	

C342–3

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... 0°C to +70°C

Maximum Junction Temperature (under bias) ..... 150°C

Supply Voltage to Ground Potential ..... −3.0V to +7.0V

Maximum Power Dissipation ..... 2500 mW

DC V_{CC} or GND Current ..... 500 mA

DC Output Current per Pin ..... −25 mA to +25 mA

DC Input Voltage[1] ..... −3.0V to + 7.0V

DC Program Voltage 13.0V

Static Discharge Voltage ..... > 1100V (per MIL−STD−883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	−40°C to +85°C	5V ± 10%
Military	−55°C to +125°C (Case)	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} +0.3	V
V_{IL}	Input LOW Voltage			−0.3	0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	μA
I_{OZ}	Output Leakage Current	V_O = V_{CC} or GND		−40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[3, 4]		−30	−90	mA
I_{CC1}	Power Supply Current (Static)	V_I = GND (No Load)	Com'l		225	mA
			Mil/Ind		275	
I_{CC2}	Power Supply Current[5]	V_I = V_{CC} or GND (No Load) f = 1.0 MHz[4]	Com'l		250	mA
			Mil/Ind		320	
t_R	Recommended Input Rise Time				100	ns
t_F	Recommended Input Fall Time				100	ns

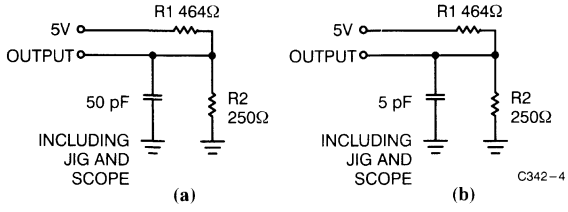
Capacitance[6]

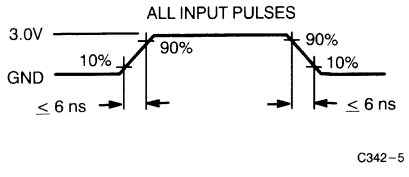
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2V, f = 1.0 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2V, f = 1.0 MHz	10	pF

Notes:

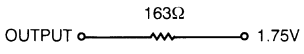
1. Minimum DC input is − 0.3V. During transitions, the inputs may undershoot to − 3.0V for periods less than 20 ns.
2. Typical values are for T_A = 25°C and V_{CC} = 5V.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. Guaranteed but not 100% tested.
5. This parameter is measured with device programmed as a 16-bit counter in each LAB.
6. Part (a) in AC Test Load and Waveforms is used for all parameters except t_{ER} and t_{XZ}, which is used for part (b) in AC Test Load and Waveforms. All external timing parameters are measured referenced to external pins of the device.

AC Test Loads and Waveforms[5]





Equivalent to: THÉVENIN EQUIVALENT (commercial/military)



Logic Array Blocks

There are 8 logic array blocks in the CY7C342/CY7C342B. Each LAB consists of a macrocell array containing 16 macrocells, an expander product term array containing 32 expanders, and an I/O block. The LAB is fed by the programmable interconnect array and the dedicated input bus. All macrocell feedbacks go to the macrocell array, the expander array, and the programmable interconnect array. Expanders feed themselves and the macrocell array. All I/O feedbacks go to the programmable interconnect array so that they may be accessed by macrocells in other LABs as well as the macrocells in the LAB in which they are situated.

Externally, the CY7C342/CY7C342B provides eight dedicated inputs, one of which may be used as a system clock. There are 52 I/O pins that may be individually configured for input, output, or bidirectional data flow.

Programmable Interconnect Array

The Programmable Interconnect Array (PIA) solves interconnect limitations by routing only the signals needed by each logic array block. The inputs to the PIA are the outputs of every macrocell within the device and the I/O pin feedback of every pin on the device.

Unlike masked or programmable gate arrays, which induce variable delay dependent on routing, the PIA has a fixed delay. This eliminates undesired skews among logic signals that may cause glitches in internal or external logic. The fixed delay, regardless of programmable interconnect array configuration, simplifies design by assuring that internal signal skews or races are avoided. The result is ease of design implementation, often in a signal pass, without the multiple internal logic placement and routing iterations required for a programmable gate array to achieve design timing objectives.

Timing Delays

Timing delays within the CY7C342/CY7C342B may be easily determined using *Warp2*™, *Warp3*™, or MAX+PLUS® software or by the model shown in *Figure 1*. The CY7C342/CY7C342B has fixed internal delays, allowing the user to determine the worst case timing delays for any design. For complete timing information the *Warp3* or MAX+PLUS software provides a timing simulator.

Design Recommendations

Operation of the devices described herein with conditions above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this datasheet is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect device reliability. The CY7C342/CY7C342B contains circuitry to protect device pins from high static voltages or electric fields, but normal precautions should be taken to avoid application of any voltage higher than the maximum rated voltages.

For proper operation, input and output pins must be constrained to the range GND $\leq$ (V_{IN} or V_{OUT}) $\leq V_{CC}$. Unused inputs must always be tied to an appropriate logic level (either V_{CC} or GND). Each set of V_{CC} and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 µF must be connected between V_{CC} and GND. For the most effective decoupling, each V_{CC} pin should be separately decoupled to

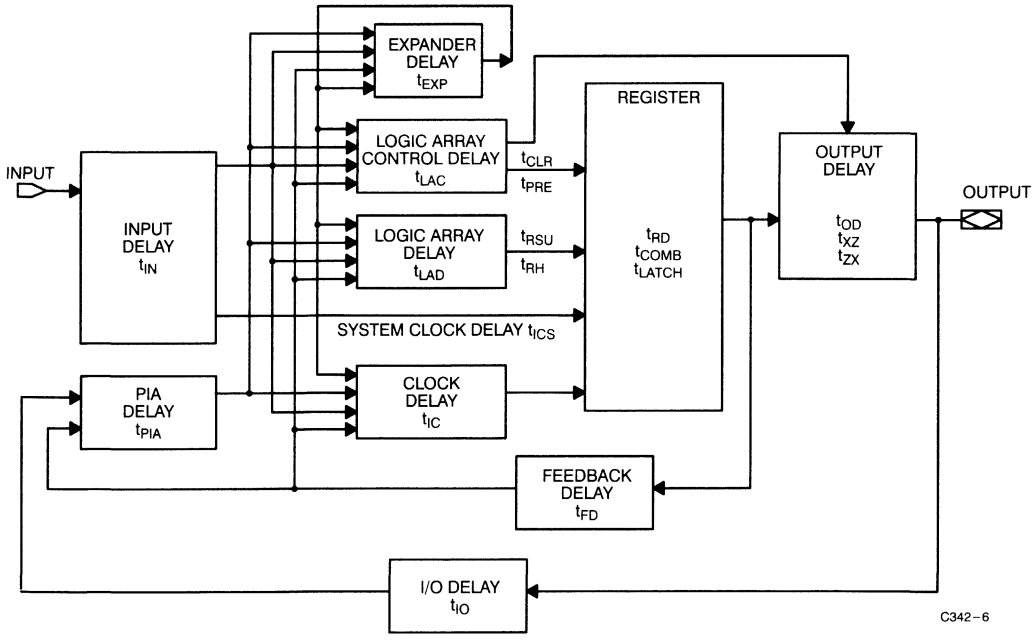


Figure 1. CY7C342/CY7C342B Internal Timing Model

GND directly at the device. Decoupling capacitors should have good frequency response, such as monolithic ceramic types have.

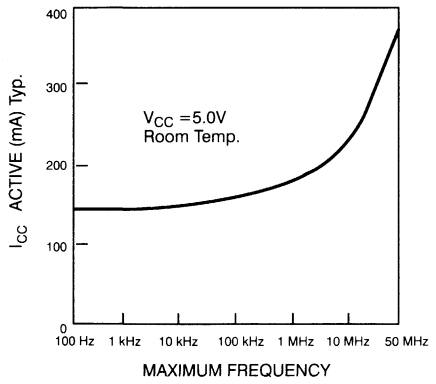
Design Security

The CY7C342/CY7C342B contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the entire device.

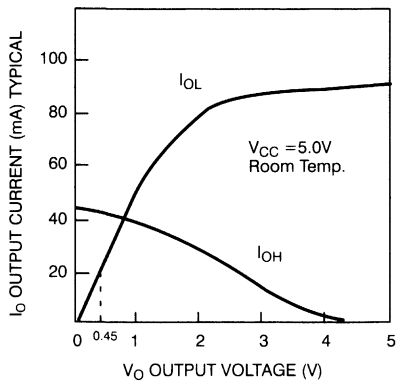
The CY7C342/CY7C342B is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

The erasable nature of these devices allows test programs to be used and erased during early stages of the production flow. The devices also contain on-board logic test circuitry to allow verification of function and AC specification once encapsulated in non-windowed packages.

Typical I_{CC} vs. f_{MAX}



Output Drive Current



Timing Considerations

Unless otherwise stated, propagation delays do not include expanders. When using expanders, add the maximum expander delay t_{EXP} to the overall delay. Similarly, there is an additional t_{PIA} delay for an input from an I/O pin when compared to a signal from straight input pin.

When calculating synchronous frequencies, use t_{S1} if all inputs are on dedicated input pins. The parameter t_{S2} should be used if data is applied at an I/O pin. If t_{S2} is greater than t_{CO1}, $1/t_{S2}$ becomes the limiting frequency in the data path mode unless $1/(t_{WH} + t_{WL})$ is less than $1/t_{S2}$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{S1}. Determine which of $1/(t_{WH} + t_{WL})$, $1/t_{CO1}$, or $1/(t_{EXP} + t_{S1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the synchronous configuration.

When calculating external asynchronous frequencies, use t_{AS1} if all inputs are on the dedicated input pins. If any data is applied to an I/O pin, t_{AS2} must be used as the required set-up time. If $(t_{AS2} + t_{AH})$ is greater than t_{ACO1}, $1/(t_{AS2} + t_{AH})$ becomes the limiting frequency in the data path mode unless $1/(t_{AWH} + t_{AWL})$ is less than $1/(t_{AS2} + t_{AH})$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{AS1}. Determine which of $1/(t_{AWH} + t_{AWL})$, $1/t_{ACO1}$, or $1/(t_{EXP} + t_{AS1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the asynchronous configuration.

The parameter t_{OH} indicates the system compatibility of this device when driving other synchronous logic with positive input hold times, which is controlled by the same synchronous clock. If t_{OH} is greater than the minimum required input hold time of the subsequent synchronous logic, then the devices are guaranteed to function properly with a common synchronous clock under worst-case environmental and supply voltage conditions.

The parameter t_{AOH} indicates the system compatibility of this device when driving subsequent registered logic with a positive hold time and using the same asynchronous clock as the CY7C342/CY7C342B.

In general, if t_{AOH} is greater than the minimum required input hold time of the subsequent logic (synchronous or asynchronous) then the devices are guaranteed to function properly under worst-case environmental and supply voltage conditions, provided the clock signal source is the same. This also applies if expander logic is used in the clock signal path of the driving device, but not for the driven device. This is due to the expander logic in the second device's clock signal path adding an additional delay (t_{EXP}) causing the output data from the preceding device to change prior to the arrival of the clock signal at the following device's register.

Commercial and Industrial External Synchronous Switching Characteristics[6] Over Operating Range

Parameter	Description	7C342B–12		7C342B–15		7C342B–20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[7]		12		15		20	ns
t_{PD2}	I/O Input to Combinatorial Output Delay[8]		20		25		32	ns
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[9]		18		23		30	ns
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[4, 10]		26		33		42	ns
t_{EA}	Input to Output Enable Delay[4, 7]		12		15		20	ns
t_{ER}	Input to Output Disable Delay[4, 7]		12		15		20	ns
t_{CO1}	Synchronous Clock Input to Output Delay		6		7		8	ns
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[4, 11]		14		17		20	ns
t_{S1}	Dedicated Input or Feedback Set-Up Time to Synchronous Clock Input[7, 12]	8		10		13		ns
t_{S2}	I/O Input Set-Up Time to Synchronous Clock Input[7]	16		20		24		ns
t_H	Input Hold Time from Synchronous Clock Input[7]	0		0		0		ns
t_{WH}	Synchronous Clock Input HIGH Time	4.5		5		7		ns
t_{WL}	Synchronous Clock Input LOW Time	4.5		5		7		ns
t_{RW}	Asynchronous Clear Width[4, 7]	12		15		20		ns
t_{RR}	Asynchronous Clear Recovery Time[4, 7]	12		15		20		ns
t_{RO}	Asynchronous Clear to Registered Output Delay[7]		12		15		20	ns
t_{PW}	Asynchronous Preset Width[4, 7]	12		15		20		ns
t_{PR}	Asynchronous Preset Recovery Time[4, 7]	12		15		20		ns
t_{PO}	Asynchronous Preset to Registered Output Delay[7]		12		15		20	ns
t_{CF}	Synchronous Clock to Local Feedback Input[4, 13]		3		3		3	ns
t_P	External Synchronous Clock Period ($1/(f_{MAX3})$)[4]	9		12		15		ns
f_{MAX1}	External Feedback Maximum Frequency ($1/(t_{CO1} + t_{S1})$)[4, 14]	71.4		58.8		47.6		MHz
f_{MAX2}	Internal Local Feedback Maximum Frequency, lesser of ($1/(t_{S1} + t_{CF})$) or ($1/t_{CO1}$)[4, 15]	90.9		76.9		62.5		MHz
f_{MAX3}	Data Path Maximum Frequency, lesser of ($1/(t_{WL} + t_{WH})$), ($1/(t_{S1} + t_H)$) or ($1/t_{CO1}$)[4, 16]	111.1		100		71.4		MHz
f_{MAX4}	Maximum Register Toggle Frequency ($1/(t_{WL}+t_{WH})$)[4, 17]	111.1		100		71.4		MHz
t_{OH}	Output Data Stable Time from Synchronous Clock Input[4, 18]	3		3		3		ns

Shaded area contains preliminary information.

Parameter	Description	7C342–25 7C342B–25		7C342–30 7C342B–30		7C342–35 7C342B–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[7]		25		30		35	ns
t_{PD2}	I/O Input to Combinatorial Output Delay[8]		39		46		55	ns
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[9]		37		44		55	ns
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[4, 10]		51		60		75	ns
t_{EA}	Input to Output Enable Delay[4, 7]		25		30		35	ns
t_{ER}	Input to Output Disable Delay[4, 7]		25		30		35	ns
t_{CO1}	Synchronous Clock Input to Output Delay		14		16		20	ns

Commercial and Industrial External Synchronous Switching Characteristics (continued)

Parameter	Description	7C342–25 7C342B–25		7C342–30 7C342B–30		7C342–35 7C342B–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[4, 11]		30		35		42	ns
t_{S1}	Dedicated Input or Feedback Set-Up Time to Synchronous Clock Input[7, 12]	15		20		25		ns
t_{S2}	I/O Input Set-Up Time to Synchronous Clock Input[7]	29		36		45		ns
t_H	Input Hold Time from Synchronous Clock Input[7]	0		0		0		ns
t_{WH}	Synchronous Clock Input HIGH Time	8		10		12.5		ns
t_{WL}	Synchronous Clock Input LOW Time	8		10		12.5		ns
t_{RW}	Asynchronous Clear Width[4, 7]	25		30		35		ns
t_{RR}	Asynchronous Clear Recovery Time[4, 7]	25		30		35		ns
t_{RO}	Asynchronous Clear to Registered Output Delay[7]		25		30		35	ns
t_{PW}	Asynchronous Preset Width[4, 7]	25		30		35		ns
t_{PR}	Asynchronous Preset Recovery Time[4, 7]	25		30		35		ns
t_{PO}	Asynchronous Preset to Registered Output Delay[7]		25		30		35	ns
t_{CF}	Synchronous Clock to Local Feedback Input[4, 13]		3		3		6	ns
t_P	External Synchronous Clock Period ($1/(f_{MAX3})$)[4]	16		20		25		ns
f_{MAX1}	External Feedback Maximum Frequency ($1/(t_{CO1} + t_{S1})$)[4, 14]	34.5		27.7		22.2		MHz
f_{MAX2}	Internal Local Feedback Maximum Frequency, lesser of ($1/(t_{S1} + t_{CF})$) or ($1/t_{CO1}$)[4, 15]	55.5		43.4		32.2		MHz
f_{MAX3}	Data Path Maximum Frequency, lesser of ($1/(t_{WL} + t_{WH})$), ($1/(t_{S1} + t_H)$) or ($1/t_{CO1}$)[4, 16]	62.5		50		40		MHz
f_{MAX4}	Maximum Register Toggle Frequency ($1/(t_{WL}+t_{WH})$)[4, 17]	62.5		50		40		MHz
t_{OH}	Output Data Stable Time from Synchronous Clock Input[4, 18]	3		3		3		ns

Notes:

7. This specification is a measure of the delay from input signal applied to a dedicated input (68-pin PLCC input pin 1, 2, 32, 34, 35, 66, or 68) to combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function.
   When this note is applied to any parameter specification it indicates that the signal (data, asynchronous clock, asynchronous clear, and/or asynchronous preset) is applied to a dedicated input only and no signal path (either clock or data) employs expander logic.
   If an input signal is applied to an I/O pin an additional delay equal to t_{PIA} should be added to the comparable delay for a dedicated input. If expanders are used, add the maximum expander delay t_{EXP} to the overall delay for the comparable delay without expanders.
8. This specification is a measure of the delay from input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.
9. This specification is a measure of the delay from an input signal applied to a dedicated input (68-pin PLCC input pin 1, 2, 32, 34, 35, 36, 66, or 68) to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic.
10. This specification is a measure of the delay from an input signal applied to an I/O macrocell pin to any output. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
11. This specification is a measure of the delay from synchronous register clock to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used, register is synchronously clocked and all feedback is within the same LAB. This parameter is tested periodically by sampling production material.
12. If data is applied to an I/O input for capture by a macrocell register, the I/O pin input set-up time minimums should be observed. These parameters are t_{S2} for synchronous operation and t_{AS2} for asynchronous operation.
13. This specification is a measure of the delay associated with the internal register feedback path. This is the delay from synchronous clock to LAB logic array input. This delay plus the register set-up time, t_{S1}, is the minimum internal period for an internal synchronous state machine configuration. This delay is for feedback within the same LAB. This parameter is tested periodically by sampling production material.
14. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which a state machine configuration with external feedback can operate. It is assumed that all data inputs and feedback signals are applied to dedicated inputs. All feedback is assumed to be local originating within the same LAB.
15. This specification indicates the guaranteed maximum frequency at which a state machine with internal-only feedback can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{CO1}$.
16. This frequency indicates the maximum frequency at which the device may operate in data path mode (dedicated input pin to output pin). This assumes data input signals are applied to dedicated input pins and no expander logic is used. If any of the data inputs are I/O pins, t_{S2} is the appropriate t_S for calculation.
17. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which an individual output or buried register can be cycled by a clock signal applied to the dedicated clock input pin.
18. This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.

Commercial and Industrial External Asynchronous Switching Characteristics[6] Over Operating Range

Parameter	Description	7C342B–12		7C342B–15		7C342B–20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACO1}	Asynchronous Clock Input to Output Delay[7]		12		15		20	ns
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output[19]		20		25		32	ns
t_{AS1}	Dedicated Input or Feedback Set-Up Time to Asynchronous Clock Input[7]	4		5		5		ns
t_{AS2}	I/O Input Set-Up Time to Asynchronous Clock Input[7]	12		14.5		17		ns
t_{AH}	Input Hold Time from Asynchronous Clock Input[7]	4		5		6		ns
t_{AWH}	Asynchronous Clock Input HIGH Time[7]	8		9		10		ns
t_{AWL}	Asynchronous Clock Input LOW Time[7, 20]	6		7		8		ns
t_{ACF}	Asynchronous Clock to Local Feedback Input[4, 21]		9		11		13	ns
t_{AP}	External Asynchronous Clock Period ($1/(f_{MAXA4})$)[4]	14		16		18		ns
f_{MAXA1}	External Feedback Maximum Frequency in Asynchronous Mode ($1/(t_{ACO1} + t_{AS1})$)[4, 22]	62.5		50		40		MHz
f_{MAXA2}	Maximum Internal Asynchronous Frequency[4, 23]	71.4		62.5		55.5		MHz
f_{MAXA3}	Data Path Maximum Frequency in Asynchronous Mode[4, 24]	83.3		66.6		50		MHz
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[4, 25]	71.4		62.5		55.5		MHz
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[4, 26]	12		12		12		ns

Shaded area contains preliminary information.

Notes:

19. This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used in the logic of combinatorial output or the asynchronous clock input. The clock signal is applied to the dedicated clock input pin and all feedback is within a single LAB. This parameter is tested periodically by sampling production material.
20. This parameter is measured with a positive-edge triggered clock at the register. For negative edge triggering, the t_{AWH} and t_{AWL} parameters must be swapped. If a given input is used to clock multiple registers with both positive and negative polarity, t_{AWH} should be used for both t_{AWH} and t_{AWL}.
21. This specification is a measure of the delay associated with the internal register feedback path for an asynchronous clock to LAB logic array input. This delay plus the asynchronous register set-up time, t_{AS1}, is the minimum internal period for an internal asynchronously clocked state machine configuration. This delay is for feedback within the same LAB, assumes no expander logic in the clock path, and assumes that the clock input signal is applied to a dedicated input pin. This parameter is tested periodically by sampling production material.
22. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that all data inputs, clock inputs, and feedback signals are applied to dedicated inputs and that no expander logic is employed in the clock signal path or data path.
23. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal-only feedback can operate. This parameter is determined by the lesser of $(1/(t_{ACF} + t_{AS1}))$ or $(1/(t_{AWH} + t_{AWL}))$. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO1}$.
    This specification assumes no expander logic is utilized, all data inputs and clock inputs are applied to dedicated inputs, and all state feedback is within a single LAB. This parameter is tested periodically by sampling production material.
24. This frequency is the maximum frequency at which the device may operate in the asynchronously clocked data path mode. This specification is determined by the lesser of $1/(t_{AWH} + t_{AWL})$, $1/(t_{AS1} + t_{AH})$ or $1/t_{ACO1}$. It assumes data and clock input signals are applied to dedicated input pins and no expander logic is used.
25. This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to an external dedicated input pin.
26. This parameter indicates the minimum time that the previous register output data is maintained on the output after an asynchronous register clock input applied to an external dedicated input pin.

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Commercial and Industrial External Asynchronous Switching Characteristics[6] Over Operating Range (continued)

Parameter	Description	7C342–25 7C342B–25		7C342–30 7C342B–30		7C342–35 7C342B–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACO1}	Asynchronous Clock Input to Output Delay[7]		25		30		35	ns
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output[19]		39		46		55	ns
t_{AS1}	Dedicated Input or Feedback Set-Up Time to Asynchronous Clock Input[7]	5		6		8		ns
t_{AS2}	I/O Input Set-Up Time to Asynchronous Clock Input[7]	19		22		28		ns
t_{AH}	Input Hold Time from Asynchronous Clock Input[7]	6		8		10		ns
t_{AWH}	Asynchronous Clock Input HIGH Time[7]	11		14		16		ns
t_{AWL}	Asynchronous Clock Input LOW Time[7, 20]	9		11		14		ns
t_{ACF}	Asynchronous Clock to Local Feedback Input[4, 21]		15		18		22	ns
t_{AP}	External Asynchronous Clock Period ($1/(f_{MAXA4})$)[4]	20		25		30		ns
f_{MAXA1}	External Feedback Maximum Frequency in Asynchronous Mode ($1/(t_{ACO1} + t_{AS1})$)[4, 22]	33.3		27.7		23.2		MHz
f_{MAXA2}	Maximum Internal Asynchronous Frequency[4, 23]	50		40		33.3		MHz
f_{MAXA3}	Data Path Maximum Frequency in Asynchronous Mode[4, 24]	40		33.3		28.5		MHz
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[4, 25]	50		40		33.3		MHz
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[4, 26]	15		15		15		ns

Commercial and Industrial Typical Internal Switching Characteristics Over Operating Range

Parameter	Description	7C342B–12		7C342B–15		7C342B–20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay		2.5		3		4	ns
t_{IO}	I/O Input Pad and Buffer Delay		2.5		3		4	ns
t_{EXP}	Expander Array Delay		6		8		10	ns
t_{LAD}	Logic Array Data Delay		6		8		10	ns
t_{LAC}	Logic Array Control Delay		5		5		7	ns
t_{OD}	Output Buffer and Pad Delay		3		3		3	ns
t_{ZX}	Output Buffer Enable Delay[27]		5		5		5	ns
t_{XZ}	Output Buffer Disable Delay		5		5		5	ns
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	2		4		5		ns
t_{RH}	Register Hold Time Relative to Clock Signal at Register	4		4		5		ns
t_{LATCH}	Flow Through Latch Delay		1		1		2	ns
t_{RD}	Register Delay		0.5		1		1	ns
t_{COMB}	Transparent Mode Delay[28]		1		1		2	ns
t_{CH}	Clock HIGH Time	3		4		6		ns
t_{CL}	Clock LOW Time	3		4		6		ns
t_{IC}	Asynchronous Clock Logic Delay		5		6		8	ns
t_{ICS}	Synchronous Clock Delay		0.5		0.5		0.5	ns
t_{FD}	Feedback Delay		1		1		1	ns
t_{PRE}	Asynchronous Register Preset Time		3		3		3	ns
t_{CLR}	Asynchronous Register Clear Time		3		3		3	ns
t_{PCW}	Asynchronous Preset andClear Pulse Width	2		3		4		ns
t_{PCR}	Asynchronous Preset and Clear Recovery Time	2		3		4		ns
t_{PIA}	Programmable Interconnect Array Delay Time		8		10		12	ns

Shaded area contains preliminary information.

Commercial and Industrial Typical Internal Switching Characteristics Over Operating Range (continued)

Parameter	Description	7C342–25 7C342B–25		7C342–30 7C342B–30		7C342–35 7C342B–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay		5		7		9	ns
t_{IO}	I/O Input Pad and Buffer Delay		6		6		9	ns
t_{EXP}	Expander Array Delay		12		14		20	ns
t_{LAD}	Logic Array Data Delay		12		14		16	ns
t_{LAC}	Logic Array Control Delay		10		12		13	ns
t_{OD}	Output Buffer and Pad Delay		5		5		6	ns
t_{ZX}	Output Buffer Enable Delay[27]		10		11		13	ns
t_{XZ}	Output Buffer Disable Delay		10		11		13	ns
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	6		8		10		ns
t_{RH}	Register Hold Time Relative to Clock Signal at Register	6		8		10		ns
t_{LATCH}	Flow Through Latch Delay		3		4		4	ns
t_{RD}	Register Delay		1		2		2	ns
t_{COMB}	Transparent Mode Delay[28]		3		4		4	ns
t_{CH}	Clock HIGH Time	8		10		12.5		ns
t_{CL}	Clock LOW Time	8		10		12.5		ns
t_{IC}	Asynchronous Clock Logic Delay		14		16		18	ns
t_{ICS}	Synchronous Clock Delay		2		2		3	ns
t_{FD}	Feedback Delay		1		1		2	ns
t_{PRE}	Asynchronous Register Preset Time		5		6		7	ns
t_{CLR}	Asynchronous Register Clear Time		5		6		7	ns
t_{PCW}	Asynchronous Preset and Clear Pulse Width	5		6		7		ns
t_{PCR}	Asynchronous Preset and Clear Recovery Time	5		6		7		ns
t_{PIA}	Programmable Interconnect Array Delay Time		14		16		20	ns

Notes:
27. Sample tested only for an output change of 500 mV.
28. This specification guarantees the maximum combinatorial delay associated with the macrocell register bypass when the macrocell is configured for combinatorial operation.

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Military External Synchronous Switching Characteristics[6] Over Operating Range

Parameter	Description	7C342B–15		7C342B–20		7C342B–25		7C342–30 7C342B–30		7C342–35 7C342B–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[7]		15		20		25		30		35	ns
t_{PD2}	I/O Input to Combinatorial Output Delay[8]		25		32		39		46		55	ns
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[9]		23		30		37		44		55	ns
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[4, 10]		33		42		51		60		75	ns
t_{EA}	Input to Output Enable Delay[4, 7]		15		20		25		30		35	ns
t_{ER}	Input to Output Disable Delay[4, 7]		15		20		25		30		35	ns
t_{CO1}	Synchronous Clock Input to Output Delay		7		8		14		16		20	ns
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[4, 11]		17		20		30		35		42	ns
t_{S1}	Dedicated Input or Feedback Set-Up Time to Synchronous Clock Input[7, 12]	10		13		15		20		25		ns
t_{S2}	I/O Input Set-Up Time to Synchronous Clock Input[7]	20		24		29		36		45		ns
t_H	Input Hold Time from Synchronous Clock Input[7]	0		0		0		0		0		ns
t_{WH}	Synchronous Clock Input HIGH Time	5		7		8		10		12.5		ns
t_{WL}	Synchronous Clock Input LOW Time	5		7		8		10		12.5		ns
t_{RW}	Asynchronous Clear Width[4, 7]	15		20		25		30		35		ns
t_{RR}	Asynchronous Clear Recovery Time[4, 7]	15		20		25		30		35		ns
t_{RO}	Asynchronous Clear to Registered Output Delay[7]		15		20		25		30		35	ns
t_{PW}	Asynchronous Preset Width[4, 7]	15		20		25		30		35		ns
t_{PR}	Asynchronous Preset Recovery Time[4, 7]	15		20		25		30		35		ns
t_{PO}	Asynchronous Preset to Registered Output Delay[7]		15		20		25		30		35	ns
t_{CF}	Synchronous Clock to Local Feedback Input[4, 13]		3		3		3		3		6	ns
t_P	External Synchronous Clock Period ($1/(f_{MAX3})$)[4]	12		14		16		20		25		ns

Military External Synchronous Switching Characteristics[6] Over Operating Range (continued)

Parameter	Description	7C342B–15		7C342B–20		7C342B–25		7C342–30 7C342B–30		7C342–35 7C342B–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX1}	External Feedback Maximum Frequency $(1/(t_{CO1} + t_{S1}))$[4, 14]	58.8		47.6		34.5		27.7		22.2		MHz
f_{MAX2}	Internal Local Feedback Maximum Frequency, lesser of $(1/(t_{S1} + t_{CF}))$ or $(1/t_{CO1})$[4, 15]	76.9		62.5		55.5		43.4		32.2		MHz
f_{MAX3}	Data Path Maximum Frequency, lesser of $(1/(t_{WL} + t_{WH}))$, $(1/(t_{S1} + t_H))$ or $(1/t_{CO1})$[4, 16]	100		71.4		62.5		50		40		MHz
f_{MAX4}	Maximum Register Toggle Frequency $(1/(t_{WL} + t_{WH}))$[4, 17]	100		71.4		62.5		50		40		MHz
t_{OH}	Output Data Stable Time from Synchronous Clock Input[4, 18]	3		3		3		3		3		ns

Shaded area contains preliminary information.

Military External Asynchronous Switching Characteristics[6] Over Operating Range

Parameter	Description	7C342B–15		7C342B–20		7C342B–25		7C342–30 7C342B–30		7C342–35 7C342B–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACO1}	Asynchronous Clock Input to Output Delay[7]		15		20		25		30		35	ns
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output[19]		25		32		39		46		55	ns
t_{AS1}	Dedicated Input or Feedback Set-Up Time to Asynchronous Clock Input[7]	5		6		5		6		8		ns
t_{AS2}	I/O Input Set-Up Time to Asynchronous Clock Input[7]	14.5		17		19		22		28		ns
t_{AH}	Input Hold Time from Asynchronous Clock Input[7]	5		6		6		8		10		ns
t_{AWH}	Asynchronous Clock Input HIGH Time[7]	9		10		11		14		16		ns
t_{AWL}	Asynchronous Clock Input LOW Time[7, 20]	7		8		9		11		14		ns
t_{ACF}	Asynchronous Clock to Local Feedback Input[4, 21]		11		13		15		18		22	ns
t_{AP}	External Asynchronous Clock Period $(1/(f_{MAXA4}))$[4]	16		18		20		25		30		ns
f_{MAXA1}	External Feedback Maximum Frequency in Asynchronous Mode $(1/(t_{ACO1} + t_{AS1}))$[4, 22]	50.0		40		33.3		27.7		23.2		MHz
f_{MAXA2}	Maximum Internal Asynchronous Frequency[4, 23]	62.5		55.5		50		40		33.3		MHz
f_{MAXA3}	Data Path Maximum Frequency in Asynchronous Mode[4, 24]	66.6		50		40		33.3		28.5		MHz
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[4, 25]	62.5		55.5		50		40		33.3		MHz
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[4, 26]	12		12		15		15		15		ns

Shaded area contains preliminary information.

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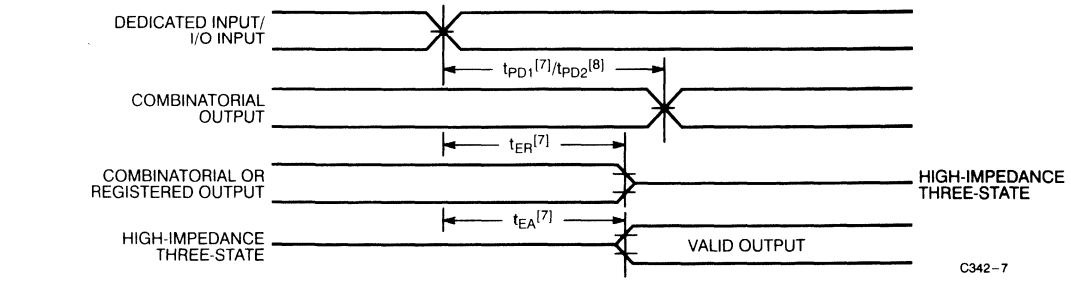
Military Typical Internal Switching Characteristics Over Operating Range

Parameter	Description	7C342B–15		7C342B–20		7C342B–25		7C342–30		7C342–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay		3		4		5		7		9	ns
t_{IO}	I/O Input Pad and Buffer Delay		3		4		6		6		9	ns
t_{EXP}	Expander Array Delay		8		10		12		14		20	ns
t_{LAD}	Logic Array Data Delay		8		10		12		14		16	ns
t_{LAC}	Logic Array Control Delay		5		7		10		12		13	ns
t_{OD}	Output Buffer and Pad Delay		3		3		5		5		6	ns
t_{ZX}	Output Buffer Enable Delay[27]		5		5		10		11		13	ns
t_{XZ}	Output Buffer Disable Delay		5		5		10		11		13	ns
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	4		5		6		8		10		ns
t_{RH}	Register Hold Time Relative to Clock Signal at Register	4		5		6		8		10		ns
t_{LATCH}	Flow Through Latch Delay		1		2		3		4		4	ns
t_{RD}	Register Delay		1		1		1		2		2	ns
t_{COMB}	Transparent Mode Delay[28]		1		2		3		4		4	ns
t_{CH}	Clock HIGH Time	4		6		8		10		12.5		ns
t_{CL}	Clock LOW Time	4		6		8		10		12.5		ns
t_{IC}	Asynchronous Clock Logic Delay		6		8		14		16		18	ns
t_{ICS}	Synchronous Clock Delay		0.5		0.5		2		2		3	ns
t_{FD}	Feedback Delay		1		1		1		1		2	ns
t_{PRE}	Asynchronous Register Preset Time		3		3		5		6		7	ns
t_{CLR}	Asynchronous Register Clear Time		3		3		5		6		7	ns
t_{PCW}	Asynchronous Preset and Clear Pulse Width	3		4		5		6		7		ns
t_{PCR}	Asynchronous Preset and Clear Recovery Time	3		4		5		6		7		ns
t_{PIA}	Programmable Interconnect Array Delay Time		10		12		14		16		20	ns

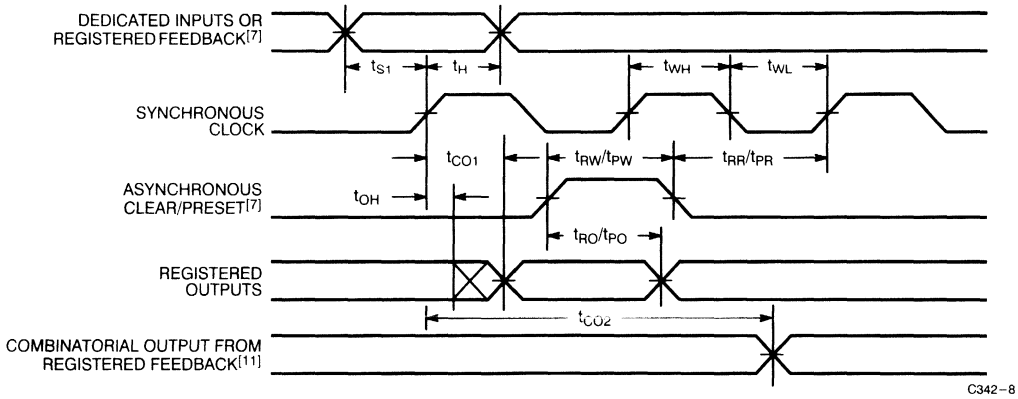
Shaded area contains preliminary information.

Switching Waveforms

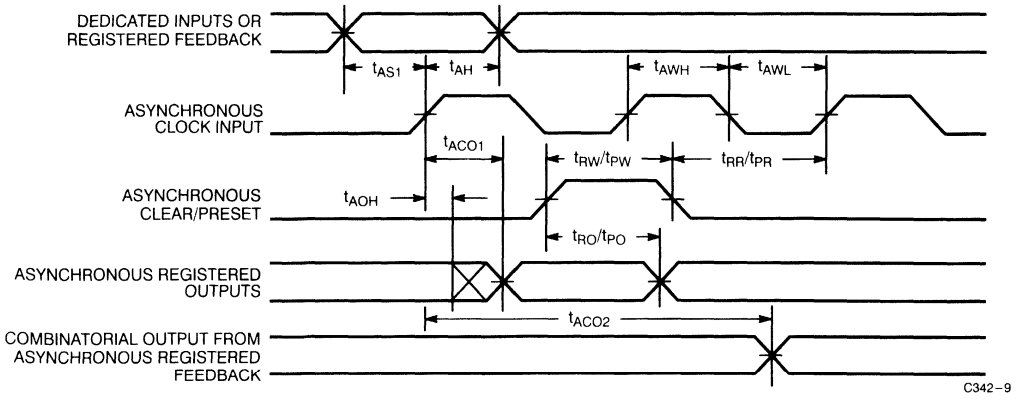
External Combinatorial



External Synchronous

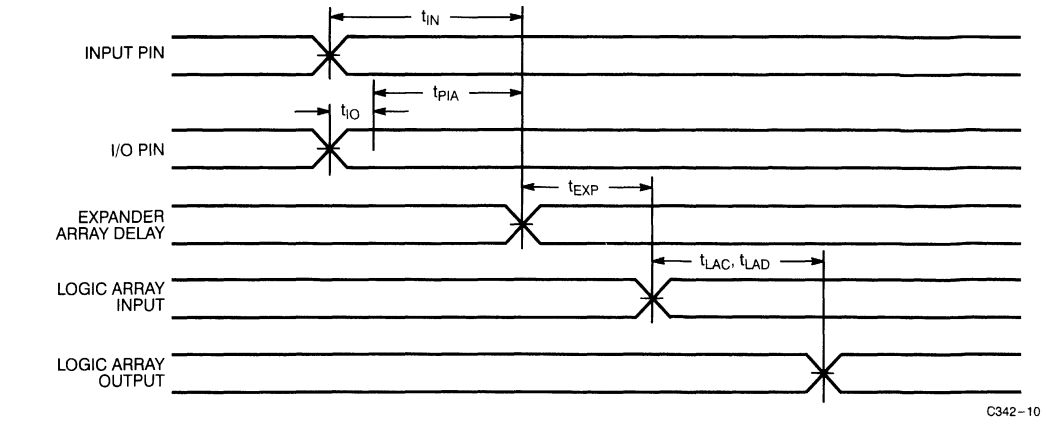


External Asynchronous

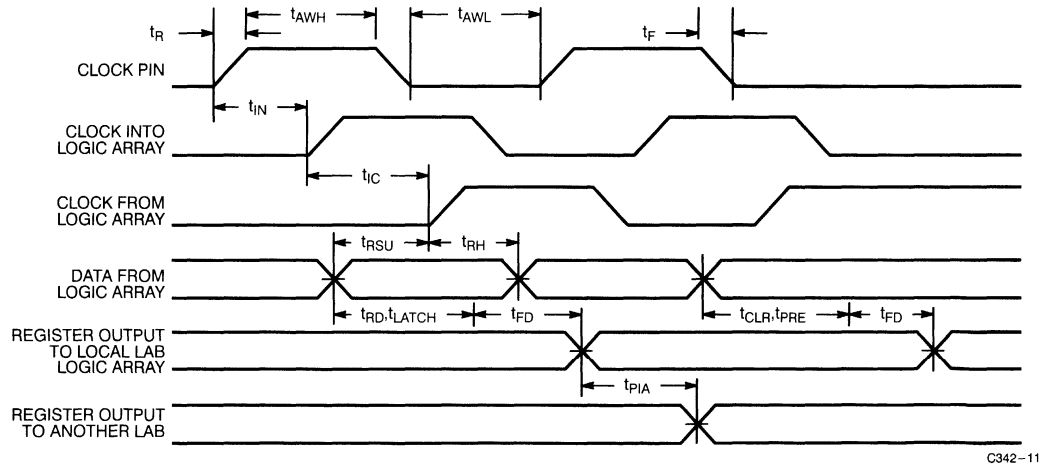


Switching Waveforms (continued)

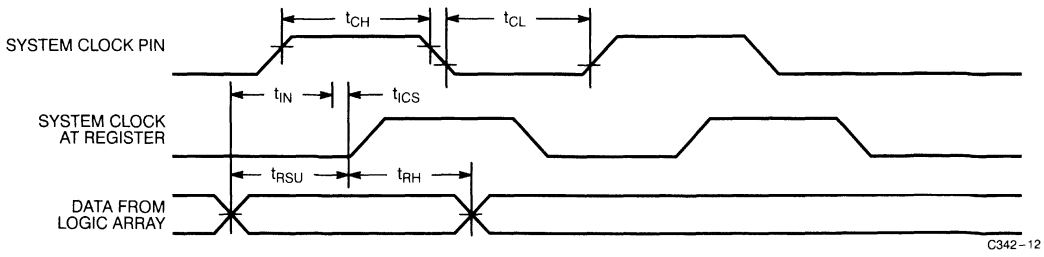
Internal Combinatorial



Internal Asynchronous

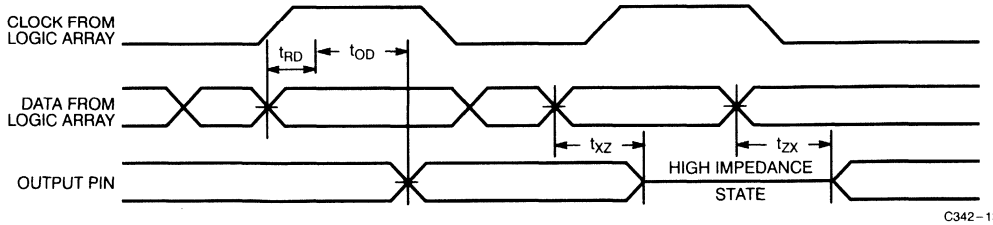


Internal Synchronous



Switching Waveforms (continued)

Internal Synchronous



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C342B–12HC	H81	68-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C342B–12JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C342B–12RC	R68	68-Pin Windowed Ceramic Pin Grid Array	
15	CY7C342B–15HC/HI	H81	68-Pin Windowed Leaded Chip Carrier	Commercial/ Industrial
	CY7C342B–15JC/JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C342B–15RC/RI	R68	68-Pin Windowed Ceramic Pin Grid Array	
	CY7C342B–15HMB	H81	68-Pin Windowed Leaded Chip Carrier	Military
	CY7C342B–15RMB	R68	68-Pin Windowed Ceramic Pin Grid Array	
20	CY7C342B–20HC/HI	H81	68-Pin Windowed Leaded Chip Carrier	Commercial/ Industrial
	CY7C342B–20JC/JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C342B–20RC/RI	R68	68-Pin Windowed Ceramic Pin Grid Array	
	CY7C342B–20HMB	H81	68-Pin Windowed Leaded Chip Carrier	Military
	CY7C342B–20RMB	R68	68-Pin Windowed Ceramic Pin Grid Array	
25	CY7C342–25HC/HI	H81	68-Pin Windowed Leaded Chip Carrier	Commercial/ Industrial
	CY7C342–25JC/JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C342–25RC/RI	R68	68-Pin Windowed Ceramic Pin Grid Array	
	CY7C342B–25HC/HI	H81	68-Pin Windowed Leaded Chip Carrier	
	CY7C342B–25JC/JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C342B–25RC/RI	R68	68-Pin Windowed Ceramic Pin Grid Array	
	CY7C342B–25HMB	H81	68-Pin Windowed Leaded Chip Carrier	Military
	CY7C342B–25RMB	R68	68-Pin Windowed Ceramic Pin Grid Array	
30	CY7C342–30HC/HI	H81	68-Pin Windowed Leaded Chip Carrier	Commercial/ Industrial
	CY7C342–30JC/JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C342–30RC/RI	R68	68-Pin Windowed Ceramic Pin Grid Array	
	CY7C342B–30HC/HI	H81	68-Pin Windowed Leaded Chip Carrier	
	CY7C342B–30JC/JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C342B–30RC/RI	R68	68-Pin Windowed Ceramic Pin Grid Array	
	CY7C342–30HMB	H81	68-Pin Windowed Leaded Chip Carrier	Military
	CY7C342–30RMB	R68	68-Pin Windowed Ceramic Pin Grid Array	
	CY7C342B–30HMB	H81	68-Pin Windowed Leaded Chip Carrier	
	CY7C342B–30RMB	R68	68-Pin Windowed Ceramic Pin Grid Array	
35	CY7C342–35HC/HI	H81	68-Pin Windowed Leaded Chip Carrier	Commercial/ Industrial
	CY7C342–35JC/JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C342–35RC/RI	R68	68-Pin Windowed Ceramic Pin Grid Array	
	CY7C342B–35HC/HI	H81	68-Pin Windowed Leaded Chip Carrier	
	CY7C342B–35JC/JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C342B–35RC/RI	R68	68-Pin Windowed Ceramic Pin Grid Array	
	CY7C342–35HMB	H81	68-Pin Windowed Leaded Chip Carrier	Military
	CY7C342–35RMB	R68	68-Pin Windowed Ceramic Pin Grid Array	
	CY7C342B–35HMB	H81	68-Pin Windowed Leaded Chip Carrier	
	CY7C342B–35RMB	R68	68-Pin Windowed Ceramic Pin Grid Array	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD1}	7, 8, 9, 10, 11
t_{PD2}	7, 8, 9, 10, 11
t_{PD3}	7, 8, 9, 10, 11
t_{CO1}	7, 8, 9, 10, 11
t_{S1}	7, 8, 9, 10, 11
t_{S2}	7, 8, 9, 10, 11
t_{H}	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{WL}	7, 8, 9, 10, 11
t_{RO}	7, 8, 9, 10, 11
t_{PO}	7, 8, 9, 10, 11
t_{ACO1}	7, 8, 9, 10, 11
t_{AS1}	7, 8, 9, 10, 11
t_{AH}	7, 8, 9, 10, 11
t_{AWH}	7, 8, 9, 10, 11
t_{AWL}	7, 8, 9, 10, 11

Document #: 38-00119-F

CY7C343
CY7C343B

64-Macrocell MAX® EPLD

Features

- **64 MAX macrocells in 4 LABs**
- **8 dedicated inputs, 24 bidirectional I/O pins**
- **Programmable interconnect array**
- **0.8-micron double-metal CMOS EPROM technology (CY7C343)**
- **Advanced 0.65-micron CMOS technology to increase performance (CY7C343B)**
- **Available in 44-pin HLCC, PLCC**
- **Lowest power MAX device**

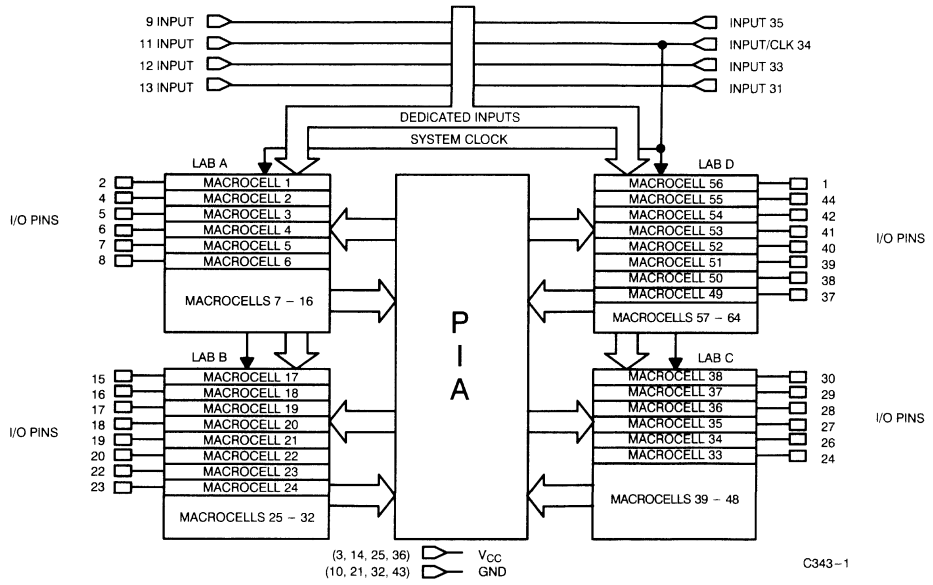
Functional Description

The CY7C343/CY7C343B is a high-performance, high-density erasable programmable logic device, available in 44-pin PLCC and HLCC packages.

The CY7C343/CY7C343B contains 64 highly flexible macrocells and 128 expander product terms. These resources are divided into four Logic Array Blocks (LABs) connected through the Programmable Interconnect Array (PIA). There are 8 input pins, one that doubles as a clock pin when needed. The CY7C343/CY7C343B also has 28 I/O pins, each connected to a macrocell (6 for LABs A and C, and 8 for LABs B and D). The remaining 36 macrocells are used for embedded logic.

The CY7C343/CY7C343B is excellent for a wide range of both synchronous and asynchronous applications.

Logic Block Diagram



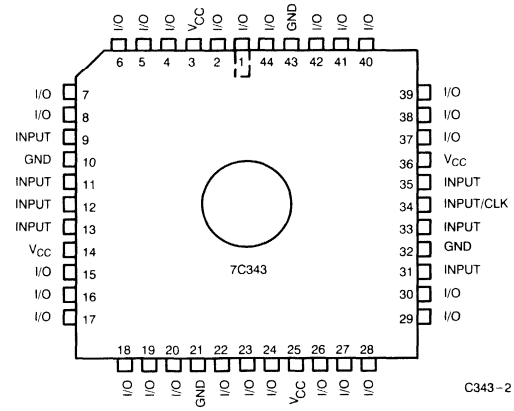
Selection Guide

		7C343B–12	7C343B–15	7C343–20 7C343B–20	7C343–25 7C343B–25	7C343–30 7C343B–30	7C343–35 7C343B–35
Maximum Access Time (ns)		12	15	20	25	30	35
Maximum Operating Current (mA)	Commercial	135	135	135	135	135	135
	Military		225	225	225	225	225
	Industrial	225	225	225	225	225	225
Maximum Standby Current (mA)	Commercial	125	125	125	125	125	125
	Military		200	200	200	200	200
	Industrial	200	200	200	200	200	200

Shaded area contains advanced information.

Pin Configuration

HLCC
Top View



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... 0°C to +70°C

Maximum Junction Temperature (Under Bias) ..... 150°C

Supply Voltage to Ground Potential ..... −2.0V to +7.0V

Maximum Power Dissipation ..... 2500 mW

DC V_{CC} or GND Current ..... 500 mA

DC Output Current, per Pin ..... −25 mA to +25 mA

DC Input Voltage[1] ..... −3.0V to +7.0V

DC Program Voltage 13.0V

Static Discharge Voltage ..... >1100V (per MIL-STD-883, method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±5%
Industrial	−40°C to +85°C	5V ±10%
Military	−55°C to +125°C (Case)	5V ±10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA			0.45	V
V_{IH}	Input HIGH Level			2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Level			− 0.3	0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		− 10	+10	μA
I_{OZ}	Output Leakage Current	V_O = V_{CC} or GND		− 40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[3, 4]		− 30	− 90	mA
I_{CC1}	Power Supply Current (Standby)	V_I = V_{CC} or GND (No Load)	Commercial		125	mA
			Military/Industrial		200	mA
I_{CC2}	Power Supply Current[5]	V_I = V_{CC} or GND (No Load) f = 1.0 MHz[4, 5]	Commercial		135	mA
			Military/Industrial		225	mA
t_R	Recommended Input Rise Time				100	ns
t_F	Recommended Input Fall Time				100	ns

Notes:

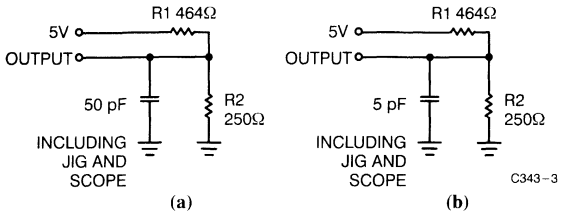
1. Minimum DC input is −0.3V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns.
2. Typical values are for T_A = 25°C and V_{CC} = 5V.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. Guaranteed but not 100% tested.
5. Measured with device programmed as a 16-bit counter in each LAB. This parameter is tested periodically by sampling production material.

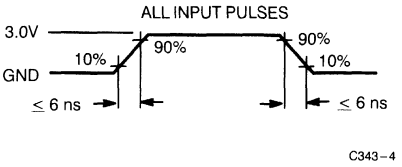
Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2V, f = 1.0 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, f = 1.0 MHz	10	pF

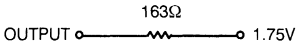
Notes:
6. Part (a) in AC Test Load and Waveforms is used for all parameters except t_{ER} and t_{XZ}, which is used for part (b) in AC Test Load and Waveforms. All external timing parameters are measured referenced to external pins of the device.

AC Test Loads and Waveforms[6]





Equivalent to: THÉVENIN EQUIVALENT (commercial/military)



Programmable Interconnect Array

The Programmable Interconnect Array (PIA) solves interconnect limitations by routing only the signals needed by each logic array block. The inputs to the PIA are the outputs of every macrocell within the device and the I/O pin feedback of every pin on the device.

Unlike masked or programmable gate arrays, which induce variable delay dependent on routing, the PIA has a fixed delay. This eliminates undesired skews among logic signals, which may cause glitches in internal or external logic. The fixed delay, regardless of programmable interconnect array configuration, simplifies design by ensuring that internal signal skews or races are avoided. The result is simpler design implementation, often in a single pass, without the multiple internal logic placement and routing iterations required for a programmable gate array to achieve design timing objectives.

Timing Delays

Timing delays within the CY7C343/CY7C343B may be easily determined using *Warp2™*, *Warp3™*, or MAX+PLUS® software or by the model shown in *Figure 1*. The CY7C343/CY7C343B has fixed internal delays, allowing the user to determine the worst case timing delays for any design. For complete timing information, the *Warp3* or MAX+PLUS software provides a timing simulator.

Design Recommendations

Operation of the devices described herein with conditions above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect device reliability.The CY7C343/CY7C343B contains circuitry to protect device pins from high static voltages or electric fields; however, normal precautions should be taken to avoid applying any voltage higher than maximum rated voltages.

For proper operation, input and output pins must be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic level (either V_{CC} or GND). Each set of V_{CC} and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 μF must be connected between V_{CC} and GND. For the most effective decoupling, each V_{CC} pin should be separately decoupled to GND, directly at the device. Decoupling capacitors should have good frequency response, such as monolithic ceramic types.

Timing Considerations

Unless otherwise stated, propagation delays do not include expanders. When using expanders, add the maximum expander delay t_{EXP} to the overall delay. Similarly, there is an additional t_{PIA} delay for an input from an I/O pin when compared to a signal from a straight input pin.

When calculating synchronous frequencies, use t_{S1} if all inputs are on the input pins. t_{S2} should be used if data is applied at an I/O pin. If t_{S2} is greater than t_{CO1}, $1/t_{S2}$ becomes the limiting frequency in the data path mode unless $1/(t_{WH} + t_{WL})$ is less than $1/t_{S2}$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{S1}. Determine which of $1/(t_{WH} + t_{WL})$, $1/t_{CO1}$, or $1/(t_{EXP} + t_{S1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the synchronous configuration.

When calculating external asynchronous frequencies, use t_{AS1} if all inputs are on dedicated input pins. If any data is applied to an I/O pin, t_{AS2} must be used as the required set-up time. If ($t_{AS2} + t_{AH}$)

is greater than t_{ACO1}, $1/(t_{AS2} + t_{AH})$ becomes the limiting frequency in the data path mode unless $1/(t_{AWH} + t_{AH})$ is less than $1/(t_{AS2} + t_{AH})$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{AS1}. Determine which of $1/(t_{AWH} + t_{AWL})$, $1/t_{ACO1}$, or $1/(t_{EXP} + t_{AS1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the asynchronous configuration.

The parameter t_{OH} indicates the system compatibility of this device when driving other synchronous logic with positive input hold times, which is controlled by the same synchronous clock. If t_{OH} is greater than the minimum required input hold time of the subsequent synchronous logic, then the devices are guaranteed to function properly with a common synchronous clock under worst-case environmental and supply voltage conditions.

The parameter t_{AOH} indicates the system compatibility of this device when driving subsequent registered logic with a positive hold time and using the same clock as the CY7C343/CY7C343B.

In general, if t_{AOH} is greater than the minimum required input hold time of the subsequent logic (synchronous or asynchronous), then the devices are guaranteed to function properly under worst-case environmental and supply voltage conditions, provided the clock signal source is the same. This also applies if expander logic is used in the clock signal path of the driving device, but not for the driven device. This is due to the expander logic in the second device's clock signal path adding an additional delay (t_{EXP}), causing the output data from the preceding device to change prior to the arrival of the clock signal at the following device's register.

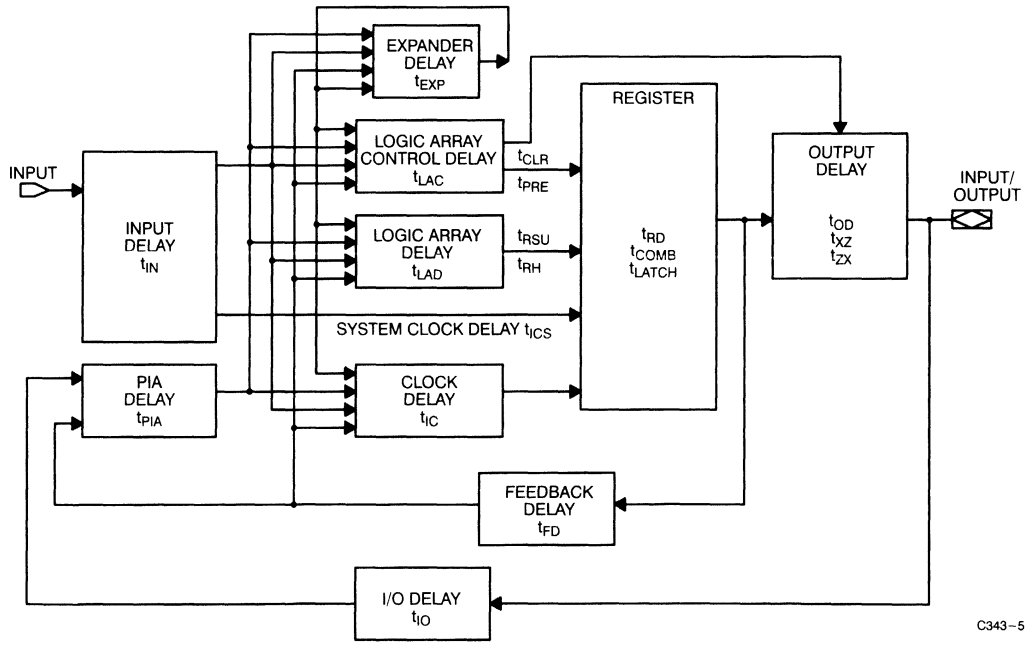


Figure 1. CY7C343/CY7C343B Internal Timing Model

External Synchronous Switching Characteristics[6] Over Operating Range

Parameter	Description		7C343B–12		7C343B–15		7C343–20 7C343B–20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[7]	Com'l/Ind		12		15		20	ns
		Mil				15		20	
t_{PD2}	I/O Input to Combinatorial Output Delay[8]	Com'l/Ind		20		25		32	ns
		Mil				25		32	
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[9]	Com'l/Ind		18		23		30	ns
		Mil				23		30	
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[4, 10]	Com'l/Ind		26		33		42	ns
		Mil				33		42	
t_{EA}	Input to Output Enable Delay[4, 7]	Com'l/Ind		12		15		20	ns
		Mil				15		20	
t_{ER}	Input to Output Disable Delay[4, 7]	Com'l/Ind		12		15		20	ns
		Mil				15		20	
t_{CO1}	Synchronous Clock Input to Output Delay	Com'l/Ind		6		7		12	ns
		Mil				7		12	
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[4, 11]	Com'l/Ind		14		17		25	ns
		Mil				17		25	
t_{S1}	Dedicated Input or Feedback Set-Up Time to Synchronous Clock Input[7]	Com'l/Ind	8		10		12		ns
		Mil			10		12		
t_{S2}	I/O Input Set-Up Time to Synchronous Clock Input[7, 12]	Com'l/Ind	16		20		24		ns
		Mil			20		24		
t_H	Input Hold Time from Synchronous Clock Input[7]	Com'l/Ind	0		0		0		ns
		Mil			0		0		
t_{WH}	Synchronous Clock Input HIGH Time	Com'l/Ind	4.5		5		6		ns
		Mil			5		6		
t_{WL}	Synchronous Clock Input LOW Time	Com'l/Ind	4.5		5		6		ns
		Mil			5		6		
t_{RW}	Asynchronous Clear Width[4, 7]	Com'l/Ind	12		15		20		ns
		Mil			15		20		
t_{RR}	Asynchronous Clear Recovery Time[4, 7]	Com'l/Ind	12		15		20		ns
		Mil			15		20		
t_{RO}	Asynchronous Clear to Registered Output Delay[7]	Com'l/Ind		12		15		20	ns
		Mil				15		20	
t_{PR}	Asynchronous Preset Recovery Time[4, 7]	Com'l/Ind	12		15		20		ns
		Mil			15		20		
t_{PO}	Asynchronous Preset to Registered Output Delay[7]	Com'l/Ind		12		15		20	ns
		Mil				15		20	
t_{CF}	Synchronous Clock to Local Feedback Input[4, 13]	Com'l/Ind		3		3		3	ns
		Mil				3		3	
t_P	External Synchronous Clock Period ($1/f_{MAX3}$)[4]	Com'l/Ind	9		10		12		ns
		Mil			10		12		
f_{MAX1}	External Maximum Frequency ($1/(t_{CO1} + t_{S1})$)[4, 14]	Com'l/Ind	71.4		58.8		41.6		MHz
		Mil			58.8		41.6		

Shaded areas contain advanced information.

External Synchronous Switching Characteristics[6] Over Operating Range (continued)

Parameter	Description		7C343B–12		7C343B–15		7C343–20 7C343B–20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX2}	Internal Local Feedback Maximum Frequency, lesser of $(1/(t_{S1} + t_{CF}))$ or $(1/t_{CO1})$[4, 15]	Com'l/Ind	90.9		76.9		66.6		MHz
		Mil			76.9		66.6		
f_{MAX3}	Data Path Maximum Frequency, least of $1/(t_{WL} + t_{WH})$, $1/(t_{S1} + t_H)$, or $(1/t_{CO1})$[4, 16]	Com'l/Ind	111.1		100		83.3		MHz
		Mil			100		83.3		
f_{MAX4}	Maximum Register Toggle Frequency $(1/(t_{WL} + t_{WH}))$[4, 17]	Com'l/Ind	111.1		100		83.3		MHz
		Mil			100		83.3		
t_{OH}	Output Data Stable Time from Synchronous Clock Input[4, 18]	Com'l/Ind	3		3		3		ns
		Mil			3		3		
t_{PW}	Asynchronous Preset Width[4, 7]	Com'l/Ind	12		15		20		ns
		Mil			15		20		

Shaded areas contain advanced information.

Notes:

7. This specification is a measure of the delay from input signal applied to a dedicated input (44-pin PLCC input pin 9, 11, 12, 13, 31, 33, 34, or 35) to combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function.
   When this note is applied to any parameter specification it indicates that the signal (data, asynchronous clock, asynchronous clear, and/or asynchronous preset) is applied to a dedicated input only and no signal path (either clock or data) employs expander logic.
   If an input signal is applied to an I/O pin, an additional delay equal to t_{PIA} should be added to the comparable delay for a dedicated input.
   If expanders are used, add the maximum expander delay t_{EXP} to the overall delay for the comparable delay without expanders.
8. This specification is a measure of the delay from input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.
9. This specification is a measure of the delay from an input signal applied to a dedicated input (44-pin PLCC input pin 9, 11, 12, 13, 31, 33, 34, or 35) to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
10. This specification is a measure of the delay from an input signal applied to an I/O macrocell pin to any output. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
11. This specification is a measure of the delay from synchronous register clock to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used, register is synchronously clocked and all feedback is within the same LAB. This parameter is tested periodically by sampling production material.
12. If data is applied to an I/O input for capture by a macrocell register, the I/O pin set-up time minimums should be observed. These parameters are t_{S2} for synchronous operation and t_{AS2} for asynchronous operation.
13. This specification is a measure of the delay associated with the internal register feedback path. This is the delay from synchronous clock to LAB logic array input. This delay plus the register set-up time, t_{S1}, is the minimum internal period for an internal synchronous state machine configuration. This delay is for feedback within the same LAB. This parameter is tested periodically by sampling production material.
14. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which a state machine configuration with external feedback can operate. It is assumed that all data inputs and feedback signals are applied to dedicated inputs.
15. This specification indicates the guaranteed maximum frequency at which a state machine, with internal-only feedback, can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{CO1}$. All feedback is assumed to be local, originating within the same LAB.
16. This frequency indicates the maximum frequency at which the device may operate in data path mode. This delay assumes data input signals are applied to dedicated inputs and no expander logic is used.
17. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which an individual output or buried register can be cycled.
18. This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.

3

External Synchronous Switching Characteristics[6] Over Operating Range (continued)

Parameter	Description		7C343–25 7C343B–25		7C343–30 7C343B–30		7C343–35 7C343B–35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[7]	Com'l/Ind		25		30		35	ns
		Mil		25		30		35	
t_{PD2}	I/O Input to Combinatorial Output Delay[8]	Com'l/Ind		39		44		53	ns
		Mil		39		44		53	
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[9]	Com'l/Ind		37		44		55	ns
		Mil		37		44		55	
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[4, 10]	Com'l/Ind		51		58		73	ns
		Mil		51		58		73	
t_{EA}	Input to Output Enable Delay[4, 7]	Com'l/Ind		25		30		35	ns
		Mil		25		30		35	
t_{ER}	Input to Output Disable Delay[4, 7]	Com'l/Ind		25		30		35	ns
		Mil		25		30		35	
t_{CO1}	Synchronous Clock Input to Output Delay	Com'l/Ind		14		16		20	ns
		Mil		14		16		20	
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[4, 11]	Com'l/Ind		30		35		42	ns
		Mil		30		35		42	
t_{S1}	Dedicated Input or Feedback Set-Up Time to Synchronous Clock Input[7]	Com'l/Ind	15		20		25		ns
		Mil	15		20		25		
t_{S2}	I/O Input Set-Up Time to Synchronous Clock Input[7, 12]	Com'l/Ind	30		35		42		ns
		Mil	30		35		42		
t_H	Input Hold Time from Synchronous Clock Input[7]	Com'l/Ind	0		0		0		ns
		Mil	0		0		0		
t_{WH}	Synchronous Clock Input HIGH Time	Com'l/Ind	8		10		12.5		ns
		Mil	8		10		12.5		
t_{WL}	Synchronous Clock Input LOW Time	Com'l/Ind	8		10		12.5		ns
		Mil	8		10		12.5		
t_{RW}	Asynchronous Clear Width[4, 7]	Com'l/Ind	25		30		35		ns
		Mil	25		30		35		
t_{RR}	Asynchronous Clear Recovery Time[4, 7]	Com'l/Ind	25		30		35		ns
		Mil	25		30		35		
t_{RO}	Asynchronous Clear to Registered Output Delay[7]	Com'l/Ind		25		30		35	ns
		Mil		25		30		35	
t_{PR}	Asynchronous Preset Recovery Time[4, 7]	Com'l/Ind	25		30		35		ns
		Mil	25		30		35		
t_{PO}	Asynchronous Preset to Registered Output Delay[7]	Com'l/Ind		25		30		35	ns
		Mil		25		30		35	
t_{CF}	Synchronous Clock to Local Feedback Input[4, 13]	Com'l/Ind		3		3		5	ns
		Mil		3		3		5	
t_P	External Synchronous Clock Period ($1/f_{MAX3}$)[4]	Com'l/Ind	16		20		25		ns
		Mil	16		20		25		
f_{MAX1}	External Maximum Frequency ($1/(t_{CO1} + t_{S1})$)[4, 14]	Com'l/Ind	34		27		22.2		MHz
		Mil	34		27		22.2		

External Synchronous Switching Characteristics[6] Over Operating Range (continued)

Parameter	Description		7C343–25 7C343B–25 Min.	7C343–25 7C343B–25 Max.	7C343–30 7C343B–30 Min.	7C343–30 7C343B–30 Max.	7C343–35 7C343B–35 Min.	7C343–35 7C343B–35 Max.	Unit
f_{MAX2}	Internal Local Feedback Maximum Frequency, lesser of $(1/(t_{S1} + t_{CF}))$ or $(1/t_{CO1})$[4, 15]	Com'l/Ind	55		43		33		MHz
		Mil	55		43		33		
f_{MAX3}	Data Path Maximum Frequency, least of $1/(t_{WL} + t_{WH})$, $1/(t_{S1} + t_H)$, or $(1/t_{CO1})$[4, 16]	Com'l/Ind	62.5		50		40		MHz
		Mil	62.5		50		40		
f_{MAX4}	Maximum Register Toggle Frequency $(1/(t_{WL} + t_{WH}))$[4, 17]	Com'l/Ind	62.5		50		40		MHz
		Mil	62.5		50		40		
t_{OH}	Output Data Stable Time from Synchronous Clock Input[4, 18]	Com'l/Ind	3		3		3		ns
		Mil	3		3		3		
t_{PW}	Asynchronous Preset Width[4, 7]	Com'l/Ind	25		30		35		ns
		Mil	25		30		35		

External Asynchronous Switching Characteristics Over Operating Range[6]

Parameter	Description		7C343B–12 Min.	7C343B–12 Max.	7C343B–15 Min.	7C343B–15 Max.	7C343–20 7C343B–20 Min.	7C343–20 7C343B–20 Max.	Unit
t_{ACO1}	Asynchronous Clock Input to Output Delay[7]	Com'l/Ind		12		15		20	ns
		Mil				15		20	
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output[19]	Com'l/Ind		20		25		32	ns
		Mil				25		32	
t_{AS1}	Dedicated Input or Feedback Set-Up Time to Asynchronous Clock Input[7]	Com'l/Ind	3		3.5		4		ns
		Mil			3.5		4		
t_{AS2}	I/O Input Set-Up Time to Asynchronous Clock Input[7]	Com'l/Ind	12		13.5		15		ns
		Mil			13.5		15		
t_{AH}	Input Hold Time from Asynchronous Clock Input[7]	Com'l/Ind	4		4.5		5		ns
		Mil			4.5		5		
t_{AWH}	Asynchronous Clock Input HIGH Time[7]	Com'l/Ind	8		8.5		9		ns
		Mil			8.5		9		
t_{AWL}	Asynchronous Clock Input LOW Time[7, 20]	Com'l/Ind	6		6.5		7		ns
		Mil			6.5		7		
t_{ACF}	Asynchronous Clock to Local Feedback Input[4, 21]	Com'l/Ind		9		11		13	ns
		Mil				11		13	
t_{AP}	External Asynchronous Clock Period $(1/f_{MAXA4})$[4]	Com'l/Ind	14		15		16		ns
		Mil			15		16		
f_{MAXA1}	External Maximum Frequency in Asynchronous Mode $1/(t_{ACO1} + t_{AS1})$[4, 22]	Com'l/Ind	66.6		54.0		41.6		MHz
		Mil			54.0		41.6		
f_{MAXA2}	Maximum Internal Asynchronous Frequency[4, 23]	Com'l/Ind	71.4		66.6		58.8		MHz
		Mil			66.6		58.8		
f_{MAXA3}	Data Path Maximum Frequency in Asynchronous Mode[4, 24]	Com'l/Ind	71.4		66.6		50		MHz
		Mil			66.6		50		
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[4, 25]	Com'l/Ind	71.4		66.6		62.5		MHz
		Mil			66.6		62.5		
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[4, 26]	Com'l/Ind	12		12		15		ns
		Mil			12		15		

Shaded areas contain advanced information.

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External Asynchronous Switching Characteristics Over Operating Range[6] (continued)

Parameter	Description		7C343–25 7C343B–25 Min.	7C343–25 7C343B–25 Max.	7C343–30 7C343B–30 Min.	7C343–30 7C343B–30 Max.	7C343–35 7C343B–35 Min.	7C343–35 7C343B–35 Max.	Unit
t_{ACO1}	Asynchronous Clock Input to Output Delay[7]	Com'l/Ind		25		30		35	ns
		Mil		25		30		35	
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output[19]	Com'l/Ind		40		46		55	ns
		Mil		40		46		55	
t_{AS1}	Dedicated Input or Feedback Set-Up Time to Asynchronous Clock Input[7]	Com'l/Ind	5		6		8		ns
		Mil	5		6		8		
t_{AS2}	I/O Input Set-Up Time to Asynchronous Clock Input[7]	Com'l/Ind	20		25		30		ns
		Mil	20		25		30		
t_{AH}	Input Hold Time from Asynchronous Clock Input[7]	Com'l/Ind	6		8		10		ns
		Mil	6		8		10		
t_{AWH}	Asynchronous Clock Input HIGH Time[7]	Com'l/Ind	11		14		16		ns
		Mil	11		14		16		
t_{AWL}	Asynchronous Clock Input LOW Time[7, 20]	Com'l/Ind	9		11		14		ns
		Mil	9		11		14		
t_{ACF}	Asynchronous Clock to Local Feedback Input[4, 21]	Com'l/Ind		15		18		22	ns
		Mil		15		18		22	
t_{AP}	External Asynchronous Clock Period ($1/f_{MAXA4}$)[4]	Com'l/Ind	20		25		30		ns
		Mil	20		25		30		
f_{MAXA1}	External Maximum Frequency in Asynchronous Mode $1/(t_{ACO1} + t_{AS1})$[4, 22]	Com'l/Ind	33		27		23		MHz
		Mil	33		27		23		
f_{MAXA2}	Maximum Internal Asynchronous Frequency[4, 23]	Com'l/Ind	50		40		33		MHz
		Mil	50		40		33		
f_{MAXA3}	Data Path Maximum Frequency in Asynchronous Mode[4, 24]	Com'l/Ind	40		33		28		MHz
		Mil	40		33		28		
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[4, 25]	Com'l/Ind	50		40		33		MHz
		Mil	50		40		33		
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[4, 26]	Com'l/Ind	15		15		15		ns
		Mil	15		15		15		

Notes:

19. This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used in the logic of combinatorial output or the asynchronous clock input. The clock signal is applied to a dedicated input pin and all feedback is within a single LAB. This parameter is tested periodically by sampling production material.
20. This parameter is measured with a positive-edge triggered clock at the register. For negative edge triggering, the t_{AWH} and t_{AWL} parameters must be swapped. If a given input is used to clock multiple registers with both positive and negative polarity, t_{AWH} should be used for both t_{AWH} and t_{AWL}.
21. This specification is a measure of the delay associated with the internal register feedback path for an asynchronous clock to LAB logic array input. This delay plus the asynchronous register set-up time, t_{AS1}, is the minimum internal period for an internal asynchronously clocked state machine configuration. This delay is for feedback within the same LAB, assumes no expander logic in the clock path, and assumes that the clock input signal is applied to a dedicated input pin. This parameter is tested periodically by sampling production material.
22. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that all data inputs, clock inputs, and feedback signals are applied to dedicated inputs, and that no expander logic is employed in the clock signal path or data path.

Internal Switching Characteristics Over Operating Range[6]

Parameter	Description		7C343B–12		7C343B–15		7C343–20 7C343B–20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay	Com'l/Ind		2.5		3		4	ns
		Mil				3		4	
t_{IO}	I/O Input Pad and Buffer Delay	Com'l/Ind		2.5		3		4	ns
		Mil				3		4	
t_{EXP}	Expander Array Delay	Com'l/Ind		6		8		10	ns
		Mil				8		10	
t_{LAD}	Logic Array Data Delay	Com'l/Ind		6		8		10	ns
		Mil				8		10	
t_{LAC}	Logic Array Control Delay	Com'l/Ind		5		6		8	ns
		Mil				6		8	
t_{OD}	Output Buffer and Pad Delay	Com'l/Ind		3		3		4	ns
		Mil				3		4	
t_{ZX}	Output Buffer Enable Delay[27]	Com'l/Ind		5		6		8	ns
		Mil				6		8	
t_{XZ}	Output Buffer Disable Delay	Com'l/Ind		5		6		8	ns
		Mil				6		8	
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	Com'l/Ind	2		3		4		ns
		Mil			3		4		
t_{RH}	Register Hold Time Relative to Clock Signal at Register	Com'l/Ind	3		3.5		4		ns
		Mil			3.5		4		
t_{LATCH}	Flow-Through Latch Delay	Com'l/Ind		1		1		2	ns
		Mil				1		2	
t_{RD}	Register Delay	Com'l/Ind		1		1		1	ns
		Mil				1		1	
t_{COMB}	Transparent Mode Delay[28]	Com'l/Ind		1		1		2	ns
		Mil				1		2	
t_{CH}	Clock HIGH Time	Com'l/Ind	3		4		6		ns
		Mil			4		6		
t_{CL}	Clock LOW Time	Com'l/Ind	3		4		6		ns
		Mil			4		6		
t_{IC}	Asynchronous Clock Logic Delay	Com'l/Ind		5		7		12	ns
		Mil				7		12	
t_{ICS}	Synchronous Clock Delay	Com'l/Ind		0.5		0.5		2	ns
		Mil				0.5		2	
t_{FD}	Feedback Delay	Com'l/Ind		1		1		1	ns
		Mil				1		1	
t_{PRE}	Asynchronous Register Preset Time	Com'l/Ind		3		3		4	ns
		Mil				3		4	
t_{CLR}	Asynchronous Register Clear Time	Com'l/Ind		3		3		4	ns
		Mil				3		4	
t_{PCW}	Asynchronous Preset and Clear Pulse Width	Com'l /Ind	2		3		4		ns
		Mil			3		4		
t_{PCR}	Asynchronous Preset and Clear Recovery Time	Com'l/Ind	2		3		4		ns
		Mil			3		4		
t_{PIA}	Programmable Interconnect Array Delay Time	Com'l/Ind		8		10		12	ns
		Mil				10		12	

Shaded areas contain advanced information.

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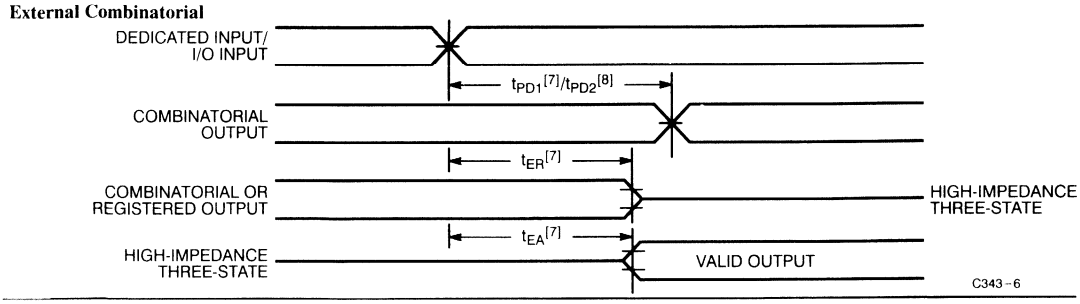
Internal Switching Characteristics Over Operating Range[6] (continued)

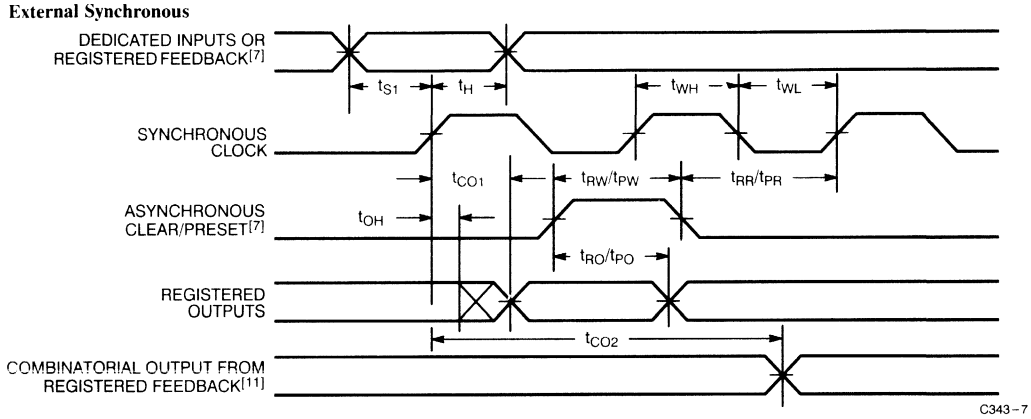
Parameter	Description		7C343–25 7C343B–25		7C343–30 7C343B–30		7C343–35 7C343B–35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay	Com'l/Ind		5		7		9	ns
		Mil		5		7		9	
t_{IO}	I/O Input Pad and Buffer Delay	Com'l/Ind		5		5		7	ns
		Mil		5		5		7	
t_{EXP}	Expander Array Delay	Com'l/Ind		12		14		20	ns
		Mil		12		14		20	
t_{LAD}	Logic Array Data Delay	Com'l/Ind		12		14		16	ns
		Mil		12		14		16	
t_{LAC}	Logic Array Control Delay	Com'l/Ind		10		12		13	ns
		Mil		10		12		13	
t_{OD}	Output Buffer and Pad Delay	Com'l/Ind		5		5		6	ns
		Mil		5		5		6	
t_{ZX}	Output Buffer Enable Delay[27]	Com'l/Ind		10		11		13	ns
		Mil		10		11		13	
t_{XZ}	Output Buffer Disable Delay	Com'l/Ind		10		11		13	ns
		Mil		10		11		13	
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	Com'l/Ind	6		8		10		ns
		Mil	6		8		10		
t_{RH}	Register Hold Time Relative to Clock Signal at Register	Com'l/Ind	6		8		12		ns
		Mil	6		8		12		
t_{LATCH}	Flow-Through Latch Delay	Com'l/Ind		3		4		4	ns
		Mil		3		4		4	
t_{RD}	Register Delay	Com'l/Ind		1		2		2	ns
		Mil		1		2		2	
t_{COMB}	Transparent Mode Delay[28]	Com'l/Ind		3		4		4	ns
		Mil		3		4		4	
t_{CH}	Clock HIGH Time	Com'l/Ind	8		10		12.5		ns
		Mil	8		10		12.5		
t_{CL}	Clock LOW Time	Com'l/Ind	8		10		12.5		ns
		Mil	8		10		12.5		
t_{IC}	Asynchronous Clock Logic Delay	Com'l/Ind		14		16		18	ns
		Mil		14		16		18	
t_{ICS}	Synchronous Clock Delay	Com'l/Ind		2		2		3	ns
		Mil		2		2		3	
t_{FD}	Feedback Delay	Com'l/Ind		1		1		2	ns
		Mil		1		1		2	
t_{PRE}	Asynchronous Register Preset Time	Com'l/Ind		5		6		7	ns
		Mil		5		6		7	
t_{CLR}	Asynchronous Register Clear Time	Com'l/Ind		5		6		7	ns
		Mil		5		6		7	
t_{PCW}	Asynchronous Preset and Clear Pulse Width	Com'l/Ind	5		6		7		ns
		Mil	5		6		7		
t_{PCR}	Asynchronous Preset and Clear Recovery Time	Com'l/Ind	5		6		7		ns
		Mil	5		6		7		
t_{PIA}	Programmable Interconnect Array Delay Time	Com'l/Ind		14		16		20	ns
		Mil		14		16		20	

Switching Waveforms

External Combinatorial



External Synchronous

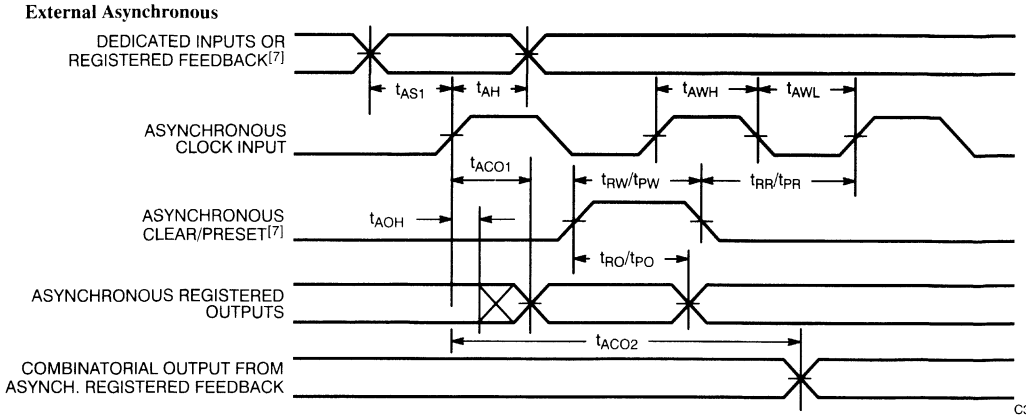


Notes:

23. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal-only feedback can operate. This parameter is determined by the lesser of ($1/t_{ACF} + t_{AS1}$)) or ($1/(t_{AWH} + t_{AWL})$). If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO1}$.
24. This frequency is the maximum frequency at which the device may operate in the asynchronously clocked data path mode. This specification is determined by the least of $1/(t_{AWH} + t_{AWL})$, $1/(t_{AS1} + t_{AH1})$ or $1/t_{ACO1}$. It assumes data and clock input signals are applied to dedicated input pins and no expander logic is used.
25. This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to an external dedicated input pin.
26. This parameter indicates the minimum time that the previous register output data is maintained on the output after an asynchronous register clock input.
27. Sample tested only for an output change of 500 mV.
28. This specification guarantees the maximum combinatorial delay associated with the macrocell register bypass when the macrocell is configured for combinatorial operation.

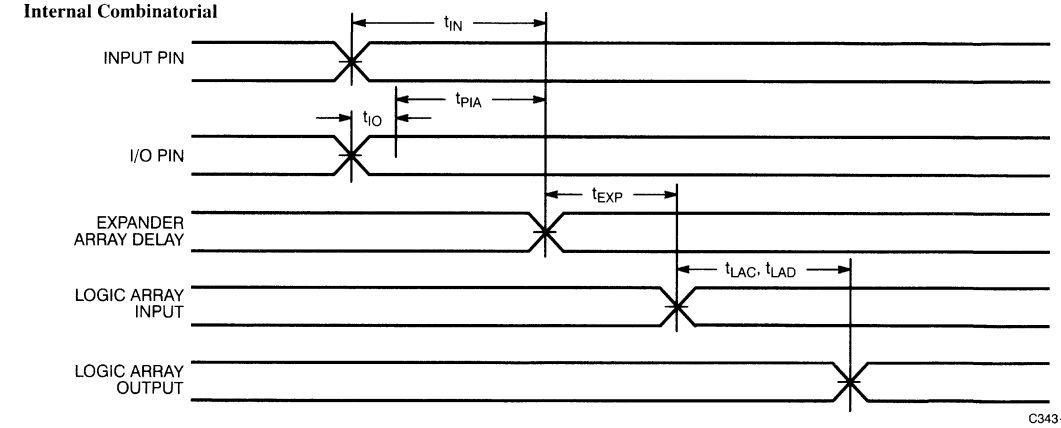
Switching Waveforms (continued)

External Asynchronous



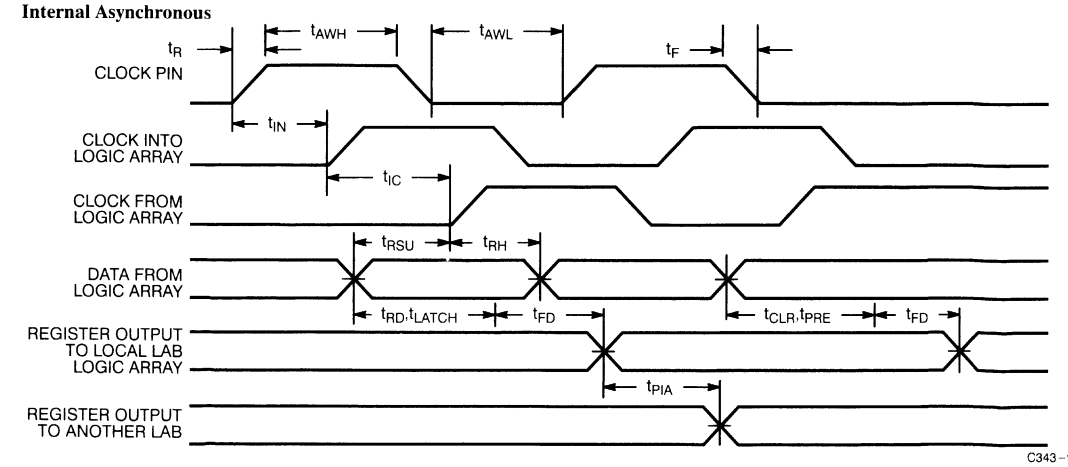
C343-10

Internal Combinatorial



C343-8

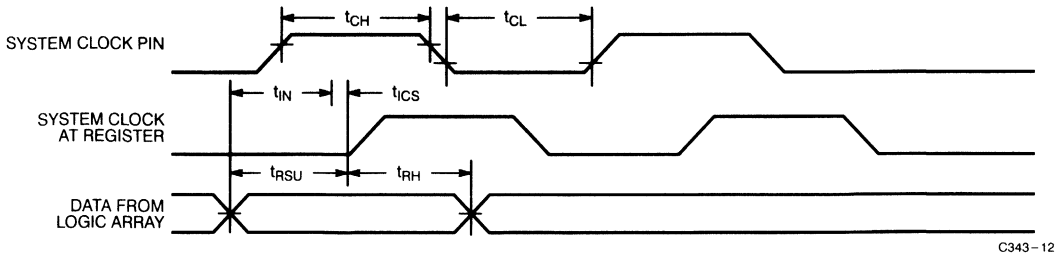
Internal Asynchronous



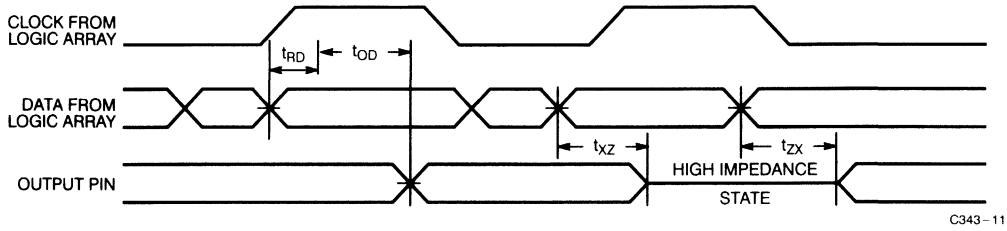
C343-9

Switching Waveforms (continued)

Internal Synchronous



Output Mode



3

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C343B–12HC/HI	H67	44-Pin Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C343B–12JC/JI	J67	44-Lead Plastic Leaded Chip Carrier	
15	CY7C343B–15HC/HI	H67	44-Pin Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C343B–15JC/JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C343B–15HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
20	CY7C343–20HC/HI	H67	44-Pin Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C343–20JC/JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C343B–20HC/HI	H67	44-Pin Windowed Leaded Chip Carrier	
	CY7C343B–20JC/JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C343B–20HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
25	CY7C343–25HC/HI	H67	44-Pin Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C343–25JC/JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C343B–25HC/HI	H67	44-Pin Windowed Leaded Chip Carrier	
	CY7C343B–25JC/JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C343–25HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C343B–25HMB	H67	44-Pin Windowed Leaded Chip Carrier	
30	CY7C343–30HC/HI	H67	44-Pin Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C343–30JC/JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C343B–30HC/HI	H67	44-Pin Windowed Leaded Chip Carrier	
	CY7C343B–30JC/JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C343–30HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C343B–30HMB	H67	44-Pin Windowed Leaded Chip Carrier	
35	CY7C343–35HC/HI	H67	44-Pin Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C343–35JC/JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C343B–35HC/HI	H67	44-Pin Windowed Leaded Chip Carrier	
	CY7C343B–35JC/JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C343–35HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C343B–35HMB	H67	44-Pin Windowed Leaded Chip Carrier	

Shaded area contains advanced information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD1}	7, 8, 9, 10, 11
t_{PD2}	7, 8, 9, 10, 11
t_{PD3}	7, 8, 9, 10, 11
t_{CO1}	7, 8, 9, 10, 11
t_S	7, 8, 9, 10, 11
t_H	7, 8, 9, 10, 11
t_{ACO1}	7, 8, 9, 10, 11
t_{ACO2}	7, 8, 9, 10, 11
t_{AS}	7, 8, 9, 10, 11
t_{AH}	7, 8, 9, 10, 11

Document #: 38-00128-F

CY7C344
CY7C344B

32-Macrocell MAX® EPLD

Features

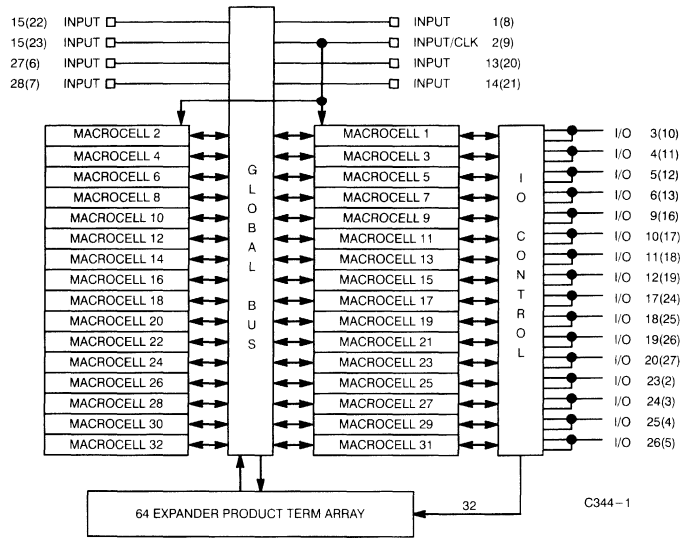
- **High-performance, high-density replacement for TTL, 74HC, and custom logic**
- **32 macrocells, 64 expander product terms in one LAB**
- **8 dedicated inputs, 16 I/O pins**
- **0.8-micron double-metal CMOS EPROM technology (CY7C344)**
- **Advanced 0.65-micron CMOS technology to increase performance (CY7C344B)**
- **28-pin 300-mil DIP, cerDIP or 28-pin HLCC, PLCC package**

Functional Description

Available in a 28-pin 300-mil DIP or windowed J-leaded ceramic chip carrier (HLCC), the CY7C344/CY7C344B represents the densest EPLD of this size. Eight dedicated inputs and 16 bidirectional I/O pins communicate to one logic array block. In the CY7C344 LAB there are 32 macrocells and 64 expander product terms. When an I/O macrocell is used as an input, two expanders are used to create an input path. Even if all of the I/O pins are driven by macrocell registers, there are still 16 "buried" registers available. All inputs, macrocells, and I/O pins are interconnected within the LAB.

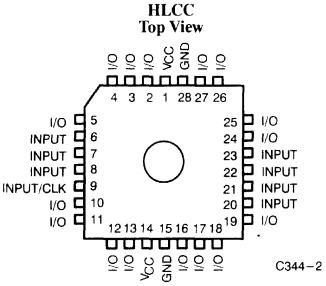
The speed and density of the CY7C344/CY7C344B makes it a natural for all types of applications. With just this one device, the designer can implement complex state machines, registered logic, and combinatorial "glue" logic, without using multiple chips. This architectural flexibility allows the CY7C344/CY7C344B to replace multichip TTL solutions, whether they are synchronous, asynchronous, combinatorial, or all three.

Logic Block Diagram[1]

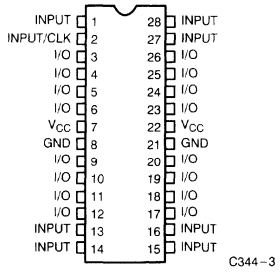


Pin Configurations

HLCC
Top View



CerDIP
Top View



Selection Guide

		7C344B-10	7C344B-12	7C344-15 7C344B-15	7C344-20 7C344B-20	7C344-25 7C344B-25	7C344-35
Maximum Access Time (ns)		10	12	15	20	25	35
Maximum Operating Current (mA)	Commercial	200	200	200	200	200	200
	Military		220		220	220	220
	Industrial		220	220	220	220	
Maximum Standby Current (mA)	Commercial	150	150	150	150	150	150
	Military		170		170	170	170
	Industrial		170	170	170	170	

Shaded area contains advanced information.

Note:

1. Numbers in parenthesis refer to J-leaded packages.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... 0°C to +70°C

Maximum Junction Temperature (Under Bias) ..... 150°C

Supply Voltage to Ground Potential ..... −2.0V to +7.0V

Maximum Power Dissipation ..... 1500 mW

DC V_{CC} or GND Current ..... 500 mA

Static Discharge Voltage (per MIL−STD−883, Method 3015) ..... >2001V

DC Output Current, per Pin ..... −25 mA to +25 mA

DC Input Voltage[2] ..... −3.0V to +7.0V

DC Program Voltage ..... +13.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±5%
Industrial	−40°C to +85°C	5V ±10%
Military	−55°C to +125°C (Case)	5V ±10%

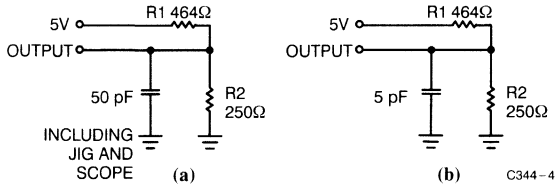
Electrical Characteristics Over the Operating Range[3]

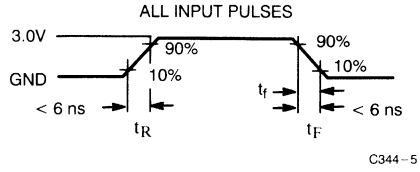
Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA			0.45	V
V_{IH}	Input HIGH Level			2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Level			−0.3	0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	µA
I_{OZ}	Output Leakage Current	V_O = V_{CC} or GND		−40	+40	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[4, 5]		−30	−90	mA
I_{CC1}	Power Supply Current (Standby)	V_I = V_{CC} or GND (No Load)	Commercial		150	mA
			Military/Industrial		170	mA
I_{CC2}	Power Supply Current	V_I = V_{CC} or GND (No Load) f = 1.0 MHz[4, 6]	Commercial		200	mA
			Military/Industrial		220	mA
t_R	Recommended Input Rise Time				100	ns
t_F	Recommended Input Fall Time				100	ns

Capacitance

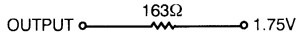
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2V, f = 1.0 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, f = 1.0 MHz	10	pF

AC Test Loads and Waveforms[7]





Equivalent to: THÉVENIN EQUIVALENT (commercial/military)



Notes:

2. Minimum DC input is −0.3V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns.
3. Typical values are for T_A = 25°C and V_{CC} = 5V.
4. Guaranteed by design but not 100% tested.
5. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
6. Measured with device programmed as a 16-bit counter.
7. Part (a) in AC Test Load and Waveforms is used for all parameters except t_{ER} and t_{XZ}, which is used for part (b) in AC Test Load and Waveforms. All external timing parameters are measured referenced to external pins of the device.

Timing Delays

Timing delays within the CY7C344/CY7C344B may be easily determined using *Warp2™*, *Warp3™* or MAX+PLUS® software or by the model shown in *Figure 1*. The CY7C344/CY7C344B has fixed internal delays, allowing the user to determine the worst case timing delays for any design. For complete timing information, the *Warp3* or MAX+PLUS software provides a timing simulator.

Design Recommendations

Operation of the devices described herein with conditions above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this datasheet is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect device reliability. The CY7C344/CY7C344B contains circuitry to protect device pins from high-static voltages or electric fields; however, normal precautions should be taken to avoid applying any voltage higher than maximum rated voltages.

For proper operation, input and output pins must be constrained to the range GND $\leq$ (V_{IN} or V_{OUT}) $\leq V_{CC}$. Unused inputs must always be tied to an appropriate logic level (either V_{CC} or GND). Each set of V_{CC} and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 µF must be connected between V_{CC} and GND. For the most effective decoupling, each V_{CC} pin should be separately decoupled.

Timing Considerations

Unless otherwise stated, propagation delays do not include expanders. When using expanders, add the maximum expander delay t_{EXP} to the overall delay.

When calculating synchronous frequencies, use t_{S1} if all inputs are on the input pins. t_{S2} should be used if data is applied at an I/O pin. If t_{S2} is greater than t_{CO1}, $1/t_{S2}$ becomes the limiting frequency in the data-path mode unless $1/(t_{WH} + t_{WL})$ is less than $1/t_{S2}$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{S1}. Determine which of $1/(t_{WH} + t_{WL})$, $1/t_{CO1}$, or $1/(t_{EXP} + t_{S1})$ is the lowest frequency. The lowest of these frequencies is the maximum data-path frequency for the synchronous configuration.

When calculating external asynchronous frequencies, use t_{AS1} if all inputs are on dedicated input pins. If any data is applied to an I/O pin, t_{AS2} must be used as the required set-up time. If $(t_{AS2} + t_{AH})$ is greater than t_{ACO1}, $1/(t_{AS2} + t_{AH})$ becomes the limiting frequency in the data-path mode unless $1/(t_{AWH} + t_{AWL})$ is less than $1/(t_{AS2} + t_{AH})$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{AS1}. Determine which of $1/(t_{AWH} + t_{AWL})$, $1/t_{ACO1}$, or $1/(t_{EXP} + t_{AS1})$ is the lowest frequency. The lowest of these frequencies is the maximum data-path frequency for the asynchronous configuration.

The parameter t_{OH} indicates the system compatibility of this device when driving other synchronous logic with positive input hold times, which is controlled by the same synchronous clock. If t_{OH} is greater than the minimum required input hold time of the subsequent synchronous logic, then the devices are guaranteed to function properly with a common synchronous clock under worst-case environmental and supply voltage conditions.

The parameter t_{AOH} indicates the system compatibility of this device when driving subsequent registered logic with a positive hold time and using the same clock as the CY7C344/CY7C344B.

In general, if t_{AOH} is greater than the minimum required input hold time of the subsequent logic (synchronous or asynchronous), then the devices are guaranteed to function properly under worst-case environmental and supply voltage conditions, provided the clock signal source is the same. This also applies if expander logic is used in the clock signal path of the driving device, but not for the driven device. This is due to the expander logic in the second device's clock signal path adding an additional delay (t_{EXP}), causing the output data from the preceding device to change prior to the arrival of the clock signal at the following device's register.

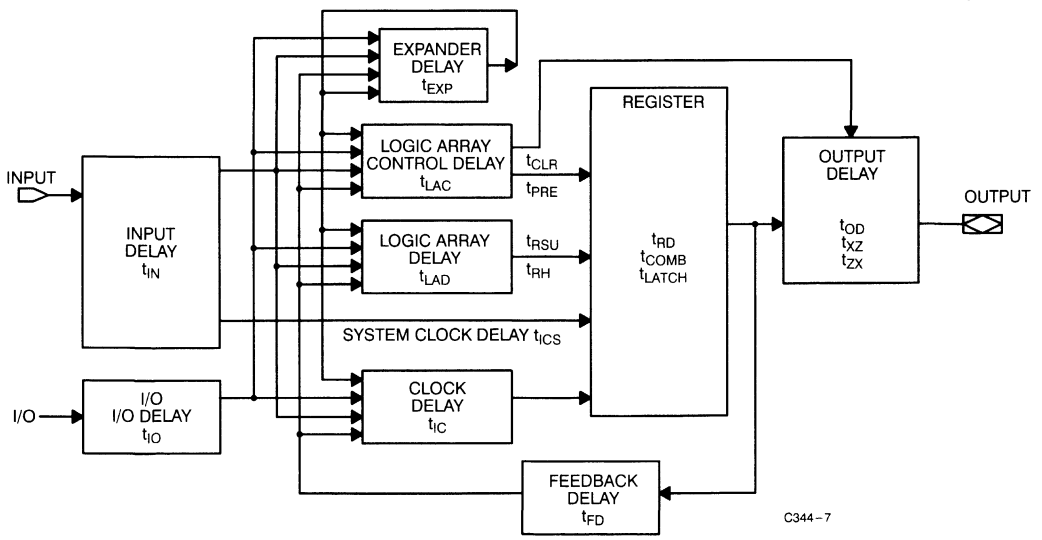


Figure 1. CY7C344/CY7C344B Timing Model

External Synchronous Switching Characteristics[7] Over Operating Range

Parameter	Description		7C344B–10		7C344B–12		7C344–15 7C344B–15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[8]	Com'l/Ind		10		12		15	ns
		Mil				12		15	
t_{PD2}	I/O Input to Combinatorial Output Delay[9]	Com'l/Ind		10		12		15	ns
		Mil				12		15	
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[10]	Com'l/Ind		16		18		30	ns
		Mil				18		30	
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[4, 11]	Com'l/Ind		16		18		30	ns
		Mil				18		30	
t_{EA}	Input to Output Enable Delay[4]	Com'l/Ind		10		12		20	ns
		Mil				12		20	
t_{ER}	Input to Output Disable Delay[4]	Com'l/Ind		10		12		20	ns
		Mil				12		20	
t_{CO1}	Synchronous Clock Input to Output Delay	Com'l/Ind		5		6		10	ns
		Mil				6		10	
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[4, 12]	Com'l/Ind		10		12		20	ns
		Mil				12		20	
t_S	Dedicated Input or Feedback Set-Up Time to Synchronous Clock Input	Com'l/Ind	6		8		10		ns
		Mil			8		10		
t_H	Input Hold Time from Synchronous Clock Input[7]	Com'l/Ind	0		0		0		ns
		Mil			0		0		
t_{WH}	Synchronous Clock Input HIGH Time[4]	Com'l/Ind	4		4.5		6		ns
		Mil			4.5		6		
t_{WL}	Synchronous Clock Input LOW Time[4]	Com'l/Ind	4		4.5		6		ns
		Mil			4.5		6		
t_{RW}	Asynchronous Clear Width[4]	Com'l/Ind	10		12		20		ns
		Mil			12		20		
t_{RR}	Asynchronous Clear Recovery Time[4]	Com'l/Ind	10		12		20		ns
		Mil			12		20		
t_{RO}	Asynchronous Clear to Registered Output Delay[4]	Com'l/Ind		10		12		15	ns
		Mil				12		15	
t_{PW}	Asynchronous Preset Width[4]	Com'l/Ind	10		12		20		ns
		Mil			12		20		
t_{PR}	Asynchronous Preset Recovery Time[4]	Com'l/Ind	10		12		20		ns
		Mil			12		20		
t_{PO}	Asynchronous Preset to Registered Output Delay[4]	Com'l/Ind		10		12		15	ns
		Mil				12		15	
t_{CF}	Synchronous Clock to Local Feedback Input[4, 13]	Com'l/Ind		3		3		4	ns
		Mil				3		4	

Shaded area contains advanced information.

External Synchronous Switching Characteristics[7] Over Operating Range (continued)

Parameter	Description		7C344B–10 Min.	7C344B–10 Max.	7C344B–12 Min.	7C344B–12 Max.	7C344–15 7C344B–15 Min.	7C344–15 7C344B–15 Max.	Unit
t_P	External Synchronous Clock Period ($1/f_{MAX3}$)[4]	Com'l/Ind	8		9		13		ns
		Mil			9		13		
f_{MAX1}	External Maximum Frequency($1/(t_{CO1}+t_S)$)[4, 14]	Com'l/Ind	90.9		71.4		50.0		MHz
		Mil			71.4		50.0		
f_{MAX2}	Maximum Frequency with Internal Only Feedback ($1/(t_{CF}+t_S)$)[4, 15]	Com'l/Ind	111.1		90.9		71.4		MHz
		Mil			90.9		71.4		
f_{MAX3}	Data Path Maximum Frequency, least of $1/(t_{WL}+t_{WH})$, $1/(t_S+t_H)$, or $(1/t_{CO1})$[4, 16]	Com'l/Ind	125.0		111.1		83.3		MHz
		Mil			111.1		83.3		
f_{MAX4}	Maximum Register Toggle Frequency $1/(t_{WL}+t_{WH})$[4, 17]	Com'l/Ind	125.0		111.1		83.3		MHz
		Mil			111.1		83.3		
t_{OH}	Output Data Stable Time from Synchronous Clock Input[4, 18]	Com'l/Ind	3		3		3		ns
		Mil			3		3		

Shaded area contains advanced information.

Notes:

8. This parameter is the delay from an input signal applied to a dedicated input pin to a combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function.
9. This parameter is the delay associated with an input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.
10. This parameter is the delay associated with an input signal applied to a dedicated input pin to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
11. This parameter is the delay associated with an input signal applied to an I/O macrocell pin to any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
12. This specification is a measure of the delay from synchronous register clock input to internal feedback of the register output signal to a combinatorial output for which the registered output signal is used as an input. This parameter assumes no expanders are used in the logic of the combinatorial output and the register is synchronously clocked. This parameter is tested periodically by sampling production material.
13. This specification is a measure of the delay associated with the internal register feedback path. This delay plus the register set-up time, t_S, is the minimum internal period for an internal state machine configuration. This parameter is tested periodically by sampling production material.
14. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external only feedback can operate.
15. This specification indicates the guaranteed maximum frequency at which a state machine with internal-only feedback can operate. If register output states must also control external points, this frequency can still be observed as long as it is less than $1/t_{CO1}$. This specification assumes no expander logic is used. This parameter is tested periodically by sampling production material.
16. This frequency indicates the maximum frequency at which the device may operate in data-path mode (dedicated input pin to output pin). This assumes that no expander logic is used.
17. This specification indicates the guaranteed maximum frequency in synchronous mode, at which an individual output or buried register can be cycled by a clock signal applied to either a dedicated input pin or an I/O pin.
18. This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.

External Synchronous Switching Characteristics[7] Over Operating Range (continued)

Parameter	Description		7C344–20 7C344B–20		7C344–25 7C344B–25		7C344–35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[8]	Com'l/Ind		20		25			ns
		Mil		20		25		35	
t_{PD2}	I/O Input to Combinatorial Output Delay[9]	Com'l/Ind		20		25			ns
		Mil		20		25		35	
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[10]	Com'l/Ind		30		40			ns
		Mil		30		40		55	
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[4, 11]	Com'l/Ind		30		40			ns
		Mil		30		40		55	
t_{EA}	Input to Output Enable Delay[4]	Com'l/Ind		20		25			ns
		Mil		20		25		35	
t_{ER}	Input to Output Disable Delay[4]	Com'l/Ind		20		25			ns
		Mil		20		25		35	
t_{CO1}	Synchronous Clock Input to Output Delay	Com'l/Ind		12		15			ns
		Mil		12		15		20	
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[4, 12]	Com'l/Ind		22		29			ns
		Mil		22		29		37	
t_S	Dedicated Input or Feedback Set-Up Time to Synchronous Clock Input	Com'l/Ind	12		15				ns
		Mil	12		15		21		
t_H	Input Hold Time from Synchronous Clock Input[7]	Com'l/Ind	0		0				ns
		Mil	0		0		0		
t_{WH}	Synchronous Clock Input HIGH Time[4]	Com'l/Ind	7		8				ns
		Mil	7		8		10		
t_{WL}	Synchronous Clock Input LOW Time[4]	Com'l/Ind	7		8				ns
		Mil	7		8		10		
t_{RW}	Asynchronous Clear Width[4]	Com'l/Ind	20		25				ns
		Mil	20		25		35		
t_{RR}	Asynchronous Clear Recovery Time[4]	Com'l/Ind	20		25				ns
		Mil	20		25		35		
t_{RO}	Asynchronous Clear to Registered Output Delay[4]	Com'l/Ind		20		25			ns
		Mil		20		25		35	
t_{PW}	Asynchronous Preset Width[4]	Com'l/Ind	20		25				ns
		Mil	20		25		35		
t_{PR}	Asynchronous Preset Recovery Time[4]	Com'l/Ind	20		25				ns
		Mil	20		25		35		
t_{PO}	Asynchronous Preset to Registered Output Delay[4]	Com'l/Ind		20		25			ns
		Mil		20		25		35	
t_{CF}	Synchronous Clock to Local Feedback Input[4, 13]	Com'l/Ind		4		7			ns
		Mil		4		7		13	
t_P	External Synchronous Clock Period ($1/f_{MAX3}$)[4]	Com'l/Ind	14		16				ns
		Mil	14		16		20		

3

External Synchronous Switching Characteristics[7] Over Operating Range (continued)

Parameter	Description		7C344–20 7C344B–20 Min.	7C344–20 7C344B–20 Max.	7C344–25 7C344B–25 Min.	7C344–25 7C344B–25 Max.	7C344–35 Min.	7C344–35 Max.	Unit
f_{MAX1}	External Maximum Frequency$(1/(t_{CO1} + t_S))$[4, 14]	Com'l/Ind	41.6		33.3				MHz
		Mil	41.6		33.3		24.3		
f_{MAX2}	Maximum Frequency with Internal Only Feedback $(1/(t_{CF} + t_S))$[4, 15]	Com'l/Ind	62.5		45.4				MHz
		Mil	62.5		45.4		29.4		
f_{MAX3}	Data Path Maximum Frequency, least of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $(1/t_{CO1})$[4, 16]	Com'l/Ind	71.4		62.5				MHz
		Mil	71.4		62.5		47.6		
f_{MAX4}	Maximum Register Toggle Frequency $1/(t_{WL} + t_{WH})$[4, 17]	Com'l/Ind	71.4		62.5				MHz
		Mil	71.4		62.5		50.0		
t_{OH}	Output Data Stable Time from Synchronous Clock Input[4, 18]	Com'l/Ind	3		3				ns
		Mil	3		3		3		

External Asynchronous Switching Characteristics Over Operating Range[7]

Parameter	Description		7C344B–10 Min.	7C344B–10 Max.	7C344B–12 Min.	7C344B–12 Max.	7C344–15 7C344B–15 Min.	7C344–15 7C344B–15 Max.	Unit
t_{ACO1}	Asynchronous Clock Input to Output Delay	Com'l/Ind		10		12		15	ns
		Mil				12		15	
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output[19]	Com'l/Ind		15		18		30	ns
		Mil				18		30	
t_{AS}	Dedicated Input or Feedback Set-Up Time to Asynchronous Clock Input	Com'l/Ind	4		4		7		ns
		Mil			4		7		
t_{AH}	Input Hold Time from Asynchronous Clock Input	Com'l/Ind	3		4		7		ns
		Mil			4		7		
t_{AWH}	Asynchronous Clock Input HIGH Time[4, 20]	Com'l/Ind	4		5		6		ns
		Mil			5		6		
t_{AWL}	Asynchronous Clock Input LOW Time[4]	Com'l/Ind	5		6		7		ns
		Mil			6		7		
t_{ACF}	Asynchronous Clock to Local Feedback Input[4, 21]	Com'l/Ind		7		9		18	ns
		Mil				9		18	
t_{AP}	External Asynchronous Clock Period $(1/f_{MAX4})$[4]	Com'l/Ind	12		12.5		13		ns
		Mil			12.5		13		
f_{MAXA1}	External Maximum Frequency in Asynchronous Mode $1/(t_{ACO1} + t_{AS})$[4, 22]	Com'l/Ind	71.4		62.5		45.4		MHz
		Mil			62.5		45.4		
f_{MAXA2}	Maximum Internal Asynchronous Frequency $1/(t_{ACF} + t_{AS})$ or $1/(t_{AWH} + t_{AWL})$[4, 23]	Com'l/Ind	90.9		76.9		40		MHz
		Mil			76.9		40		
f_{MAXA3}	Data Path Maximum Frequency in Asynchronous Mode[4, 24]	Com'l/Ind	100.0		83.3		66.6		MHz
		Mil			83.3		66.6		
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[4, 25]	Com'l/Ind	111.1		90.9		76.9		MHz
		Mil			90.9		76.9		
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[4, 26]	Com'l/Ind	12		12		15		ns
		Mil					15		

Shaded area contains advanced information.

External Asynchronous Switching Characteristics Over Operating Range[7] (continued)

Parameter	Description		7C344–20 7C344B–20 Min.	7C344–20 7C344B–20 Max.	7C344–25 7C344B–25 Min.	7C344–25 7C344B–25 Max.	7C344–35 Min.	7C344–35 Max.	Unit
t_{ACO1}	Asynchronous Clock Input to Output Delay	Com'l/Ind		20		25			ns
		Mil		20		25		35	
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output[19]	Com'l/Ind		30		37			ns
		Mil		30		37		49	
t_{AS}	Dedicated Input or Feedback Set-Up Time to Asynchronous Clock Input	Com'l/Ind	9		12				ns
		Mil	9		12		15		
t_{AH}	Input Hold Time from Asynchronous Clock Input	Com'l/Ind	9		12				ns
		Mil	9		12		17.5		
t_{AWH}	Asynchronous Clock Input HIGH Time[4, 20]	Com'l/Ind	7		9				ns
		Mil	7		9		15		
t_{AWL}	Asynchronous Clock Input LOW Time[4]	Com'l/Ind	9		11				ns
		Mil	9		11		15		
t_{ACF}	Asynchronous Clock to Local Feedback Input[4, 21]	Com'l/Ind		18		21			ns
		Mil		18		21		27	
t_{AP}	External Asynchronous Clock Period ($1/f_{MAX4}$)[4]	Com'l/Ind	16		20				ns
		Mil	16		20		30		
f_{MAXA1}	External Maximum Frequency in Asynchronous Mode $1/(t_{ACO1} + t_{AS})$[4, 22]	Com'l/Ind	34.4		27				MHz
		Mil	34.4		27		20		
f_{MAXA2}	Maximum Internal Asynchronous Frequency $1/(t_{ACF} + t_{AS})$ or $1/(t_{AWH} + t_{AWL})$[4, 23]	Com'l/Ind	37		30.3				MHz
		Mil	37		30.3		23.8		
f_{MAXA3}	Data Path Maximum Frequency in Asynchronous Mode[4, 24]	Com'l/Ind	50		40				MHz
		Mil	50		40		28.5		
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[4, 25]	Com'l/Ind	62.5		50				MHz
		Mil	62.5		50		33.3		
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[4, 26]	Com'l/Ind	15		15				ns
		Mil	15		15		15		

Notes:

19. This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the registered output signal to a combinatorial output for which the registered output signal is used as an input. Assumes no expanders are used in logic of combinatorial output or the asynchronous clock input. This parameter is tested periodically by sampling production material.
20. This parameter is measured with a positive-edge-triggered clock at the register. For negative edge triggering, the t_{AWH} and t_{AWL} parameters must be swapped. If a given input is used to clock multiple registers with both positive and negative polarity, t_{AWH} should be used for both t_{AWH} and t_{AWL}.
21. This specification is a measure of the delay associated with the internal register feedback path for an asynchronously clocked register. This delay plus the asynchronous register set-up time, t_{AS}, is the minimum internal period for an asynchronously clocked state machine configuration. This delay assumes no expander logic in the asynchronous clock path. This parameter is tested periodically by sampling production material.
22. This parameter indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that no expander logic is employed in the clock signal path or data path.
23. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal-only feedback can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO1}$. This specification assumes no expander logic is utilized. This parameter is tested periodically by sampling production material.
24. This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode. This frequency is least of $1/(t_{AWH} + t_{AWL})$, $1/(t_{AS} + t_{AH})$, or $1/t_{ACO1}$. It also indicates the maximum frequency at which the device may operate in the asynchronously clocked data-path mode. Assumes no expander logic is used.
25. This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to an external dedicated input or an I/O pin.
26. This parameter indicates the minimum time that the previous register output data is maintained on the output pin after an asynchronous register clock input to an external dedicated input or I/O pin.

Typical Internal Switching Characteristics Over Operating Range[7]

Parameter	Description		7C344B–10		7C344B–12		7C344–15 7C344B–15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay	Com'l/Ind		2		2.5		4	ns
		Mil				2.5		4	
t_{IO}	I/O Input Pad and Buffer Delay	Com'l/Ind		2		2.5		4	ns
		Mil				2.5		4	
t_{EXP}	Expander Array Delay	Com'l/Ind		6		6		8	ns
		Mil				6		8	
t_{LAD}	Logic Array Data Delay	Com'l/Ind		5		6		7	ns
		Mil				6		7	
t_{LAC}	Logic Array Control Delay	Com'l/Ind		5		5		5	ns
		Mil				5		5	
t_{OD}	Output Buffer and Pad Delay	Com'l/Ind		3		3		4	ns
		Mil				3		4	
t_{ZX}	Output Buffer Enable Delay[27]	Com'l/Ind		5		5		7	ns
		Mil				5		7	
t_{XZ}	Output Buffer Disable Delay	Com'l/Ind		5		5		7	ns
		Mil				5		7	
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	Com'l/Ind	2		2		5		ns
		Mil			2		5		
t_{RH}	Register Hold Time Relative to Clock Signal at Register	Com'l/Ind	4		5		7		ns
		Mil			5		7		
t_{LATCH}	Flow-Through Latch Delay	Com'l/Ind		0.5		0.5		1	ns
		Mil				0.5		1	
t_{RD}	Register Delay	Com'l/Ind		0.5		0.5		1	ns
		Mil				0.5		1	
t_{COMB}	Transparent Mode Delay[28]	Com'l/Ind		0.5		0.5		1	ns
		Mil				0.5		1	
t_{CH}	Clock HIGH Time	Com'l/Ind	3		4		6		ns
		Mil			4		6		
t_{CL}	Clock LOW Time	Com'l/Ind	3		4		6		ns
		Mil			4		6		
t_{IC}	Asynchronous Clock Logic Delay	Com'l/Ind		5		6		7	ns
		Mil				6		7	
t_{ICS}	Synchronous Clock Delay	Com'l/Ind		0.5		0.5		1	ns
		Mil				0.5		1	
t_{FD}	Feedback Delay	Com'l/Ind		1		1		1	ns
		Mil				1		1	
t_{PRE}	Asynchronous Register Preset Time	Com'l/Ind		2		3		5	ns
		Mil				3		5	
t_{CLR}	Asynchronous Register Clear Time	Com'l/Ind		2		3		5	ns
		Mil				3		5	
t_{PCW}	Asynchronous Preset and Clear Pulse Width	Com'l/Ind	2		3		5		ns
		Mil			3		5		
t_{PCR}	Asynchronous Preset and Clear Recovery Time	Com'l/Ind	2		3		5		ns
		Mil			3		5		

Shaded area contains advanced information.

Note:

27. Sample tested only for an output change of 500 mV.
28. This specification guarantees the maximum combinatorial delay associated with the macrocell register bypass when the macrocell is configured for combinatorial operation.

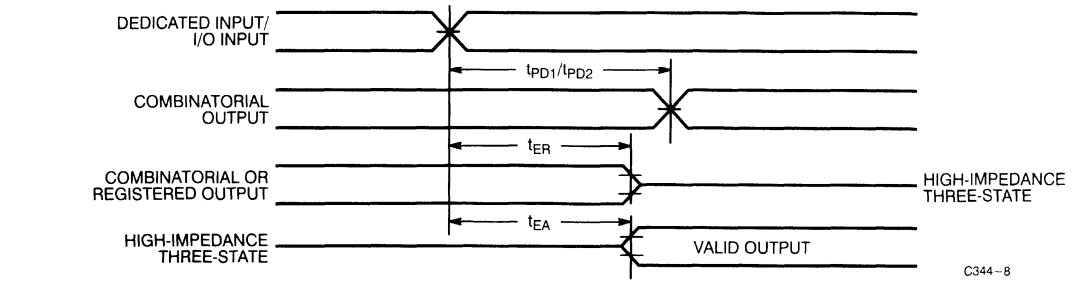
Typical Internal Switching Characteristics Over Operating Range[7] (continued)

Parameter	Description		7C344–20 7C344B–20		7C344–25 7C344B–25		7C344–35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay	Com'l/Ind		5		7			ns
		Mil		5		7		11	
t_{IO}	I/O Input Pad and Buffer Delay	Com'l/Ind		5		7			ns
		Mil		5		7		11	
t_{EXP}	Expander Array Delay	Com'l/Ind		10		15			ns
		Mil		10		15		20	
t_{LAD}	Logic Array Data Delay	Com'l/Ind		9		10			ns
		Mil		9		10		11	
t_{LAC}	Logic Array Control Delay	Com'l/Ind		7		7			ns
		Mil		7		7		7	
t_{OD}	Output Buffer and Pad Delay	Com'l/Ind		5		5			ns
		Mil		5		5		8	
t_{ZX}	Output Buffer Enable Delay[27]	Com'l/Ind		8		11			ns
		Mil		8		11		12	
t_{XZ}	Output Buffer Disable Delay	Com'l/Ind		8		11			ns
		Mil		8		11		12	
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	Com'l/Ind	5		8				ns
		Mil	5		8		11		
t_{RH}	Register Hold Time Relative to Clock Signal at Register	Com'l/Ind	9		12				ns
		Mil	9		12		15		
t_{LATCH}	Flow-Through Latch Delay	Com'l/Ind		1		3			ns
		Mil		1		3		5	
t_{RD}	Register Delay	Com'l/Ind		1		1			ns
		Mil		1		1		1	
t_{COMB}	Transparent Mode Delay[28]	Com'l/Ind		1		3			ns
		Mil		1		3		5	
t_{CH}	Clock HIGH Time	Com'l/Ind	7		8				ns
		Mil	7		8		9		
t_{CL}	Clock LOW Time	Com'l/Ind	7		8				ns
		Mil	7		8		9		
t_{IC}	Asynchronous Clock Logic Delay	Com'l/Ind		8		10			ns
		Mil		8		10		12	
t_{ICS}	Synchronous Clock Delay	Com'l/Ind		2		3			ns
		Mil		2		3		5	
t_{FD}	Feedback Delay	Com'l/Ind		1		1			ns
		Mil		1		1		1	
t_{PRE}	Asynchronous Register Preset Time	Com'l/Ind		6		9			ns
		Mil		6		9		12	
t_{CLR}	Asynchronous Register Clear Time	Com'l/Ind		6		9			ns
		Mil		6		9		12	
t_{PCW}	Asynchronous Preset and Clear Pulse Width	Com'l/Ind	5		7				ns
		Mil	5		7		9		
t_{PCR}	Asynchronous Preset and Clear Recovery Time	Com'l/Ind	5		7				ns
		Mil	5		7		9		

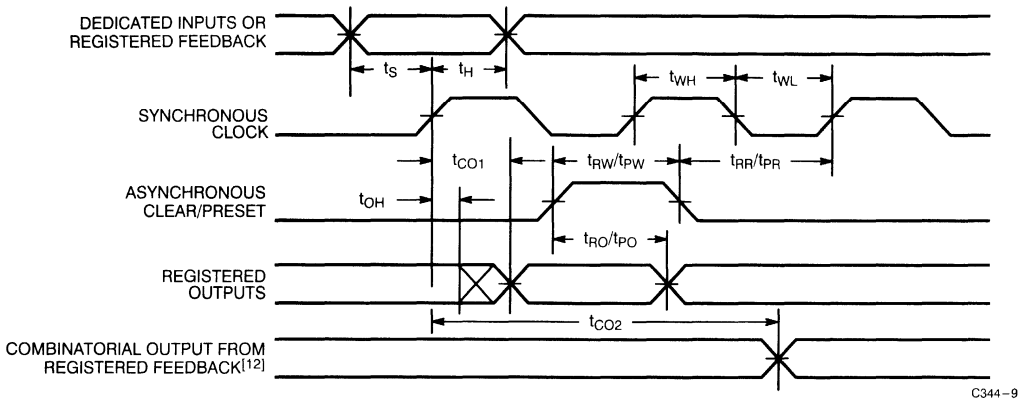
3

Switching Waveforms

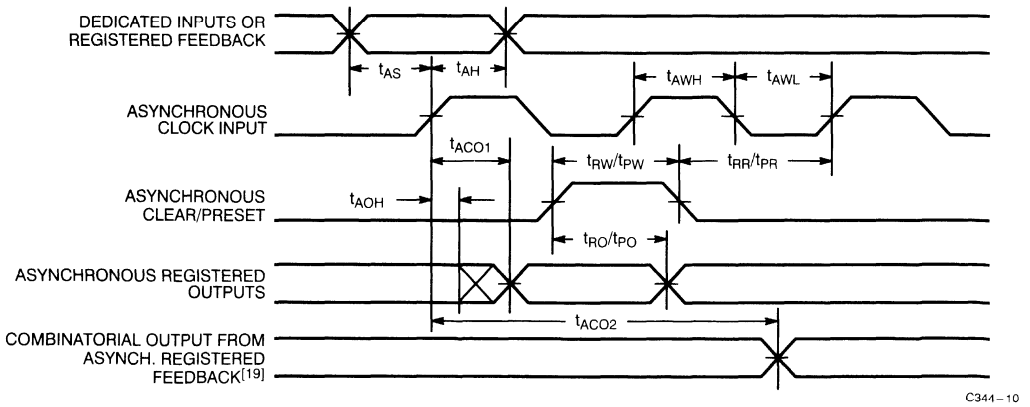
External Combinatorial



External Synchronous

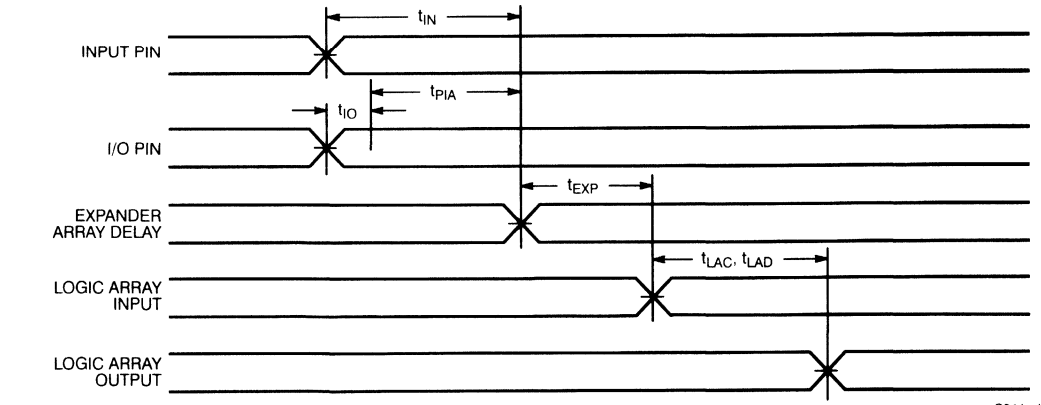


External Asynchronous

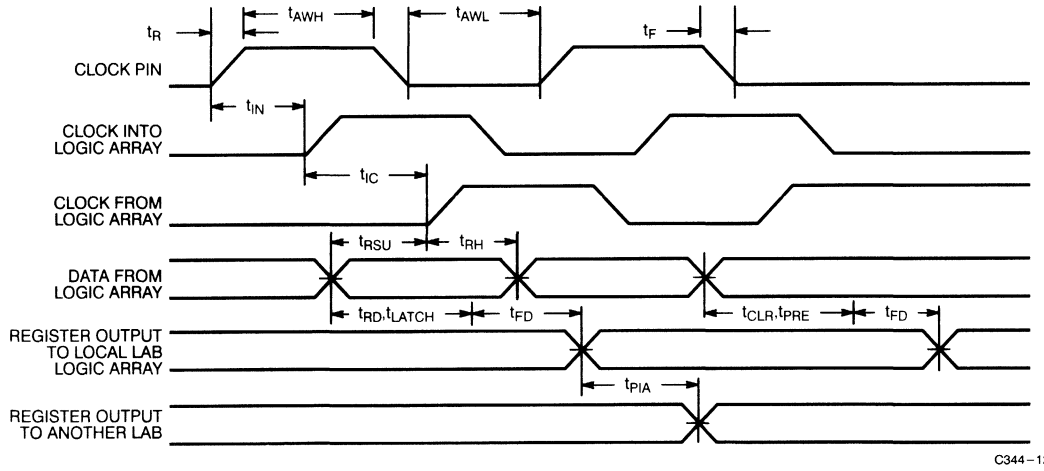


Switching Waveforms (continued)

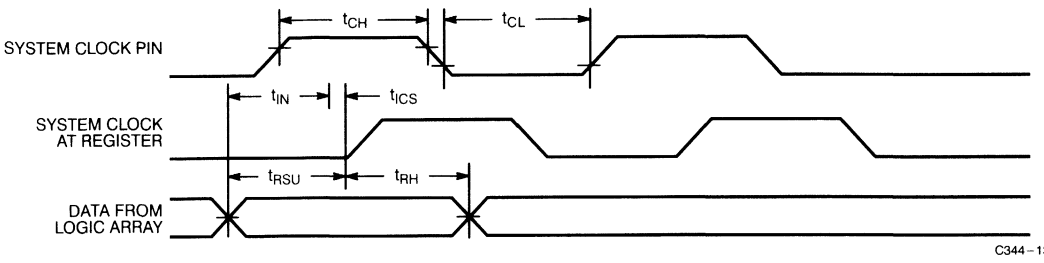
Internal Combinatorial



Internal Asynchronous

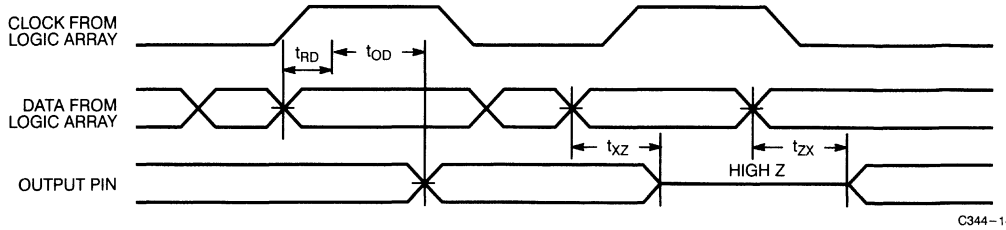


Internal Synchronous (Input Path)



Switching Waveforms (continued)

Internal Synchronous (Output Path)



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C344B–10HC	H64	28-Lead Windowed Leaded Chip Carrier	Commercial
	CY7C344B–10JC	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C344B–10PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C344B–10WC	W22	28-Lead Windowed CerDIP	
12	CY7C344B–12HC/HI	H64	28-Lead Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C344B–12JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C344B–12PC/PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C344B–12WC/WI	W22	28-Lead Windowed CerDIP	
	CY7C344B–12HMB	H64	28-Lead Windowed Leaded Chip Carrier	Military
	CY7C344B–12WMB	W22	28-Lead Windowed CerDIP	
15	CY7C344–15HC/HI	H64	28-Lead Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C344–15JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C344–15PC/PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C344–15WC/WI	W22	28-Lead Windowed CerDIP	
	CY7C344B–15HC/HI	H64	28-Lead Windowed Leaded Chip Carrier	
	CY7C344B–15JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C344B–15PC/PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C344B–15WC/WI	W22	28-Lead Windowed CerDIP	
	CY7C344B–15HMB	H64	28-Lead Windowed Leaded Chip Carrier	Military
	CY7C344B–15WMB	W22	28-Lead Windowed CerDIP	
20	CY7C344–20HC/HI	H64	28-Lead Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C344–20JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C344–20PC/PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C344–20WC/WI	W22	28-Lead Windowed CerDIP	
	CY7C344B–20HC/HI	H64	28-Lead Windowed Leaded Chip Carrier	
	CY7C344B–20JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C344B–20PC/PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C344B–20WC/WI	W22	28-Lead Windowed CerDIP	
	CY7C344–20HMB	H64	28-Lead Windowed Leaded Chip Carrier	Military
	CY7C344–20WMB	W22	28-Lead Windowed CerDIP	
	CY7C344B–20HMB	H64	28-Lead Windowed Leaded Chip Carrier	
	CY7C344B–20WMB	W22	28-Lead Windowed CerDIP	
25	CY7C344–25HC/HI	H64	28-Lead Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C344–25JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C344–25PC/PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C344–25WC/WI	W22	28-Lead Windowed CerDIP	
	CY7C344B–25HC/HI	H64	28-Lead Windowed Leaded Chip Carrier	
	CY7C344B–25JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C344B–25PC/PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C344B–25WC/WI	W22	28-Lead Windowed CerDIP	
	CY7C344–25HMB	H64	28-Lead Windowed Leaded Chip Carrier	Military
	CY7C344–25WMB	W22	28-Lead Windowed CerDIP	
	CY7C344B–25HMB	H64	28-Lead Windowed Leaded Chip Carrier	
	CY7C344B–25WMB	W22	28-Lead Windowed CerDIP	
35	CY7C344–35HMB	H64	28-Lead Windowed Leaded Chip Carrier	Military
	CY7C344–35WMB	W22	28-Lead Windowed CerDIP	

Shaded area contains advanced information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD1}	7, 8, 9, 10, 11
t_{PD2}	7, 8, 9, 10, 11
t_{PD3}	7, 8, 9, 10, 11
t_{CO1}	7, 8, 9, 10, 11
t_S	7, 8, 9, 10, 11
t_H	7, 8, 9, 10, 11
t_{ACO1}	7, 8, 9, 10, 11
t_{ACO1}	7, 8, 9, 10, 11
t_{AS}	7, 8, 9, 10, 11
t_{AH}	7, 8, 9, 10, 11

Document #: 38−00127−F

CY7C346
CY7C346B

128-Macrocell MAX® EPLD

Features

- **128 macrocells in 8 LABs**
- **20 dedicated inputs, 64 bidirectional I/O pins**
- **Programmable interconnect array**
- **0.8-micron double-metal CMOS EPROM technology (CY7C346)**
- **Advanced 0.65-micron CMOS technology to increase performance (CY7C346B)**
- **Available in 84-pin HLCC, PLCC, and 100-pin PGA, PQFP**

Functional Description

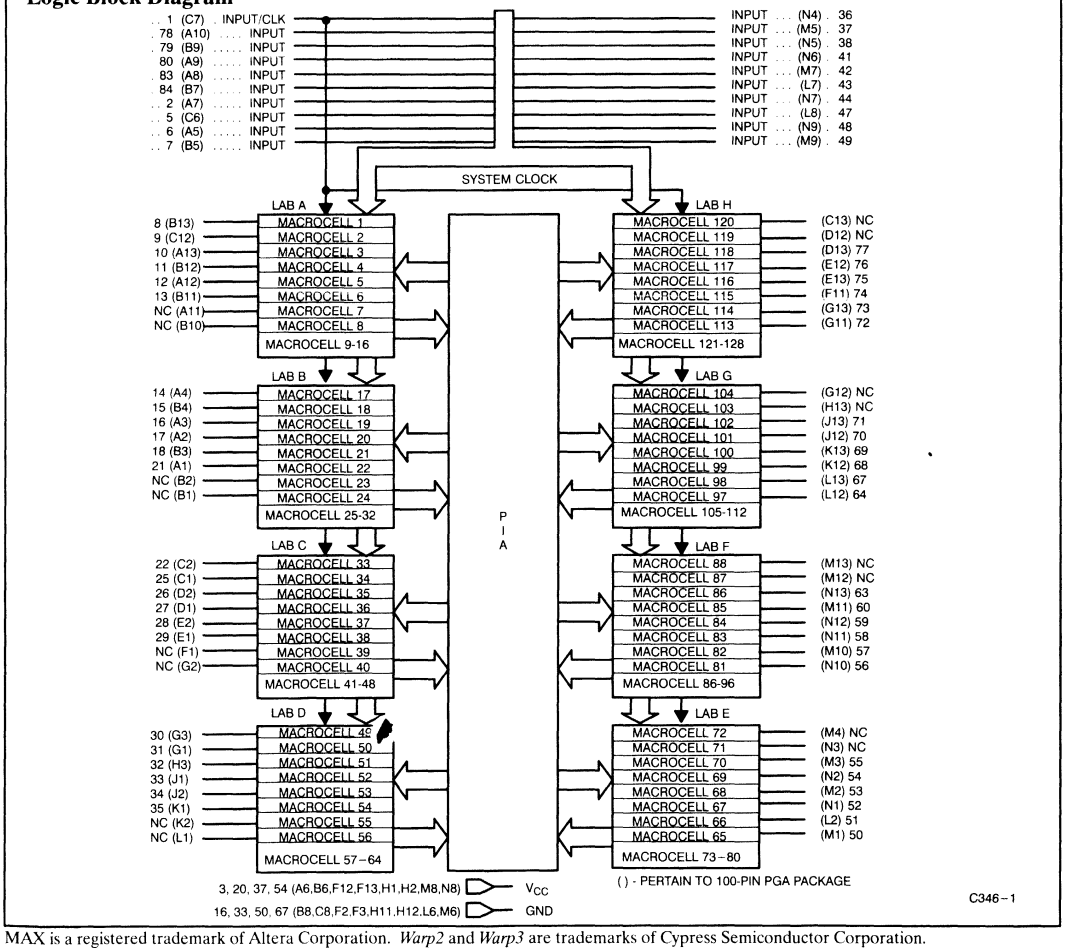
The CY7C346/CY7C346B is an Erasable Programmable Logic Device (EPLD) in which CMOS EPROM cells are used to configure logic functions within the device. The MAX architecture is 100% user configurable, allowing the devices to accommodate a variety of independent logic functions.

The 128 macrocells in the CY7C346/CY7C346B are divided into 8 Logic Array Blocks (LABs), 16 per LAB. There are 256 expander product terms, 32 per LAB, to be used and shared by the macrocells within each LAB.

Each LAB is interconnected through the programmable interconnect array, allowing all signals to be routed throughout the chip.

The speed and density of the CY7C346/CY7C346B allow it to be used in a wide range of applications, from replacement of large amounts of 7400-series TTL logic, to complex controllers and multifunction chips. With greater than 25 times the functionality of 20-pin PLDs, the CY7C346/CY7C346B allows the replacement of over 50 TTL devices. By replacing large amounts of logic, the CY7C346/CY7C346B reduces board space, part count, and increases system reliability.

Logic Block Diagram



MAX is a registered trademark of Altera Corporation. *Warp2* and *Warp3* are trademarks of Cypress Semiconductor Corporation.

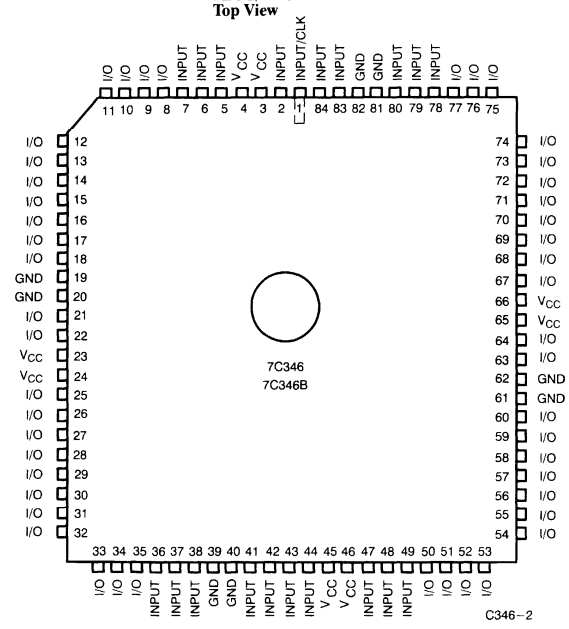
Selection Guide

		7C346B–15	7C346B–20	7C346–25 7C346B–25	7C346–30 7C346B–30	7C346–35 7C346B–35
Maximum Access Time (ns)		15	20	25	30	35
Maximum Operating Current (mA)	Commercial	250	250	250	250	250
	Military		320	325	320	320
	Industrial	320	320	320	320	320
Maximum Standby Current (mA)	Commercial	225	225	225	225	225
	Military		275	275	275	275
	Industrial	275	275	275	275	275

Shaded area contains advanced information.

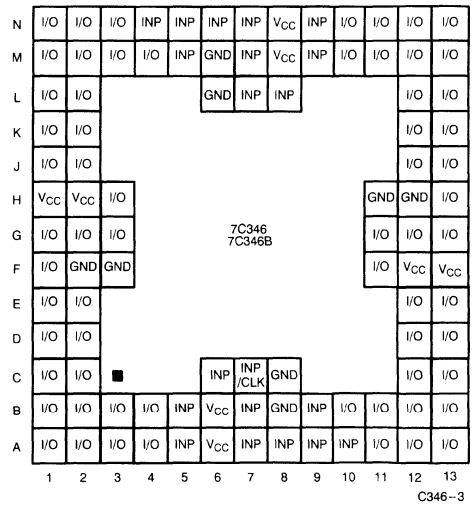
Pin Configurations

PLCC/CLCC
Top View



C346–2

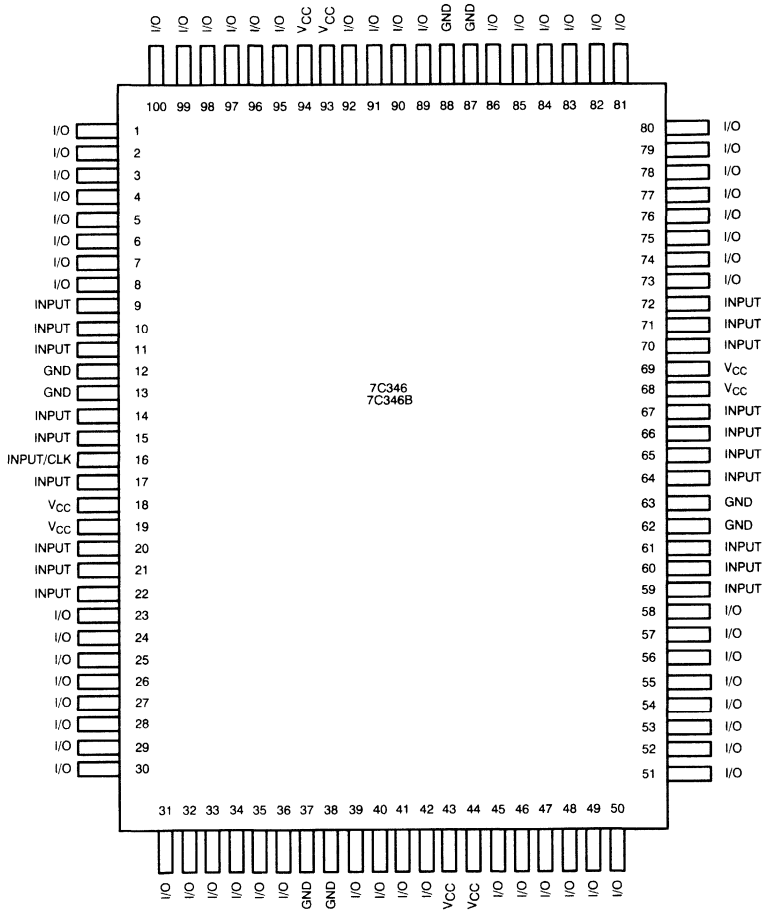
PGA
Bottom View



C346–3

Pin Configurations (continued)

PQFP
Top View



C346-4

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Maximum Junction Temperature (under bias) ..... 150°C

Supply Voltage to Ground Potential ..... −2.0V to +7.0V

Maximum Power Dissipation ..... 2500 mW

DC V_{CC} or GND Current ..... 500 mA

DC Output Current per Pin ..... −25 mA to +25 mA

DC Input Voltage[1] ..... −3.0V to + 7.0V

DC Program Voltage 13.0V

Static Discharge Voltage ..... > 1100V (per MIL−STD−883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	−40°C to +85°C	5V ± 10%
Military	−55°C to +125°C (Case)	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} +0.3	V
V_{IL}	Input LOW Voltage			−0.3	0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	μA
I_{OZ}	Output Leakage Current	V_O = V_{CC} or GND		−40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[3, 4]		−30	−90	mA
I_{CC1}	Power Supply Current (Standby)	V_I = GND (No Load)	Com'l		225	mA
			Mil/Ind		275	
I_{CC2}	Power Supply Current[5]	V_I = V_{CC} or GND (No Load) f = 1.0 MHz[4]	Com'l		250	mA
			Mil/Ind		320	
t_R	Recommended Input Rise Time				100	ns
t_F	Recommended Input Fall Time				100	ns

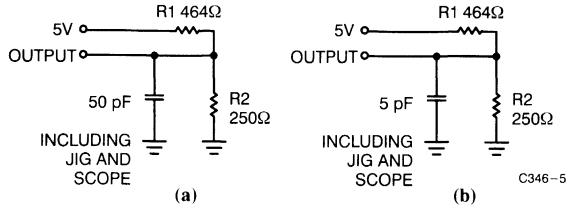
Capacitance[6]

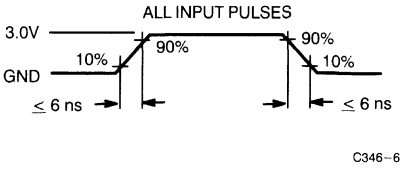
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2V, f = 1.0 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2V, f = 1.0 MHz	20	pF

Notes:

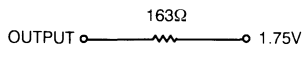
1. Minimum DC input is − 0.3V. During transitions, the inputs may undershoot to − 3.0V for periods less than 20 ns.
2. Typical values are for T_A = 25°C and V_{CC} = 5V.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. Guaranteed by design but not 100% tested.
5. This parameter is measured with device programmed as a 16-bit counter in each LAB.
6. Part (a) in AC Test Load and Waveforms is used for all parameters except t_{ER} and t_{XZ}, which is used for part (b) in AC Test Load and Waveforms. All external timing parameters are measured referenced to external pins of the device.

AC Test Loads and Waveforms[6]





Equivalent to: THÉVENIN EQUIVALENT (COMMERCIAL/MILITARY)



Logic Array Blocks

There are 8 logic array blocks in the CY7C346/CY7C346B. Each LAB consists of a macrocell array containing 16 macrocells, an expander product term array containing 32 expanders, and an I/O block. The LAB is fed by the programmable interconnect array and the dedicated input bus. All macrocell feedbacks go to the macrocell array, the expander array, and the programmable interconnect array. Expanders feed themselves and the macrocell array. All I/O feedbacks go to the programmable interconnect array so that they may be accessed by macrocells in other LABs as well as the macrocells in the LAB in which they are situated.

Externally, the CY7C346/CY7C346B provides 20 dedicated inputs, one of which may be used as a system clock. There are 64 I/O pins that may be individually configured for input, output, or bidirectional data flow.

Programmable Interconnect Array

The Programmable Interconnect Array (PIA) solves interconnect limitations by routing only the signals needed by each logic array block. The inputs to the PIA are the outputs of every macrocell within the device and the I/O pin feedback of every pin on the device.

Timing Delays

Timing delays within the CY7C346/CY7C346B may be easily determined using *Warp2*™, *Warp3*™, or MAX+PLUS® software or by the model shown in *Figure 1*. The CY7C346 /CY7C346B has fixed internal delays, allowing the user to determine the worst case timing delays for any design. For complete timing information, *Warp3* or MAX+PLUS software provides a timing simulator.

Design Recommendations

Operation of the devices described herein with conditions above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this datasheet is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect device reliability. The CY7C346/CY7C346B contains circuitry to protect device pins from high static voltages or electric fields, but normal precautions should be taken to avoid application of any voltage higher than the maximum rated voltages.

For proper operation, input and output pins must be constrained to the range GND $\leq$ (V_{IN} or V_{OUT}) $\leq V_{CC}$. Unused inputs must always be tied to an appropriate logic level (either V_{CC} or GND). Each set of V_{CC} and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 µF must be connected between V_{CC} and GND. For the most effective decoupling, each V_{CC} pin should be separately decoupled to GND directly at the device. Decoupling capacitors should have good frequency response, such as monolithic ceramic types have.

Design Security

The CY7C346/CY7C346B contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the entire device.

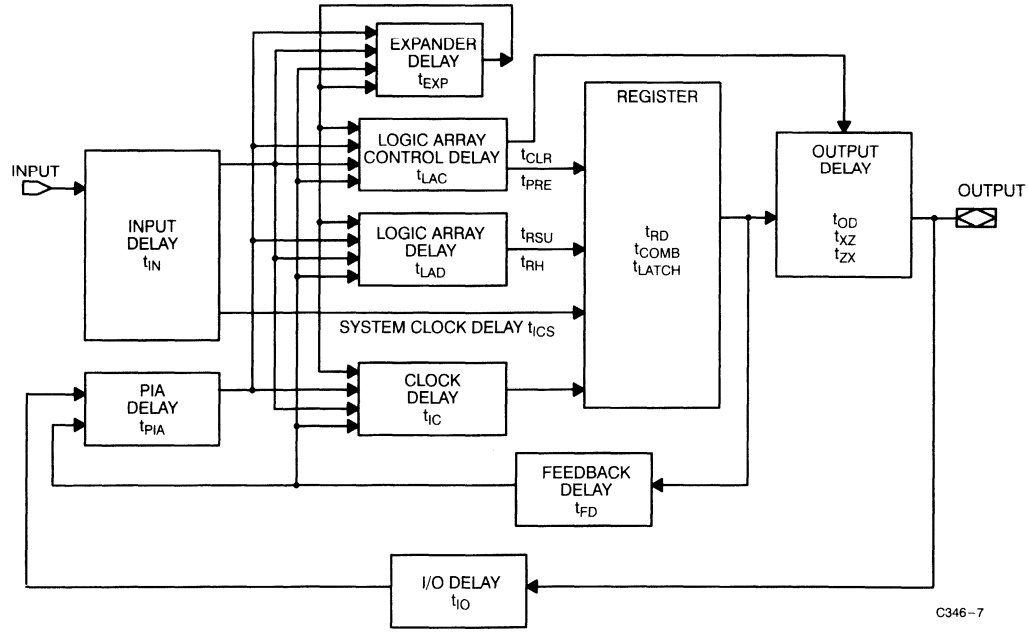
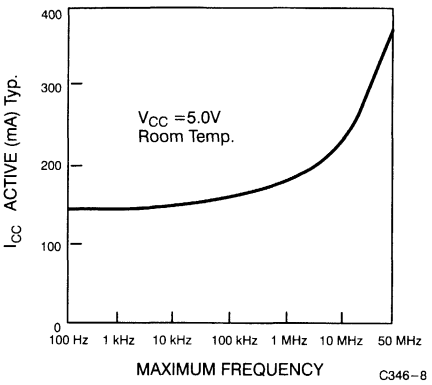


Figure 1. CY7C346/CY7C346B Internal Timing Model

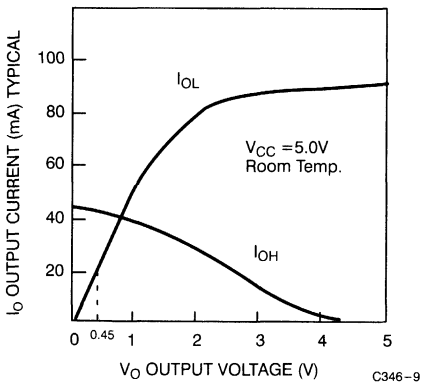
The CY7C346/CY7C346B is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

The erasable nature of these devices allows test programs to be used and erased during early stages of the production flow. The devices also contain on-board logic test circuitry to allow verification of function and AC specification once encapsulated in non-windowed packages.

Typical I_{CC} vs. f_{MAX}



Output Drive Current



Timing Considerations

Unless otherwise stated, propagation delays do not include expanders. When using expanders, add the maximum expander delay t_{EXP} to the overall delay. Similarly, there is an additional t_{PIA} delay for an input from an I/O pin when compared to a signal from straight input pin.

When calculating synchronous frequencies, use t_{S1} if all inputs are on dedicated input pins. The parameter t_{S2} should be used if data is applied at an I/O pin. If t_{S2} is greater than t_{CO1}, $1/t_{S2}$ becomes the limiting frequency in the data path mode unless $1/(t_{WH} + t_{WL})$ is less than $1/t_{S2}$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{S1}. Determine which of $1/(t_{WH} + t_{WL})$, $1/t_{CO1}$, or $1/(t_{EXP} + t_{S1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the synchronous configuration.

When calculating external asynchronous frequencies, use t_{AS1} if all inputs are on the dedicated input pins. If any data is applied to an I/O pin, t_{AS2} must be used as the required set-up time. If $(t_{AS2} + t_{AH})$ is greater than t_{ACO1}, $1/(t_{AS2} + t_{AH})$ becomes the limiting frequency in the data path mode unless $1/(t_{AWH} + t_{AWL})$ is less than $1/(t_{AS2} + t_{AH})$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{AS1}. Determine which of $1/(t_{AWH} + t_{AWL})$, $1/t_{ACO1}$, or $1/(t_{EXP} + t_{AS1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the asynchronous configuration.

The parameter t_{OH} indicates the system compatibility of this device when driving other synchronous logic with positive input hold times, which is controlled by the same synchronous clock. If t_{OH} is greater than the minimum required input hold time of the subsequent synchronous logic, then the devices are guaranteed to function properly with a common synchronous clock under worst-case environmental and supply voltage conditions.

The parameter t_{AOH} indicates the system compatibility of this device when driving subsequent registered logic with a positive hold time and using the same asynchronous clock as the CY7C346/CY7C346B.

In general, if t_{AOH} is greater than the minimum required input hold time of the subsequent logic (synchronous or asynchronous) then the devices are guaranteed to function properly under worst-case environmental and supply voltage conditions, provided the clock signal source is the same. This also applies if expander logic is used in the clock signal path of the driving device, but not for the driven device. This is due to the expander logic in the second device's clock signal path adding an additional delay (t_{EXP}) causing the output data from the preceding device to change prior to the arrival of the clock signal at the following device's register.

Commercial and Industrial External Synchronous Switching Characteristics[6] Over Operating Range

Parameter	Description	7C346B–15		7C346B–20		7C346–25 7C346B–25		7C346–30 7C346B–30		7C346–35 7C346B–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[7]		15		20		25		30		35	ns
t_{PD2}	I/O Input to Combinatorial Output Delay[8]		25		32		40		45		55	ns
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[9]		23		30		37		44		55	ns
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[4, 10]		33		42		52		59		75	ns
t_{EA}	Input to Output Enable Delay[4, 7]		15		20		25		30		35	ns
t_{ER}	Input to Output Disable Delay[4, 7]		15		20		25		30		35	ns
t_{CO1}	Synchronous Clock Input to Output Delay		7		8		14		16		20	ns
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[4, 11]		17		20		30		35		42	ns
t_{S1}	Dedicated Input or Feedback Set-Up Time to Synchronous Clock Input[7, 12]	10		13		15		20		25		ns
t_{S2}	I/O Input Set-Up Time to Synchronous Clock Input[7]	20		24		30		36		45		ns
t_H	Input Hold Time from Synchronous Clock Input[7]	0		0		0		0		0		ns
t_{WH}	Synchronous Clock Input HIGH Time	5		7		8		10		12.5		ns
t_{WL}	Synchronous Clock Input LOW Time	5		7		8		10		12.5		ns
t_{RW}	Asynchronous Clear Width[4, 7]	16		22		25		30		35		ns
t_{RR}	Asynchronous Clear Recovery Time[4,7]	16		22		25		30		35		ns
t_{RO}	Asynchronous Clear to Registered Output Delay[7]		15		20		25		30		35	ns
t_{PW}	Asynchronous Preset Width[4, 7]	15		20		25		30		35		ns
t_{PR}	Asynchronous Preset Recovery Time[4, 7]	15		20		25		30		35		ns
t_{PO}	Asynchronous Preset to Registered Output Delay[7]		15		20		25		30		35	ns
t_{CF}	Synchronous Clock to Local Feedback Input[4, 13]		3		3		3		3		6	ns
t_P	External Synchronous Clock Period ($1/(f_{MAX3})$)[4]	12		15		16		20		25		ns
f_{MAX1}	External Feedback Maximum Frequency ($1/(t_{CO1} + t_{S1})$)[4, 14]	58.8		47.6		34.5		27.7		22.2		MHz
f_{MAX2}	Internal Local Feedback Maximum Frequency, lesser of ($1/(t_{S1} + t_{CF})$) or ($1/t_{CO1}$)[4, 15]	76.9		62.5		55.5		43.4		32.2		MHz

Shaded area contains advanced information.

3

Commercial and Industrial External Synchronous Switching Characteristics[6] Over Operating Range (continued)

Parameter	Description	7C346B–15		7C346B–20		7C346–25 7C346B–25		7C346–30 7C346B–30		7C346–35 7C346B–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX3}	Data Path Maximum Frequency, lesser of $(1/(t_{WL} + t_{WH}))$, $(1/(t_{S1} + t_H))$ or $(1/t_{CO1})$[4, 16]	100		71.4		62.5		50		40		MHz
f_{MAX4}	Maximum Register Toggle Frequency $(1/(t_{WL} + t_{WH}))$[4, 17]	100		71.4		62.5		50		40		MHz
t_{OH}	Output Data Stable Time from Synchronous Clock Input[4, 18]	3		3		3		3		3		ns

Shaded area contains advanced information.

Notes:

7. This specification is a measure of the delay from input signal applied to a dedicated input (68-pin PLCC input pin 1, 2, 32, 34, 35, 66, or 68) to combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function.
   When this note is applied to any parameter specification it indicates that the signal (data, asynchronous clock, asynchronous clear, and/or asynchronous preset) is applied to a dedicated input only and no signal path (either clock or data) employs expander logic.
   If an input signal is applied to an I/O pin an additional delay equal to t_{PIA} should be added to the comparable delay for a dedicated input. If expanders are used, add the maximum expander delay t_{EXP} to the overall delay for the comparable delay without expanders.
8. This specification is a measure of the delay from input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.
9. This specification is a measure of the delay from an input signal applied to a dedicated input (68-pin PLCC input pin 1, 2, 32, 34, 35, 36, 66, or 68) to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic.
10. This specification is a measure of the delay from an input signal applied to an I/O macrocell pin to any output. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
11. This specification is a measure of the delay from synchronous register clock to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used, register is synchronously clocked and all feedback is within the same LAB. This parameter is tested periodically by sampling production material.
12. If data is applied to an I/O input for capture by a macrocell register, the I/O pin input set-up time minimums should be observed. These parameters are t_{S2} for synchronous operation and t_{AS2} for asynchronous operation.
13. This specification is a measure of the delay associated with the internal register feedback path. This is the delay from synchronous clock to LAB logic array input. This delay plus the register set-up time, t_{S1}, is the minimum internal period for an internal synchronous state machine configuration. This delay is for feedback within the same LAB. This parameter is tested periodically by sampling production material.
14. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which a state machine configuration with external feedback can operate. It is assumed that all data inputs and external feedback signals are applied to dedicated inputs.
15. This specification indicates the guaranteed maximum frequency at which a state machine with internal-only feedback can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{CO1}$. All feedback is assumed to be local originating within the same LAB.
16. This frequency indicates the maximum frequency at which the device may operate in data path mode (dedicated input pin to output pin). This assumes data input signals are applied to dedicated input pins and no expander logic is used. If any of the data inputs are I/O pins, t_{S2} is the appropriate t_S for calculation.
17. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which an individual output or buried register can be cycled by a clock signal applied to the dedicated clock input pin.
18. This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.

Commercial and Industrial External Asynchronous Switching Characteristics[6] Over Operating Range

Parameter	Description	7C346B–15		7C346B–20		7C346–25 7C346B–25		7C346–30 7C346B–30		7C346–35 7C346B–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACO1}	Asynchronous Clock Input to Output Delay[7]		15		20		25		30		35	ns
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output[19]		25		32		39		46		55	ns
t_{AS1}	Dedicated Input or Feedback Set-Up Time to Asynchronous Clock Input[7]	5		5		5		6		8		ns
t_{AS2}	I/O Input Set-Up Time to Asynchronous Clock Input[7]	14.5		17		19		22		28		ns
t_{AH}	Input Hold Time from Asynchronous Clock Input[7]	5		6		6		8		10		ns
t_{AWH}	Asynchronous Clock Input HIGH Time[7]	9		10		11		14		16		ns
t_{AWL}	Asynchronous Clock Input LOW Time[7, 20]	7		8		9		11		14		ns
t_{ACF}	Asynchronous Clock to Local Feedback Input[4, 21]		11		13		15		18		22	ns
t_{AP}	External Asynchronous Clock Period ($1/(f_{MAXA4})$)[4]	16		18		20		25		30		ns
f_{MAXA1}	External Feedback Maximum Frequency in Asynchronous Mode ($1/(t_{ACO1} + t_{AS1})$)[4, 22]	50		40		33.3		27.7		23.2		MHz
f_{MAXA2}	Maximum Internal Asynchronous Frequency[4, 23]	62.5		55.5		50		40		33.3		MHz
f_{MAXA3}	Data Path Maximum Frequency in Asynchronous Mode [4, 24]	66.6		50		40		33.3		28.5		MHz
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[4, 25]	62.5		55.5		50		40		33.3		MHz
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[4, 26]	12		12		15		15		15		ns

Shaded area contains advanced information.

Notes:

19. This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used in the logic of combinatorial output or the asynchronous clock input. The clock signal is applied to the dedicated clock input pin and all feedback is within a single LAB. This parameter is tested periodically by sampling production material.
20. This parameter is measured with a positive-edge triggered clock at the register. For negative edge triggering, the t_{AWH} and t_{AWL} parameters must be swapped. If a given input is used to clock multiple registers with both positive and negative polarity, t_{AWH} should be used for both t_{AWH} and t_{AWL}.
21. This specification is a measure of the delay associated with the internal register feedback path for an asynchronous clock to LAB logic array input. This delay plus the asynchronous register set-up time, t_{AS1}, is the minimum internal period for an internal asynchronously clocked state machine configuration. This delay is for feedback within the same LAB, assumes no expander logic in the clock path, and assumes that the clock input signal is applied to a dedicated input pin. This parameter is tested periodically by sampling production material.
22. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that all data inputs, clock inputs, and feedback signals are applied to dedicated inputs and that no expander logic is employed in the clock signal path or data path.
23. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal-only feedback can operate. This parameter is determined by the lesser of $(1/(t_{ACF} + t_{AS1}))$ or $(1/(t_{AWH} + t_{AWL}))$. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO1}$.
    This specification assumes no expander logic is utilized, all data inputs and clock inputs are applied to dedicated inputs, and all state feedback is within a single LAB. This parameter is tested periodically by sampling production material.
24. This frequency is the maximum frequency at which the device may operate in the asynchronously clocked data path mode. This specification is determined by the lesser of $1/(t_{AWH} + t_{AWL})$, $1/(t_{AS1} + t_{AH})$ or $1/t_{ACO1}$. It assumes data and clock input signals are applied to dedicated input pins and no expander logic is used.
25. This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to an external dedicated input pin.
26. This parameter indicates the minimum time that the previous register output data is maintained on the output after an asynchronous register clock input applied to an external dedicated input pin.

Commercial and Industrial Internal Switching Characteristics Over Operating Range

Parameter	Description	7C346B–15		7C346B–20		7C346–25 7C346B–25		7C346–30 7C346B–30		7C346–35 7C346B–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay		3		4		5		7		9	ns
t_{IO}	I/O Input Pad and Buffer Delay		3		4		6		6		9	ns
t_{EXP}	Expander Array Delay		8		10		12		14		20	ns
t_{LAD}	Logic Array Data Delay		8		10		12		14		16	ns
t_{LAC}	Logic Array Control Delay		5		7		10		12		13	ns
t_{OD}	Output Buffer and Pad Delay		3		3		5		5		6	ns
t_{ZX}	Output Buffer Enable Delay[27]		5		5		10		11		13	ns
t_{XZ}	Output Buffer Disable Delay		5		5		10		11		13	ns
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	4		5		6		8		10		ns
t_{RH}	Register Hold Time Relative to Clock Signal at Register	4		5		6		8		10		ns
t_{LATCH}	Flow Through Latch Delay		1		2		3		4		4	ns
t_{RD}	Register Delay		1		1		1		2		2	ns
t_{COMB}	Transparent Mode Delay[28]		1		2		3		4		4	ns
t_{CH}	Clock HIGH Time	4		6		8		10		12.5		ns
t_{CL}	Clock LOW Time	4		6		8		10		12.5		ns
t_{IC}	Asynchronous Clock Logic Delay		6		8		14		16		18	ns
t_{ICS}	Synchronous Clock Delay		0.5		0.5		1		1		1	ns
t_{FD}	Feedback Delay		1		1		1		1		2	ns
t_{PRE}	Asynchronous Register Preset Time		3		3		5		6		7	ns
t_{CLR}	Asynchronous Register Clear Time		3		3		5		6		7	ns
t_{PCW}	Asynchronous Preset and Clear Pulse Width	3		4		5		6		7		ns
t_{PCR}	Asynchronous Preset and Clear Recovery Time	3		4		5		6		7		ns
t_{PIA}	Programmable Interconnect Array Delay Time		10		12		14		16		20	ns

Shaded area contains advanced information.

Notes:

27. Sample tested only for an output change of 500 mV.
28. This specification guarantees the maximum combinatorial delay associated with the macrocell register bypass when the macrocell is configured for combinatorial operation.

Military External Synchronous Switching Characteristics[6] Over Operating Range

Parameter	Description	7C346B–20		7C346B–25		7C346–30 7C346B–30		7C346–35 7C346B–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[7]		20		25		30		35	ns
t_{PD2}	I/O Input to Combinatorial Output Delay[8]		32		39		45		55	ns
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[9]		30		37		44		55	ns
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[4, 10]		42		51		59		75	ns
t_{EA}	Input to Output Enable Delay[4, 7]		20		25		30		35	ns
t_{ER}	Input to Output Disable Delay[4, 7]		20		25		30		35	ns
t_{CO1}	Synchronous Clock Input to Output Delay		8		14		16		20	ns
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[4, 11]		20		30		35		42	ns
t_{S1}	Dedicated Input or Feedback Set-Up Time to Synchronous Clock Input[7, 12]	13		15		20		25		ns
t_{S2}	I/O Input Set-Up Time to Synchronous Clock Input[7]	24		29		36		45		ns
t_H	Input Hold Time from Synchronous Clock Input[7]	0		0		0		0		ns
t_{WH}	Synchronous Clock Input HIGH Time	7		8		10		12.5		ns
t_{WL}	Synchronous Clock Input LOW Time	7		8		10		12.5		ns
t_{RW}	Asynchronous Clear Width[4,7]	20		25		30		35		ns
t_{RR}	Asynchronous Clear Recovery Time[4,7]	20		25		30		35		ns
t_{RO}	Asynchronous Clear to Registered Output Delay[7]		20		25		30		35	ns
t_{PW}	Asynchronous Preset Width[4, 7]	20		25		30		35		ns
t_{PR}	Asynchronous Preset Recovery Time[4, 7]	20		25		30		35		ns
t_{PO}	Asynchronous Preset to Registered Output Delay[7]		20		25		30		35	ns
t_{CF}	Synchronous Clock to Local Feedback Input[4, 13]		3		3		3		6	ns
t_P	External Synchronous Clock Period ($1/(f_{MAX3})$)[4]	14		16		20		25		ns
f_{MAX1}	External Feedback Maximum Frequency ($1/(t_{CO1} + t_{S1})$)[4, 14]	47.6		34.5		27.7		22.2		MHz

Shaded area contains advanced information.

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Military External Synchronous Switching Characteristics[6] Over Operating Range (continued)

Parameter	Description	7C346B–20		7C346B–25		7C346–30 7C346B–30		7C346–35 7C346B–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX2}	Internal Local Feedback Maximum Frequency, lesser of $(1/(t_{S1} + t_{CF}))$ or $(1/t_{CO1})$[4, 15]	62.5		55.5		43.4		32.2		MHz
f_{MAX3}	Data Path Maximum Frequency, lesser of $(1/(t_{WL} + t_{WH}))$, $(1/(t_{S1} + t_H))$ or $(1/t_{CO1})$[4, 16]	71.4		62.5		50		40		MHz
f_{MAX4}	Maximum Register Toggle Frequency $(1/(t_{WL} + t_{WH}))$[4, 17]	71.4		62.5		50		40		MHz
t_{OH}	Output Data Stable Time from Synchronous Clock Input[4, 18]	3		3		3		3		ns

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Military External Asynchronous Switching Characteristics[6] Over Operating Range

Parameter	Description	7C346B–20		7C346B–25		7C346–30 7C346B–30		7C346–35 7C346B–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACO1}	Asynchronous Clock Input to Output Delay[7]		20		25		30		35	ns
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output[19]		32		39		46		55	ns
t_{AS1}	Dedicated Input or Feedback Set-Up Time to Asynchronous Clock Input[7]	6		5		6		8		ns
t_{AS2}	I/O Input Set-Up Time to Asynchronous Clock Input[7]	17		19		22		28		ns
t_{AH}	Input Hold Time from Asynchronous Clock Input[7]	6		6		8		10		ns
t_{AWH}	Asynchronous Clock Input HIGH Time[7]	10		11		14		16		ns
t_{AWL}	Asynchronous Clock Input LOW Time[7, 20]	8		9		11		14		ns
t_{ACF}	Asynchronous Clock to Local Feedback Input[4, 21]		13		15		18		22	ns
t_{AP}	External Asynchronous Clock Period $(1/(f_{MAXA4}))$[4]	18		20		25		30		ns
f_{MAXA1}	External Feedback Maximum Frequency in Asynchronous Mode $(1/(t_{ACO1} + t_{AS1}))$[4, 22]	40		33.3		27.7		23.2		MHz
f_{MAXA2}	Maximum Internal Asynchronous Frequency[4, 23]	55.5		50		40		33.3		MHz
f_{MAXA3}	Data Path Maximum Frequency in Asynchronous Mode[4, 24]	50		40		33.3		28.5		MHz
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[4, 25]	55.5		50		40		33.3		MHz
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[4, 26]	12		15		15		15		ns

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Military Typical Internal Switching Characteristics Over Operating Range

Parameter	Description	7C346B–20		7C346B–25		7C346–30 7C346B–30		7C346–35 7C346B–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay		4		5		7		9	ns
t_{IO}	I/O Input Pad and Buffer Delay		4		6		6		9	ns
t_{EXP}	Expander Array Delay		10		12		14		20	ns
t_{LAD}	Logic Array Data Delay		10		12		14		16	ns
t_{LAC}	Logic Array Control Delay		7		10		12		13	ns
t_{OD}	Output Buffer and Pad Delay		3		5		5		6	ns
t_{ZX}	Output Buffer Enable Delay[27]		5		10		11		13	ns
t_{XZ}	Output Buffer Disable Delay		5		10		11		13	ns
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	5		6		8		10		ns
t_{RH}	Register Hold Time Relative to Clock Signal at Register	5		6		8		10		ns
t_{LATCH}	Flow Through Latch Delay		2		3		4		4	ns
t_{RD}	Register Delay		1		1		2		2	ns
t_{COMB}	Transparent Mode Delay[28]		2		3		4		4	ns
t_{CH}	Clock HIGH Time	6		8		10		12.5		ns
t_{CL}	Clock LOW Time	6		8		10		12.5		ns
t_{IC}	Asynchronous Clock Logic Delay		8		14		16		18	ns
t_{ICS}	Synchronous Clock Delay		0.5		2		2		3	ns
t_{FD}	Feedback Delay		1		1		1		2	ns
t_{PRE}	Asynchronous Register Preset Time		3		5		6		7	ns
t_{CLR}	Asynchronous Register Clear Time		3		5		6		7	ns
t_{PCW}	Asynchronous Preset and Clear Pulse Width	4		5		6		7		ns
t_{PCR}	Asynchronous Preset and Clear Recovery Time	4		5		6		7		ns
t_{PIA}	Programmable Interconnect Array Delay Time		12		14		16		20	ns

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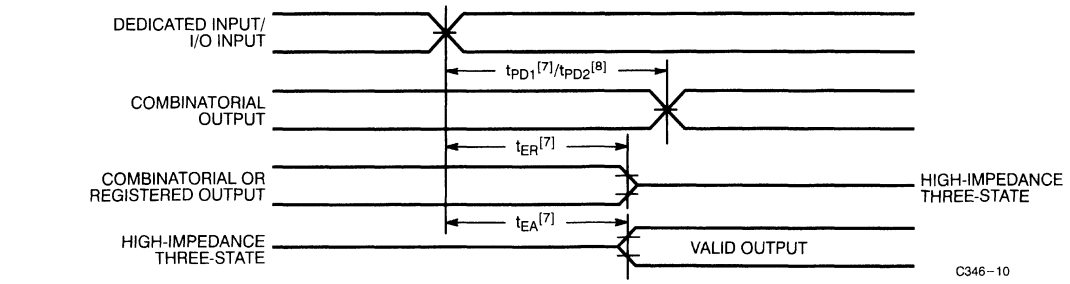
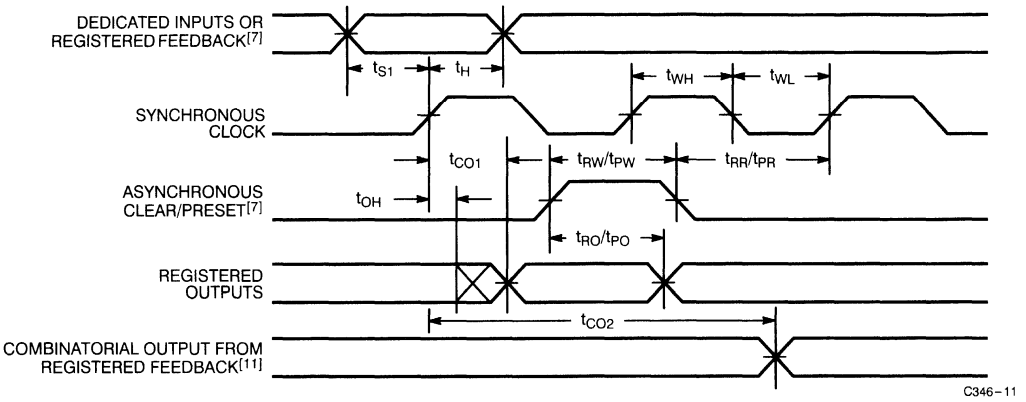
3

Switching Waveforms

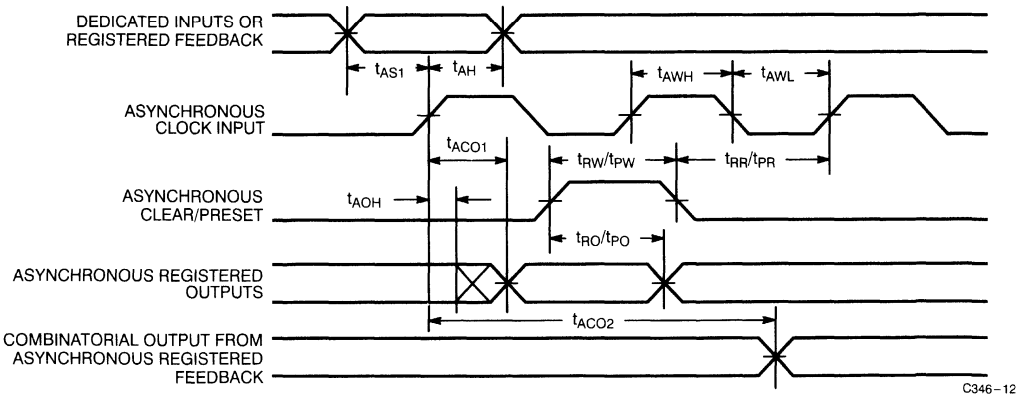
External Combinatorial



External Synchronous

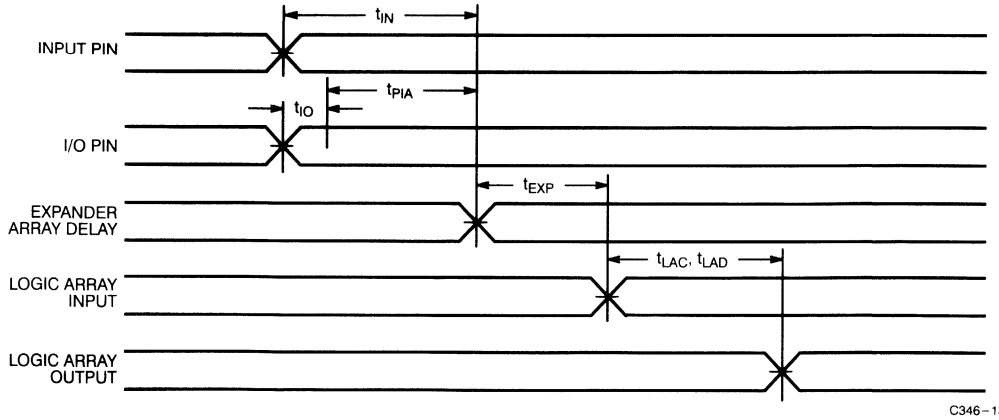


External Asynchronous

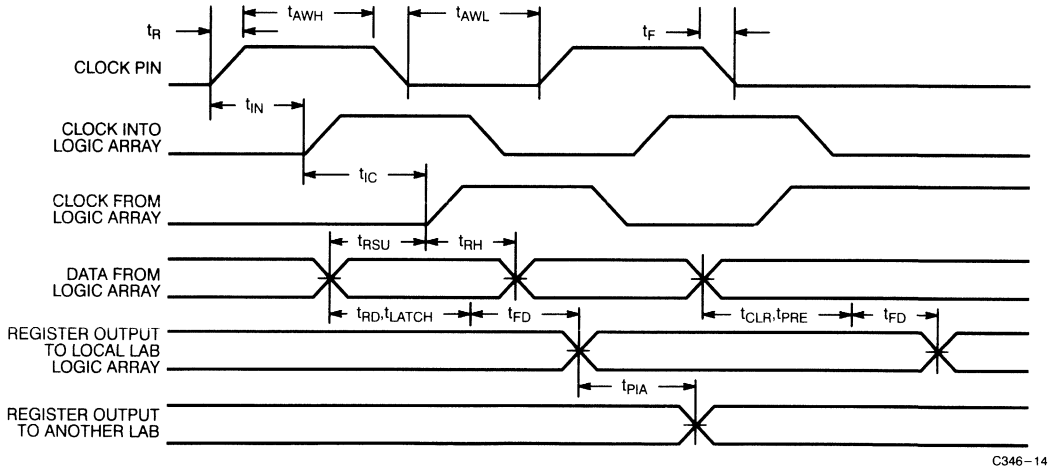


Switching Waveforms (continued)

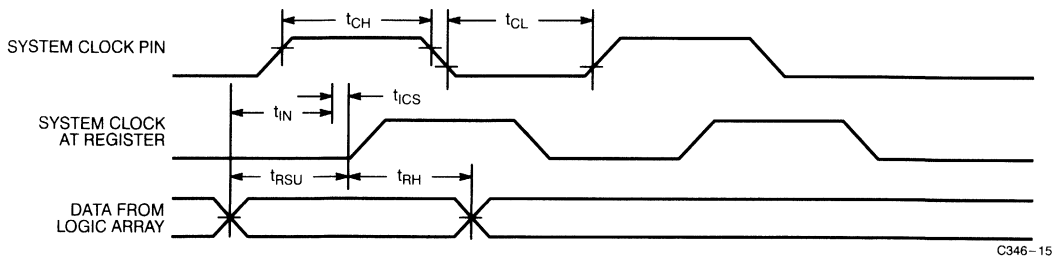
Internal Combinatorial



Internal Asynchronous

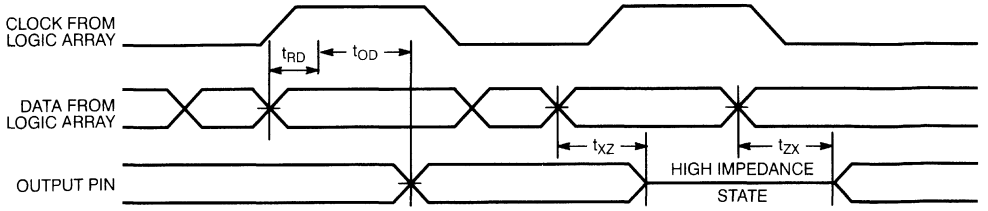


Internal Synchronous



Switching Waveforms (continued)

Internal Synchronous



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C346B–15HC/HI	H84	84-Pin Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C346B–15JC/JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C346B–15NC/NI	N100	100-Lead Plastic Quad Flatpack	
	CY7C346B–15RC/RI	R100	100-Pin Windowed Ceramic Pin Grid Array	
20	CY7C346B–20HC/HI	H84	84-Pin Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C346B–20JC/JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C346B–20NC/NI	N100	100-Lead Plastic Quad Flatpack	
	CY7C346B–20RC/RI	R100	100-Pin Windowed Ceramic Pin Grid Array	
	CY7C346B–20HMB	H84	84-Pin Windowed Leaded Chip Carrier	Military
	CY7C346B–20RMB	R100	100-Pin Windowed Ceramic Pin Grid Array	
25	CY7C346–25HC/HI	H84	84-Pin Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C346–25JC/JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C346–25NC/NI	N100	100-Lead Plastic Quad Flatpack	
	CY7C346–25RC/RI	R100	100-Pin Windowed Ceramic Pin Grid Array	
	CY7C346B–25HC/HI	H84	84-Pin Windowed Leaded Chip Carrier	
	CY7C346B–25JC/JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C346B–25NC/NI	N100	100-Lead Plastic Quad Flatpack	
	CY7C346B–25RC/RI	R100	100-Pin Windowed Ceramic Pin Grid Array	
	CY7C346B–25HMB	H84	84-Pin Windowed Leaded Chip Carrier	Military
	CY7C346B–25RMB	R100	100-Pin Windowed Ceramic Pin Grid Array	
30	CY7C346–30HC/HI	H84	84-Pin Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C346–30JC/JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C346–30NC/NI	N100	100-Lead Plastic Quad Flatpack	
	CY7C346–30RC/RI	R100	100-Pin Windowed Ceramic Pin Grid Array	
	CY7C346B–30HC/HI	H84	84-Pin Windowed Leaded Chip Carrier	
	CY7C346B–30JC/JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C346B–30NC/NI	N100	100-Lead Plastic Quad Flatpack	
	CY7C346B–30RC/RI	R100	100-Pin Windowed Ceramic Pin Grid Array	
	CY7C346–30HMB	H84	84-Pin Windowed Leaded Chip Carrier	Military
	CY7C346–30RMB	R100	100-Pin Windowed Ceramic Pin Grid Array	
	CY7C346B–30HMB	H84	84-Pin Windowed Leaded Chip Carrier	
	CY7C346B–30RMB	R100	100-Pin Windowed Ceramic Pin Grid Array	
35	CY7C346–35HC/HI	H84	84-Pin Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C346–35JC/JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C346–35NC/NI	N100	100-Lead Plastic Quad Flatpack	
	CY7C346–35RC/RI	R100	100-Pin Windowed Ceramic Pin Grid Array	
	CY7C346B–35HC/HI	H84	84-Pin Windowed Leaded Chip Carrier	
	CY7C346B–35JC/JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C346B–35NC/NI	N100	100-Lead Plastic Quad Flatpack	
	CY7C346B–35RC/RI	R100	100-Pin Windowed Ceramic Pin Grid Array	
	CY7C346–35HMB	H84	84-Pin Windowed Leaded Chip Carrier	Military
	CY7C346–35RMB	R100	100-Pin Windowed Ceramic Pin Grid Array	
	CY7C346B–35HMB	H84	84-Pin Windowed Leaded Chip Carrier	
	CY7C346B–35RMB	R100	100-Pin Windowed Ceramic Pin Grid Array	

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MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD1}	7, 8, 9, 10, 11
t_{PD2}	7, 8, 9, 10, 11
t_{PD3}	7, 8, 9, 10, 11
t_{CO1}	7, 8, 9, 10, 11
t_{S1}	7, 8, 9, 10, 11
t_{S2}	7, 8, 9, 10, 11
t_{H}	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{WL}	7, 8, 9, 10, 11
t_{RO}	7, 8, 9, 10, 11
t_{PO}	7, 8, 9, 10, 11
t_{ACO1}	7, 8, 9, 10, 11
t_{ACO2}	7, 8, 9, 10, 11
t_{AS1}	7, 8, 9, 10, 11
t_{AH}	7, 8, 9, 10, 11
t_{AWH}	7, 8, 9, 10, 11
t_{AWL}	7, 8, 9, 10, 11

Document #: 38-00244-B

This is an abbreviated datasheet. Contact a Cypress representative for complete specifications. For new designs, please refer to the FLASH370 family

CY7C361

Ultra High Speed State Machine EPLD

Features

- **High speed: 125-MHz state machine output generation**
  - **Token passing**
  - **Multiple, concurrent processes**
  - **Multiway branch or join**
- **One clock with programmable clock doubler**
- **Programmable miser bits for power savings**
- **8 to 12 inputs with input macrocells**
  - **Metastability hardened: 10-year MBTF**
  - **0, 1, or 2 input registers**
  - **3 programmable clock enables**
- **32 synchronous state macrocells**
- **10 to 14 outputs**
  - **Skew-controlled OR output array**
  - **Outputs are sum of states like PLA**
- **Security fuse**
- **Available in 28-pin slimline DIP and 28-pin HLCC**
- **UV-erasable and reprogrammable**
- **Programming and operation 100% testable**

Product Characteristics

The CY7C361 is a CMOS erasable, programmable logic device (EPLD) with very high speed sequencing capabilities.

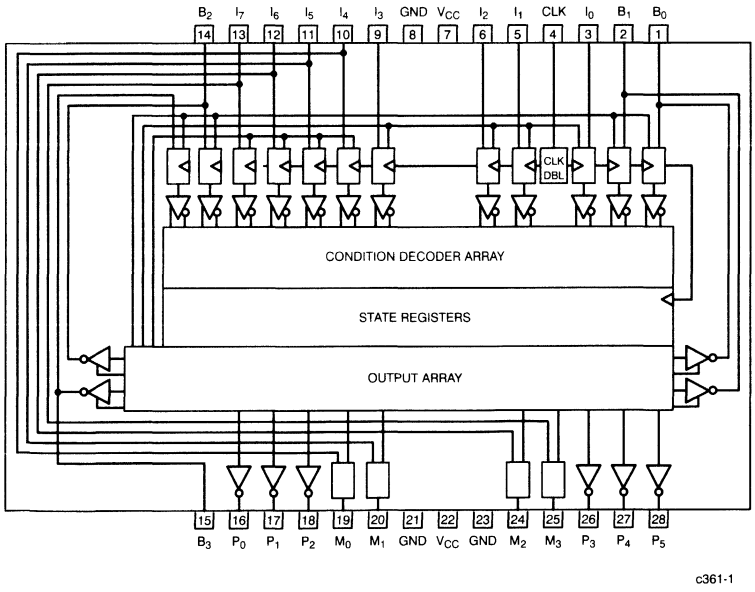
Applications include high-speed cache and I/O subsystems control, control of high-speed numeric processors, and high-speed arbitration between synchronous or asynchronous systems.

A programmable on-board clock doubler allows the device to operate at 125 MHz internally based on a 62.5-MHz input clock reference. The clock doubler is not a phase-locked loop. It produces an internal pulse on each edge of the external clock. The length of each internal pulse is determined by the intrinsic delays within the CY7C361. When the doubler is enabled, all macrocells in the CY7C361 are referenced to the doubled clock. If the clock doubler is disabled, a 125-MHz input clock can be connected to pin 4, and it will be used as a clock to all macrocells.

The CY7C361 has two arrays, similar to those in a PLA except that the registers are placed between the two arrays so that the long feedback path of the PLA is eliminated.

3

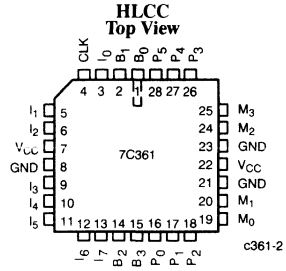
Logic Block Diagram



c361-1

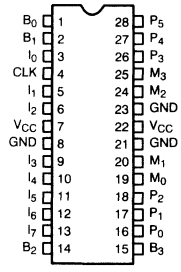
Pin Configurations

HLCC
Top View



c361-2

DIP
Top View



c361-3

Selection Guide

Generic Part Number	I_{CC} mA at f_{MAX}		f_{MAX} MHz		t_{IS} ns		t_{CO} ns	
	Com	Mil	Com	Mil	Com	Mil	Com	Mil
CY7C361-125	200		125		2		15	
CY7C361-100	200	200	100	100	3	3	19	19
CY7C361-83			83.3	83.3	5	5	23	23

Document #: 38-00106-D

FLASH370™ PRELIMINARY CPLD Family

High-Density Flash CPLDs

Features

- **Flash erasable CMOS CPLDs**
- **High density**
  - **32–256 macrocells**
  - **32–192 I/O pins**
  - **Multiple clock pins**
- **High speed**
  - **t_{PD} = 8.5 – 15 ns**
  - **t_S = 5 – 10 ns**
  - **t_{CO} = 6 – 10 ns**
- **Fast Programmable Interconnect Matrix (PIM)**
  - **Uniform predictable delay, independent of routing**
- **Intelligent product term allocator**
  - **0–16 product terms to any macrocell**
  - **Provides product term steering on an individual basis**
  - **Provides product term sharing among local macrocells**
  - **Prevents stealing of neighboring product terms**
- **Simple timing model**
  - **No fanout delays**
  - **No expander delays**
  - **No dedicated vs. I/O pin delays**
  - **No additional delay through PIM**
  - **No penalty for using full 16 product terms**
  - **No delay for steering or sharing product terms**
- **Flexible clocking**
  - **2–4 clock pins per device**
  - **Clock polarity control**
- **Security bit and user ID supported**
- **Packages**
  - **44–288 pins**
  - **PLCC, CLCC, PGA, and TQFP packages**
- ***Warp2*™**
  - **Low-cost, text-based design tool, PLD compiler**
  - **IEEE 1076-compliant VHDL**
  - **Available on PC and Sun platforms**
- ***Warp3*™ CAE development system**
  - **VHDL input**
  - **ViewLogic graphical user interface**
  - **Schematic capture (ViewDraw™)**
  - **VHDL simulation (ViewSim™)**
  - **Available on PC and Sun platforms**

General Description

The FLASH370 family of CMOS CPLDs provides a range of high-density programmable logic solutions with unparalleled performance. Each member of the family is designed with Cypress's state-of-the-art 0.65-micron Flash technology. All of the devices are electrically erasable and reprogrammable, simplifying product inventory and reducing costs.

The FLASH370 family is designed to bring the flexibility, ease of use and performance of the 22V10 to high-density CPLDs. The architecture is based on a number of logic blocks that are connected by a Programmable Interconnect Matrix (PIM). Each logic block features its own product term array, product term allocator array, and 16 macrocells. The PIM distributes signals from one logic block to another as well as all inputs from pins.

The family features a wide variety of densities and pin counts to choose from. At each density there are two packaging options to choose from—one that is I/O intensive and another that is register intensive. For example, the CY7C374 and CY7C375 both feature 128 macrocells. On the CY7C374 half of the macrocells are buried and the device is available in 84-pin packages. On the CY7C375 all of the macrocells are fed to I/O pins and the device is available in 160-pin packages. *Figure 1* shows a block diagram of the CY7C374/5.

Functional Description

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) consists of a completely global routing matrix for signals from I/O pins and feedbacks from the logic blocks. The PIM is an extremely robust interconnect that avoids fitting and density limitations. Routing is automatically accomplished by software and the propagation delay through the PIM is transparent to the user. Signals from any pin or any logic block can be routed to any or all logic blocks.

The inputs to the PIM consist of all I/O and dedicated input pins and all macrocell feedbacks from within the logic blocks. The number of PIM inputs increases with pincount and the number of logic blocks. The outputs from the PIM are signals routed to the appropriate logic block(s). Each logic block receives 36 inputs from the PIM and their complements, allowing for 32-bit operations to be implemented in a single pass through the device. The wide number of inputs to the logic block also improves the routing capacity of the FLASH370 family.

An important feature of the PIM involves timing. The propagation delay through the PIM is accounted for in the timing specifications for each device. There is no additional delay for traveling through the PIM. In fact, all inputs travel through the PIM. Likewise, there are no route-dependent timing parameters on the FLASH370 devices. The worst-case PIM delays are incorporated in all appropriate FLASH370 specifications.

FLASH370 Selection Guide

Device	Pins	Macrocells	Dedicated Inputs	I/O Pins	Flip-Flops	Speed (ns)	Speed (MHz)
371	44	32	6	32	44	8.5	143
372	44	64	6	32	76	10	125
373	84	64	6	64	76	10	125
374	84	128	6	64	140	12	100
375	160	128	6	128	140	12	100
376	160	192	6	128	204	15	83
377	240	192	6	192	204	15	83
378	160	256	6	128	268	15	83
379	240	256	6	192	268	15	83

Shaded area contains advanced information.

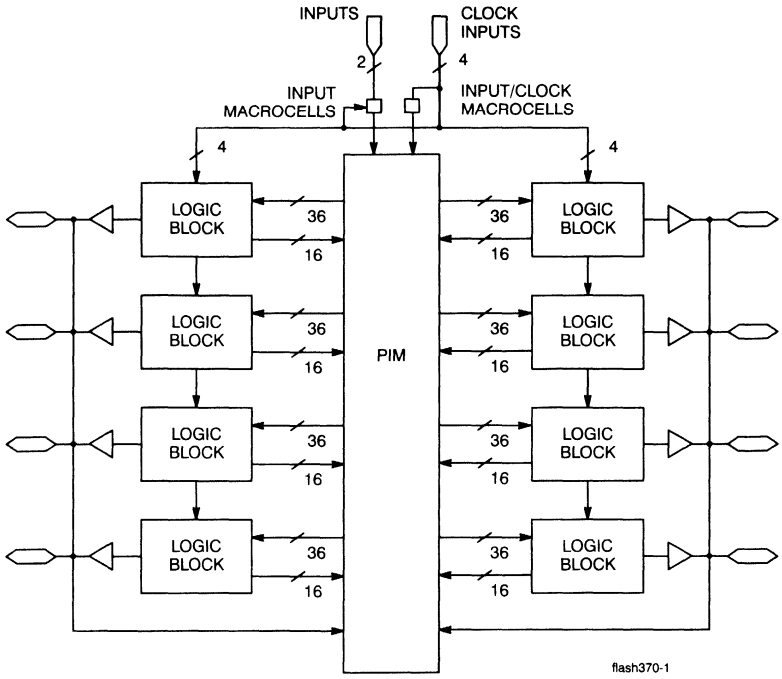


Figure 1. CY7C374/5 Block Diagram

Functional Description (continued)

Routing signals through the PIM is completely invisible to the user. All routing is accomplished 100% by software—no hand routing is necessary. *Warp2* and third-party development packages automatically route designs for the FLASH370 family in a matter of minutes. Finally, the rich routing resources of the FLASH370 family accommodate last minute logic changes while maintaining fixed pin assignments.

Logic Block

The logic block is the basic building block of the FLASH370 architecture. It consists of a product term array, an intelligent product-term allocator, 16 macrocells, and a number of I/O cells. The number of I/O cells varies depending on the device used.

There are two types of logic blocks in the FLASH370 family. The first type features an equal number (16) of I/O cells and macrocells and is shown in *Figure 2*. This architecture is best for I/O-intensive applications. The second type of logic block features a buried macrocell along with each I/O macrocell. In other words, in each logic block, there are eight macrocells that are connected to I/O cells and eight macrocells that are internally fed back to the PIM only. This organization is designed for register-intensive applications and is displayed in *Figure 3*. Note that at each FLASH370 density (except the smallest), an I/O intensive and a register-intensive device is available.

Product Term Array

Each logic block features a 72 x 86 programmable product term array. This array is fed with 36 inputs from the PIM, which originate from macrocell feedbacks and device pins. Active LOW and active HIGH versions of each of these inputs are generated to create the full 72-input field. The 86 product terms in the array can be created from any of the 72 inputs.

Of the 86 product terms, 80 are for general-purpose use for the 16 macrocells in the logic block. Four of the remaining six product terms in the logic block are output enable (OE) product terms. Each of the OE product terms control up to 8 of the 16 macrocells and are selectable on an individual macrocell basis. In other words, each I/O cell can select between one of two OE product terms to control the output buffer. The first two of these four OE product terms are available to the upper half of the I/O macrocells in a logic block. The other two OE product terms are available to the lower half of the I/O macrocells in a logic block. The final two product terms in each logic block are dedicated asynchronous set and asynchronous reset product terms.

Product Term Allocator

Through the product term allocator, software automatically distributes product terms among the 16 macrocells in the logic block as needed. A total of 80 product terms are available from the local product term array. The product term allocator provides two important capabilities without affecting performance: product term steering and product term sharing.

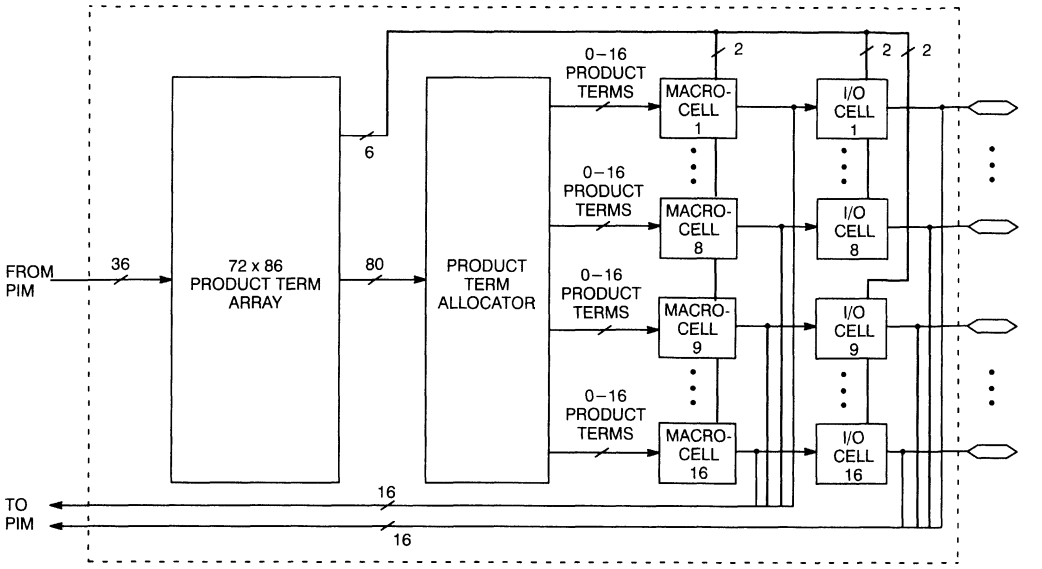


Figure 2. Logic Block for CY7C371, CY7C373, CY7C375, CY7C377, and CY7C379 (I/O Intensive)

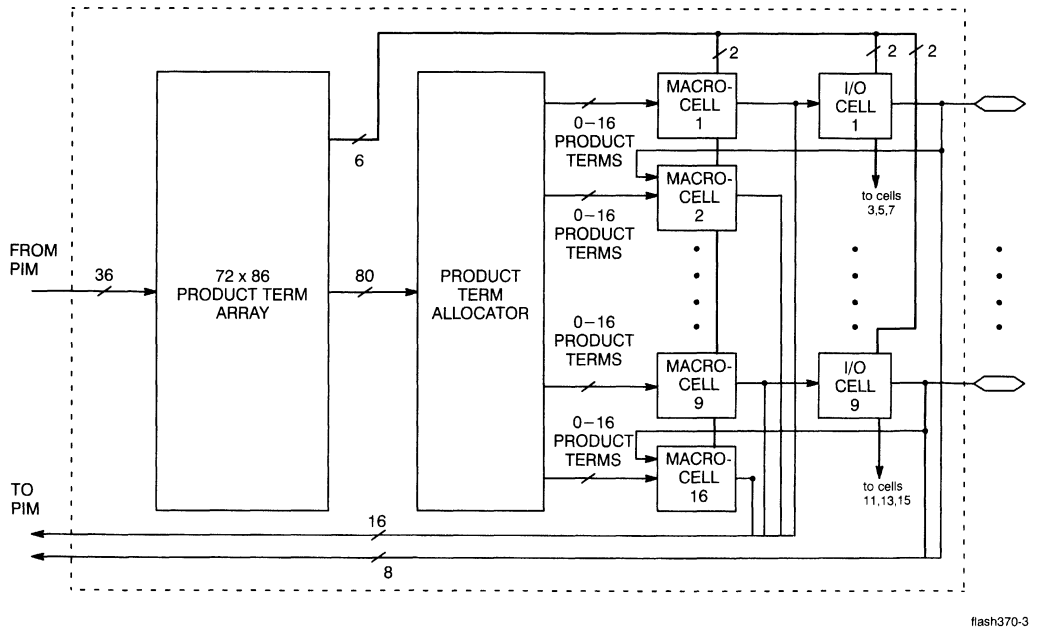


Figure 3. Logic Block for CY7C372, CY7C374, CY7C376, and CY7C378 (Register Intensive)

Product Term Steering

Product term steering is the process of assigning product terms to macrocells as needed. For example, if one macrocell requires ten product terms while another needs just three, the product term allocator will "steer" ten product terms to one macrocell and three to the other. On FLASH370 devices, product terms are steered on an individual basis. Any number between 0 and 16 product terms can be steered to any macrocell. Note that 0 product terms is useful in cases where a particular macrocell is unused or used as an input register.

Product Term Sharing

Product term sharing is the process of using the same product term among multiple macrocells. For example, if more than one output has one or more product terms in its equation that are common to other outputs, those product terms are only programmed once. The FLASH370 product term allocator allows sharing across groups of four output macrocells in a variable fashion. The software automatically takes advantage of this capability—the user does not have to intervene. Note that greater usable density can often be achieved if the user "floats" the pin assignment. This allows the compiler to group macrocells that have common product terms adjacently.

Note that neither product term sharing nor product term steering have any effect on the speed of the product. All worst-case steering and sharing configurations have been incorporated in the timing specifications for the FLASH370 devices.

FLASH370Macrocell

I/O Macrocell

Within each logic block there are 8 or 16 I/O macrocells depending on the device used. *Figure 4* illustrates the architecture of the I/O macrocell. The macrocell features a register that can be configured as combinatorial, a D flip-flop, a T flip-flop, or a level-triggered latch.

The register can be asynchronously set or asynchronously reset at the logic block level with the separate set and reset product terms. Each of these product terms features programmable polarity. This allows the registers to be set or reset based on an AND expression or an OR expression.

Clocking of the register is very flexible. Depending on the device, either two or four global synchronous clocks are available to clock the register. Furthermore, each clock features programmable polarity so that registers can be triggered on falling as well as rising edges (see the Dedicated/Clock Inputs section). Clock polarity is chosen at the logic block level.

At the output of the macrocell, a polarity control mux is available to select active LOW or active HIGH signals. This has the added advantage of allowing significant logic reduction to occur in many applications.

The FLASH370 macrocell features a feedback path to the PIM separate from the I/O pin input path. This means that if the macrocell is buried (fed back internally only), the associated I/O pin can still be used as an input.

Buried Macrocell

Some of the devices in the FLASH370 family feature additional macrocells that do not feed individual I/O pins. *Figure 5* displays the architecture of the I/O and buried macrocells for these devices. The I/O macrocell is identical to the one on devices without buried macrocells.

The buried macrocell is very similar to the I/O macrocell. Again, it includes a register that can be configured as combinatorial, a D flip-flop, a T flip-flop, or a latch. The clock for this register has the same options as described for the I/O macrocell. The primary difference between the I/O macrocell and the buried macrocell is that the buried macrocell does not have the ability to output data directly to an I/O pin.

One additional difference on the buried macrocell is the addition of input register capability. The buried macrocell can be configured to act as an input register (D-type or latch) whose input comes from the I/O pin associated with the neighboring macrocell. The output of all buried macrocells is sent directly to the PIM regardless of its configuration.

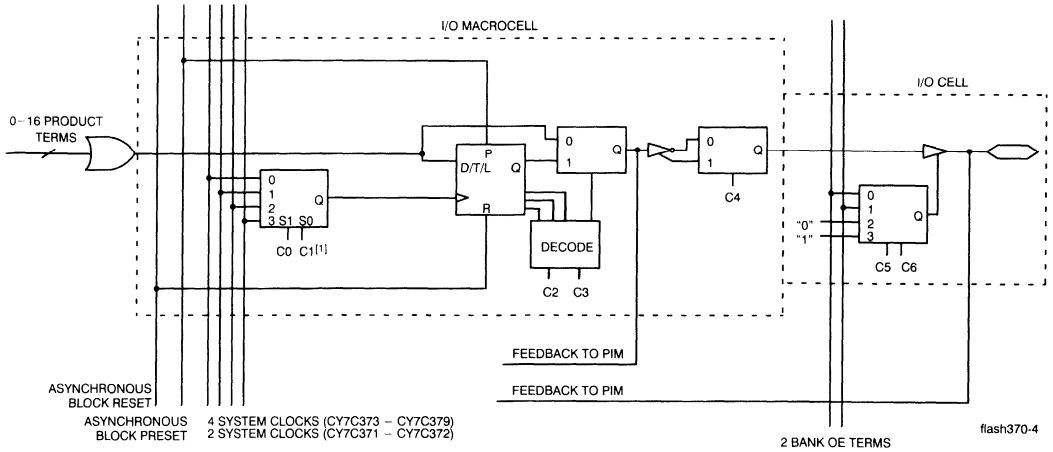


Figure 4. I/O Macrocell

Note:

1. C1 is not used on the CY7C371 and CY7C372 since the mux size is 2:1

FLASH370 I/O Cell

The I/O cell on the FLASH370 devices is illustrated along with the I/O macrocell in *Figures 4* and *5*. The user can program the I/O cell to change the way the three-state output buffer is enabled and/or disabled. Each output can be set permanently on (output only), permanently off (input only), or dynamically controlled by one of two OE product terms.

Dedicated/Clock Inputs

Six pins on each member of the FLASH370 family are designated as input-only. There are two types of dedicated inputs on FLASH370 devices: input pins and input/clock pins. *Figure 6* illustrates the ar-

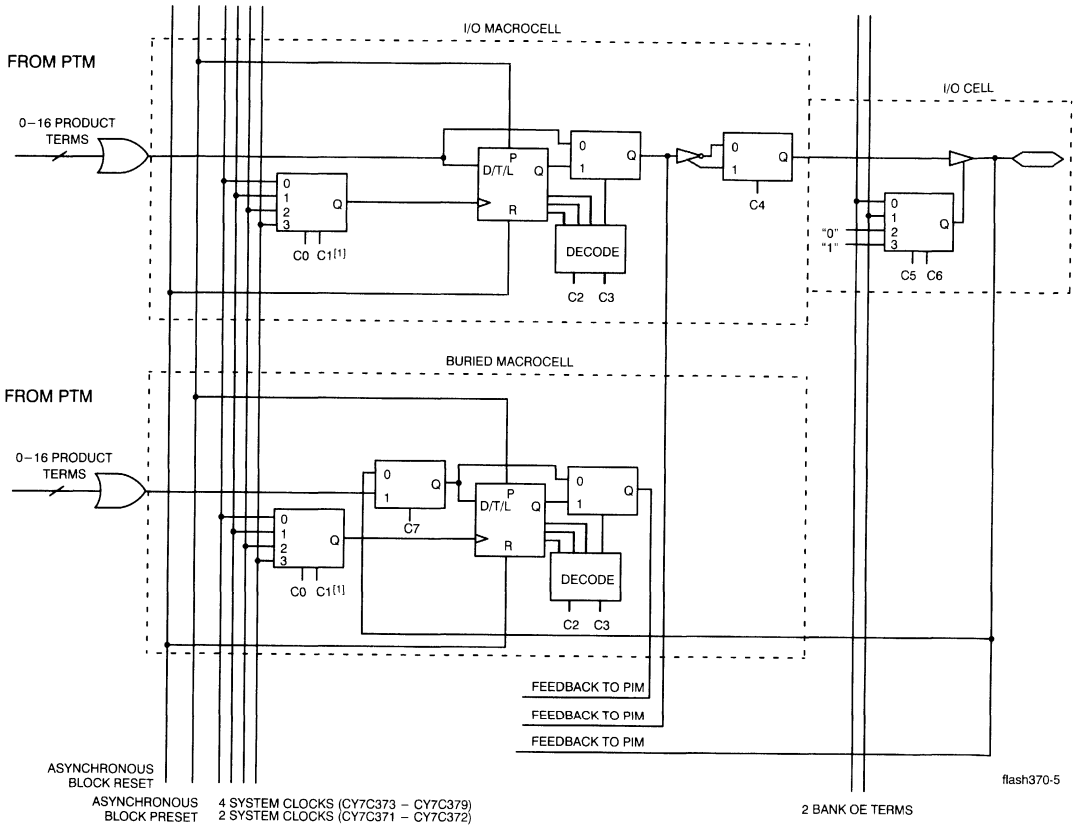


Figure 5. I/O and Buried Macrocells

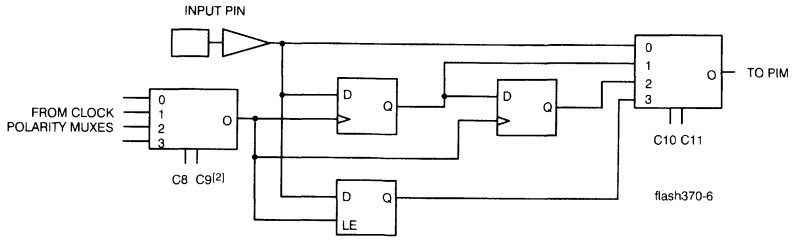


Figure 6. Input Pins

Note:

2. C9 is not used on the CY7C371 and CY7C372 since the mux size is 2:1.

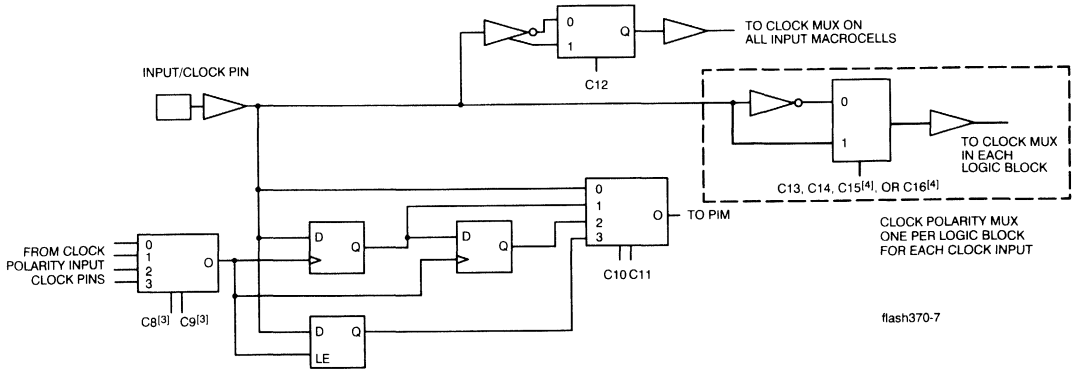


Figure 7. Input/Clock Pins

Notes:
3. C8 and C9 are not included on the CY7C371 and CY7C372 since each input/clock pin has the other input/clock pin as its clock.
4. C15 and C16 are not used on the CY7C371 and CY7C372 since there are two clocks.

chitecture for input pins. Four input options are available for the user: combinatorial, registered, double-registered, or latched. If a registered or latched option is selected, any one of the input clocks can be selected for control.

Figure 7 illustrates the architecture of input/clock pins. There are either two or four input/clock pins available, depending on the device selected. (The CY7C371 and CY7C372 have two input/clock pins while the other devices have four input/clock pins.) Like the input pins, input/clock pins can be combinatorial, registered, double registered, or latched. In addition, these pins feed the clocking structures throughout the device. The clock path at the input is user-configurable in polarity. The polarity of the clock signal can also be controlled by the user. Note that this polarity is separately controlled for input registers and output registers.

Timing Model

One of the most important features of the FLASH370 family is the simplicity of its timing. All delays are worst case and system performance is unaffected by the features used or not used on the parts. *Figure 8* illustrates the true timing model for the 8.5-ns devices. For combinatorial paths, any input to any output incurs an 8.5-ns worst-case delay regardless of the amount of logic used. For synchronous systems, the input set-up time to the output macrocells for any input is 5.0 ns and the clock to output time is also 6.0 ns.

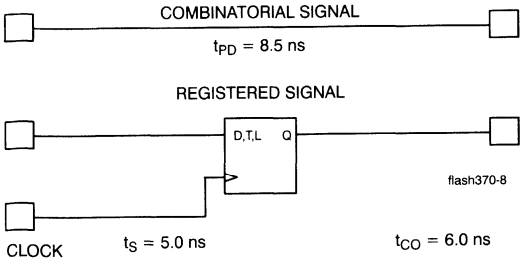


Figure 8. Timing Model for CY7C371

Again, these measurements are for any output and clock, regardless of the logic used.

Stated another way, the FLASH370 features:

- no fanout delays
- no expander delays
- no dedicated vs. I/O pin delays
- no additional delay through PIM
- no penalty for using 0–16 product terms
- no added delay for steering product terms
- no added delay for sharing product terms
- no routing delays
- no output bypass delays

The simple timing model of the FLASH370 family eliminates unexpected performance penalties.

Development Software Support

Warp2

Warp2 is a state-of-the-art VHDL compiler for designing with Cypress PLDs and PROMs. *Warp2* utilizes a proper subset of IEEE 1076 VHDL as its Hardware Description Language (HDL) for design entry. VHDL provides a number of significant benefits for the design entry. VHDL provides a number of significant benefits for the design engineer. *Warp2* accepts VHDL input, synthesizes and optimizes the entered design, and outputs a JEDEC map for the desired device. For simulation, *Warp2* provides the graphical waveform simulator called Nova.

VHDL (VHSIC Hardware Description Language) is an open, powerful, non-proprietary language that is a standard for behavioral design entry and simulation. It is already mandated for use by the Department of Defense and supported by every major vendor of CAE tools. VHDL allows designers to learn a single language that is useful for all facets of the design process.

Warp3

Warp3 is a sophisticated design tool that is based on the latest version of ViewLogic's CAE design environment. *Warp3* features schematic capture (ViewDraw), VHDL waveform simulation (ViewSim), a VHDL debugger, and VHDL synthesis, all inte-

grated in a graphical design environment. *Warp3* is available on PCs using Windows® 3.1 or subsequent versions and on Sun workstations.

Third-Party Software

Cypress maintains a very strong commitment to third-party design software vendors. All major third-party software vendors (including ABEL™, LOG/iC™, CUPL™, and Minc) will provide support for the FLASH370 family of devices. To expedite this support, Cypress supplies vendors with all pertinent architectural information as well as design fitters for our products.

Document #: 38-00215-B

Programming

The QuickPro II™ and *Impulse3*™ device programmers from Cypress will program all Cypress PLDs, CPLDs, and PROMs. Both units are standalone programmers that connect to any IBM-compatible PC via the printer port.

Third-Party Programmers

As with development software, Cypress strongly supports third-party programmers. All major third-party programmers (including Data I/O, Logical Devices, Minato, SMS, and Stag) will support the FLASH370 family.

32-Macrocell Flash CPLD

Features

- **32 macrocells in two logic blocks**
- **32 I/O pins**
- **6 dedicated inputs including 2 clock pins**
- **No hidden delays**
- **High speed**
  - **f_{MAX} = 143 MHz**
  - **t_{PD} = 8.5 ns**
  - **t_S = 5 ns**
  - **t_{CO} = 6 ns**
- **Electrically alterable FLASH technology**
- **Available in 44-pin PLCC and CLCC packages**
- **Pin compatible with the CY7C372**

Functional Description

The CY7C371 is a Flash erasable Complex Programmable Logic Device (CPLD) and is part of the FLASH370™ family of high-density, high-speed CPLDs. Like all members of the FLASH370 family, the CY7C371 is designed to bring the ease of use and high performance of the 22V10 to high-density CPLDs.

The 32 macrocells in the CY7C371 are divided between two logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

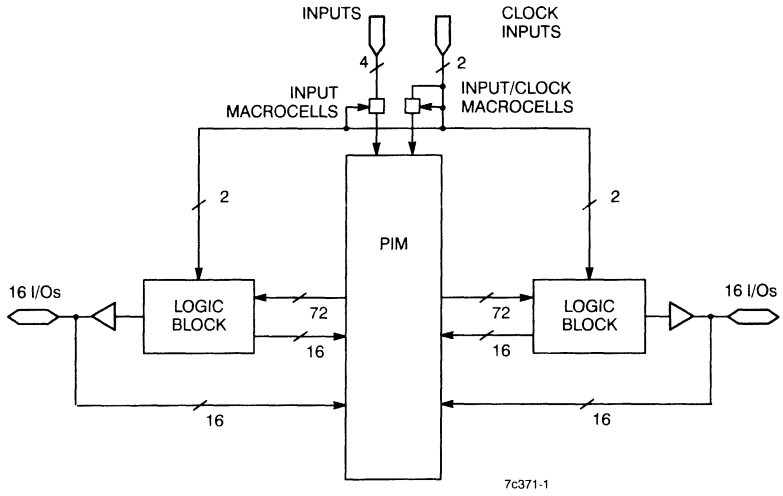
The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370 family, the CY7C371 is rich in I/O resources. Each macrocell in the device features an associated I/O pin, resulting in 32 I/O pins on the CY7C371. In addition, there are four dedicated inputs and two input/clock pins.

Finally, the CY7C371 features a very simple timing model. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C371 remain the same.

3

Logic Block Diagram

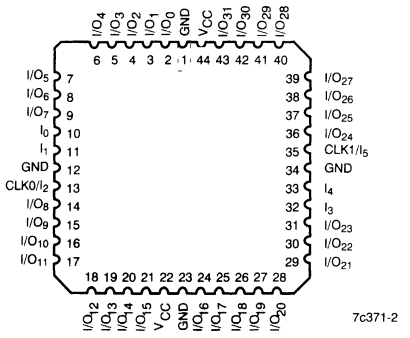


Selection Guide

		7C371–143	7C371–110	7C371–83	7C371–66
Maximum Propagation Delay, t_{PD} (ns)		8.5	10	12	15
Maximum Operating Current, I_{CC2} (mA) Conditions	Commercial	240	180	180	180
	Military			230	230
Maximum Standby Current, I_{CC1} (mA) Conditions	Commercial	220	175	175	175
	Military			220	220

Shaded area contains advanced information.

Pin Configuration



Logic Block

The number of logic blocks distinguishes the members of the FLASH370 family. The CY7C371 includes two logic blocks. Each logic block is constructed of a product term array, a product term allocator, and 16 macrocells.

Product Term Array

The product term array in the FLASH370 logic block includes 36 inputs from the PIM and outputs 86 product terms to the product term allocator. The 36 inputs from the PIM are available in both positive and negative polarity, making the overall array size 72 x 86. This large array in each logic block allows for very complex functions to be implemented in a single pass through the device.

Product Term Allocator

The product term allocator is a dynamic, configurable resource that shifts product terms to macrocells that require them. Any number of product terms between 0 and 16 inclusive can be assigned to any of the logic block macrocells (this is called product term steering). Furthermore, product terms can be shared among multiple macrocells. This means that product terms that are common to more than one output can be implemented in a single product term. Product term steering and product term sharing help to increase the effective density of the FLASH370 CPLDs. Note that product term allocation is handled by software and is invisible to the user.

I/O Macrocell

Each of the macrocells on the CY7C371 has a separate associated I/O pin. The input to the macrocell is the sum of between 0 and 16 product terms from the product term allocator. The macrocell includes a register that can be optionally bypassed. It also has polarity control, and two global clocks to trigger the register. The macrocell also features a separate feedback path to the PIM so that the register can be buried if the I/O pin is used as an input.

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) connects the two logic blocks on the CY7C371 to the inputs and to each other. All inputs (including feedbacks) travel through the PIM. There is no speed penalty incurred by signals traversing the PIM.

Design Tools

Development software for the CY7C371 is available from Cypress's *Warp2*™ and *Warp3*™ software packages. Both of these products are based on the IEEE-standard VHDL language. Cypress also actively supports third-party design tools such as ABEL™, CUPL™, MINC, and LOG/iC™. Please see the Third Party Tools datasheet for further information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Program Voltage 12.5V

Output Current into Outputs (LOW) ..... 16 mA

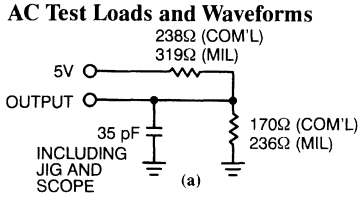
Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

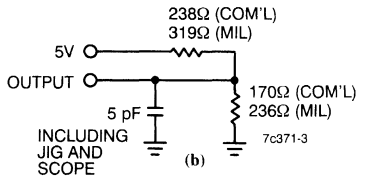
Latch-Up Current ..... >200 mA

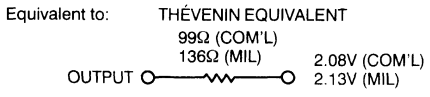
Operating Range

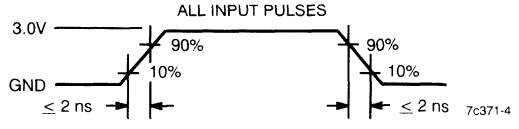
Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Military[1]	−55°C to +125°C	5V ± 10%
Industrial	−40°C to 85°C	5V ± 10%

AC Test Loads and Waveforms









Electrical Characteristics Over the Operating Range[2]

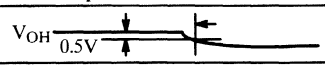
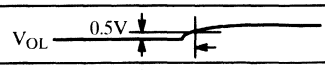
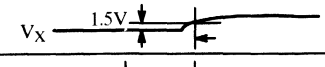
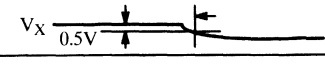
Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = −3.2 mA (Com'l/Ind)		2.4		V
			I_{OH} = −2.0 mA (Mil)				V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 16 mA (Com'l/Ind)			0.5	V
			I_{OL} = 12 mA (Mil)				V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all inputs[3]			2.0	7.0	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all inputs[3]			−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			−50	+50	μA
I_{OS}	Output Short Circuit Current[4, 5]	V_{CC} = Max., V_{OUT} = 0.5V			−30	−90	mA
I_{CC1}	Power Supply Current (Standby)	V_{CC} = Max., I_{OUT} = 0 mA, f = 0 mHz, V_{IN} = GND, V_{CC}[6]		Com'l		175	mA
				Mil		220	
I_{CC2}	Power Supply Current[5]	V_I = V_{CC} or GND, f = 1 MHz[6]		Com'l		180	mA
				Mil		230	

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V at f=1 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V at f = 1 MHz	12	pF

Endurance Characteristics[5]

Parameter	Description	Test Conditions	Min.	Max.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions	100		Cycles

Parameter	V_X	Output Waveform—Measurement Level
$t_{ER(-)}$	1.5V	
$t_{ER(+)}$	2.6V	
$t_{EA(+)}$	0V	
$t_{EA(-)}$	V_{thc}	

(a) Test Waveforms

Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
5. Tested initially and after any design or process changes that may affect these parameters.
6. Measured with loadable, 16-bit up/down counter programmed into each logic block.

Switching Characteristics Over the Operating Range[7]

Parameter	Description	7C371-143		7C371-110		7C371-83		7C371-66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters										
t_{PD}	Input to Combinatorial Output		8.5		10		12		15	ns
t_{PDL}	Input to Output Through Transparent Input or Output Latch		11.5		13		18		22	ns
t_{PDLL}	Input to Output Through Transparent Input and Output Latches		13.5		15		20		24	ns
t_{EA}	Input to Output Enable		13		14		19		24	ns
t_{ER}	Input to Output Disable		13		14		19		24	ns
Input Registered/Latched Mode Parameters										
t_{WL}	Clock or Latch Enable Input LOW Time[5]	2.5		3		5		6		ns
t_{WH}	Clock or Latch Enable Input HIGH Time[5]	2.5		3		5		6		ns
t_{IS}	Input Register or Latch Set-Up Time	2		2		3		4		ns
t_{IH}	Input Register or Latch Hold Time	2		2		3		4		ns
t_{ICO}	Input Register Clock or Latch Enable to Combinatorial Output		12.5		14		19		24	ns
t_{ICOL}	Input Register Clock or Latch Enable to Output Through Transparent Output Latch		14.5		16		21		26	ns
Output Registered/Latched Mode Parameters										
t_{CO}	Clock or Latch Enable to Output		6		6.5		10		12	ns
t_S	Set-Up Time from Input to Clock or Latch Enable	5		6		10		12		ns
t_H	Register or Latch Data Hold Time	0		0		0		0		ns
t_{CO2}	Output Clock or Latch Enable to Output Delay (Through Memory Array)		12		14		19		24	ns
t_{SCS}	Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array)	7		9		12		15		ns
t_{SCS2}	Output Clock Through Array to Output Clock (2-Pass Delay)[5]	13		16.5		21		27		ns
t_{SL}	Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch Enable	9		10		12		15		ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Clock or Latch Enable	0		0		0		0		ns
f_{MAX1}	Maximum Frequency with Internal Feedback (Least of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[5]	143		111		83.3		66.6		MHz
f_{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)[5]	166.7		153.8		100		83.3		MHz
f_{MAX3}	Maximum Frequency with external feedback (Lesser of $1/(t_{CO} + t_S)$ and $1/(t_{WL} + t_{WH})$)[5]	91		80		50		41.6		MHz
$t_{OH} - t_{IH}$ 37x	Output Data Stable from Output clock Minus Input Register Hold Time for 7C37x[5, 8]	0		0		0		0		ns
Pipelined Mode Parameters										
t_{ICS}	Input Register Clock to Output Register Clock	7		9		12		15		ns
f_{MAX4}	Maximum Frequency in Pipelined Mode (Least of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)	125		111		76.9		62.5		MHz

Shaded area contains advanced information.

Note:

7. All AC parameters are measured with 16 outputs switching.
8. This specification is intended to guarantee interface compatibility of the other members of the FLASH370 family with the CY7C371. This specification is met for the devices operating at the same ambient temperature and at the same power supply voltage.

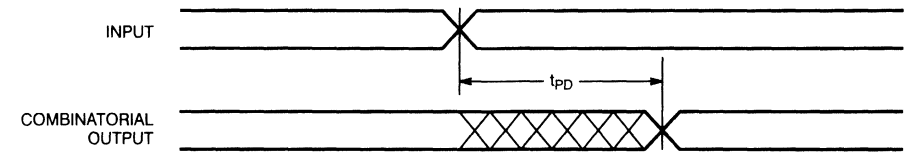
Switching Characteristics Over the Operating Range[7] (continued)

Parameter	Description	7C371–143		7C371–110		7C371–83		7C371–66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Preset Parameters										
t_{RW}	Asynchronous Reset Width[5]	8		10		15		20		ns
t_{RR}	Asynchronous Reset Recovery Time[5]	10		12		17		22		ns
t_{RO}	Asynchronous Reset to Output		14		16		21		26	ns
t_{PW}	Asynchronous Preset Width[5]	8		10		15		20		ns
t_{PR}	Asynchronous Preset Recovery Time[5]	10		12		17		22		ns
t_{PO}	Asynchronous Preset to Output		14		16		21		26	ns
t_{POR}	Power-On Reset[5]		1		1		1		1	µs

Shaded area contains advanced information.

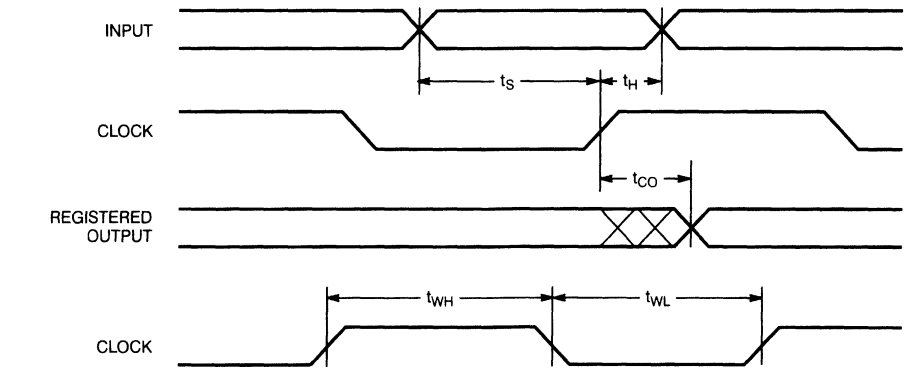
Switching Waveforms

Combinatorial Output



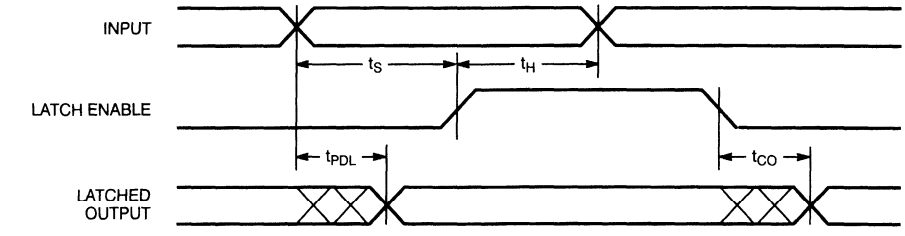
7c371-9

Registered Output



7c371-10

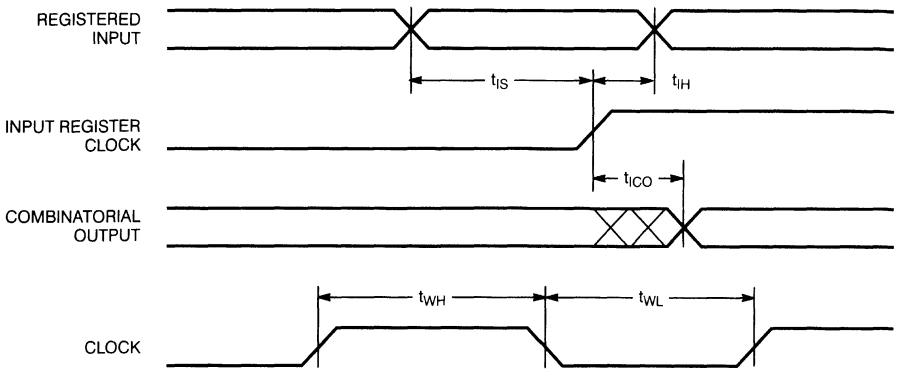
Latched Output



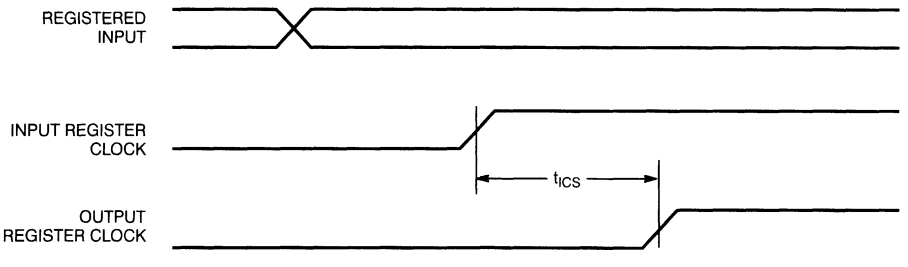
7c371-11

Switching Waveforms (continued)

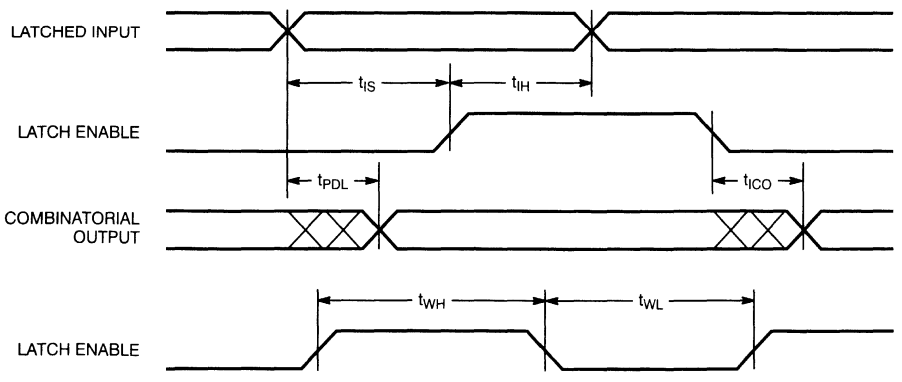
Registered Input



Input Clock to Output Clock

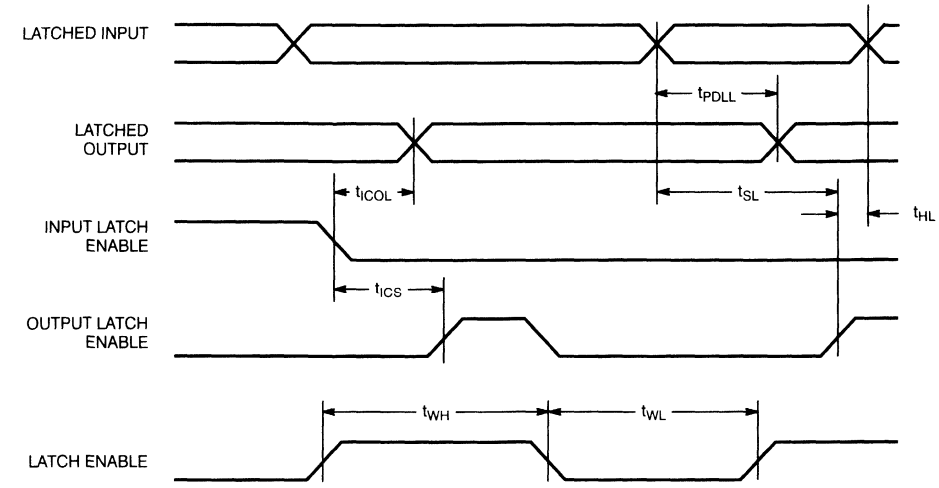


Latched Input

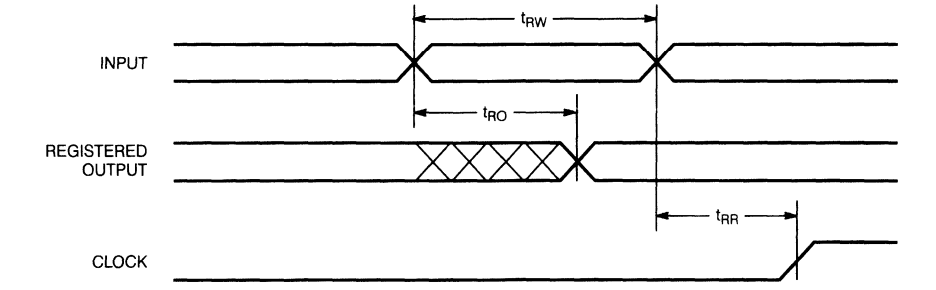


Switching Waveforms (continued)

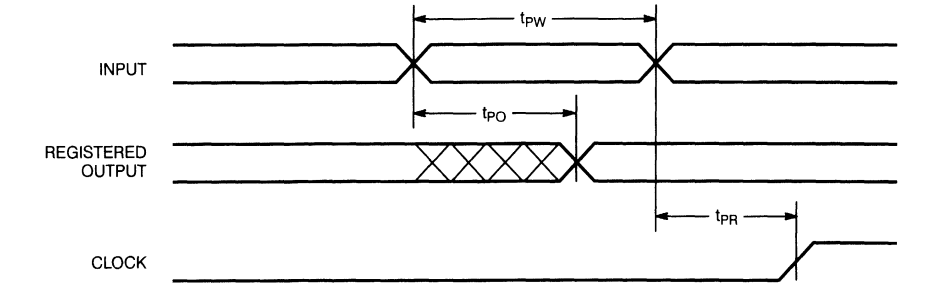
Latched Input and Output



Asynchronous Reset

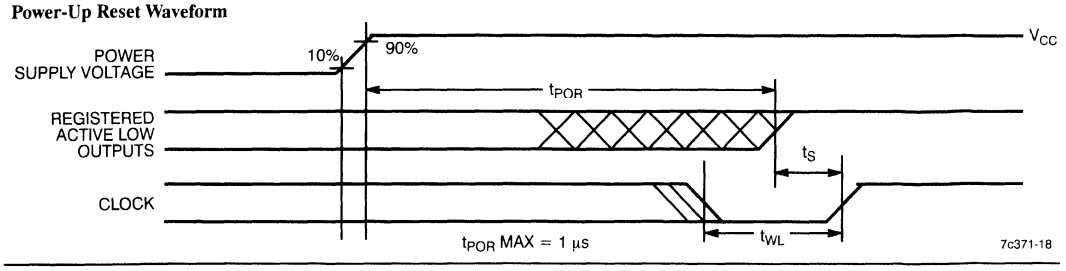


Asynchronous Preset

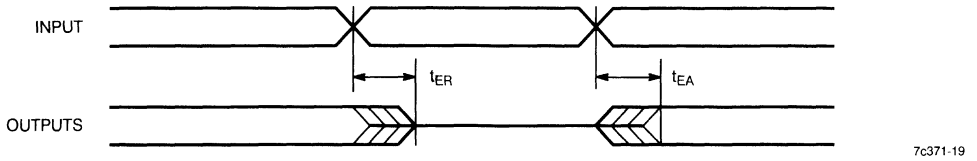


Switching Waveforms (continued)

Power-Up Reset Waveform



Output Enable/Disable



Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
143	CY7C371-143JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
110	CY7C371-110JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
83	CY7C371-83JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C371-83JI	J67	44-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C371-83YMB	Y67	44-Lead Ceramic Leaded Chip Carrier	Military
66	CY7C371-66JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C371-66JI	J67	44-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C371-66YMB	Y67	44-Lead Ceramic Leaded Chip Carrier	Military

Shaded areas contain advanced information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	9, 10, 11
t_{CO}	9, 10, 11
t_{ICO}	9, 10, 11
t_S	9, 10, 11
t_H	9, 10, 11
t_{IS}	9, 10, 11
t_{IH}	9, 10, 11
t_{ICS}	9, 10, 11

Document #: 38-00212-D

64-Macrocell Flash CPLD

Features

- **64 macrocells in four logic blocks**
- **32 I/O pins**
- **6 dedicated inputs including 2 clock pins**
- **No hidden delays**
- **High speed**
  - f_{MAX} = 125 MHz
  - t_{PD} = 10 ns
  - t_S = 5.5 ns
  - t_{CO} = 6.5 ns
- **Electrically alterable Flash technology**
- **Available in 44-pin PLCC and CLCC packages**
- **Pin compatible with the CY7C371**

Functional Description

The CY7C372 is a Flash erasable Complex Programmable Logic Device (CPLD) and is part of the FLASH370™ family of high-density, high-speed CPLDs. Like all members of the FLASH370 family, the CY7C372 is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

The 64 macrocells in the CY7C372 are divided between four logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

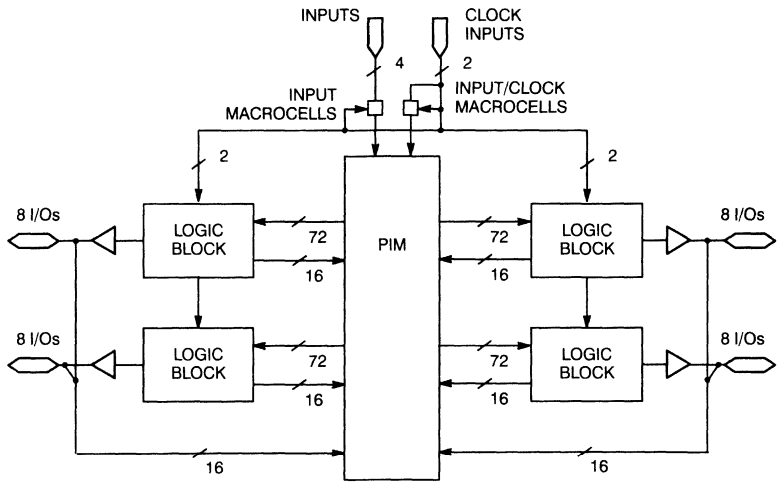
The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370 family, the CY7C372 is rich in I/O resources. Every two macrocells in the device feature an associated I/O pin, resulting in 32 I/O pins on the CY7C372. In addition, there are four dedicated inputs and two input/clock pins.

Finally, the CY7C372 features a very simple timing model. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used. or the type of application, the timing parameters on the CY7C372 remain the same.

3

Logic Block Diagram

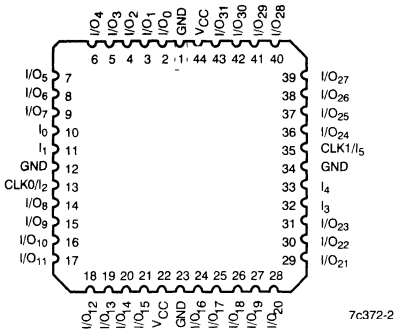


Selection Guide

		7C372–125	7C372–100	7C372–83	7C372–66
Maximum Propagation Delay t_{PD} (ns)		10	12	15	20
Maximum Standby Current, I_{CC1} (mA)	Commercial	250	250	250	250
	Military			300	300
Maximum Operating Current, I_{CC2} (mA)	Commercial	280	280	280	280
	Military			330	330

Shaded area contains advanced information.

Pin Configuration



Functional Description (continued)

Logic Block

The number of logic blocks distinguishes the members of the FLASH370 family. The CY7C372 includes four logic blocks. Each logic block is constructed of a product term array, a product term allocator, and 16 macrocells.

Product Term Array

The product term array in the FLASH370 logic block includes 36 inputs from the PIM and outputs 86 product terms to the product term allocator. The 36 inputs from the PIM are available in both positive and negative polarity, making the overall array size 72 x 86. This large array in each logic block allows for very complex functions to be implemented in a single pass through the device.

Product Term Allocator

The product term allocator is a dynamic, configurable resource that shifts product terms to macrocells that require them. Any number of product terms between 0 and 16 inclusive can be assigned to any of the logic block macrocells (this is called product term steering). Furthermore, product terms can be shared among multiple macrocells. This means that product terms that are common to more than one output can be implemented in a single product term. Product term steering and product term sharing help to increase the effective density of the FLASH370 PLDs. Note that product term allocation is handled by software and is invisible to the user.

I/O Macrocell

Half of the macrocells on the CY7C372 have separate I/O pins associated with them. In other words, each I/O pin is shared by two macrocells. The input to the macrocell is the sum of between 0 and 16 product terms from the product term allocator. The macrocell includes a register that can be optionally bypassed. It also has polarity control, and two global clocks to trigger the register. The I/O macrocell also features a separate feedback path to the PIM so that the register can be buried if the I/O pin is used as an input.

Buried Macrocell

The buried macrocell is very similar to the I/O macrocell. Again, it includes a register that can be configured as combinatorial, as a D flip-flop, a T flip-flop, or a latch. The clock for this register has the same options as described for the I/O macrocell. One difference on the buried macrocell is the addition of input register capability. The user can program the buried macrocell to act as an input register (D-type or latch) whose input comes from the I/O pin associated with the neighboring macrocell. The output of all buried macrocells is sent directly to the PIM regardless of its configuration.

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) connects the four logic blocks on the CY7C372 to the inputs and to each other. All inputs (including feedbacks) travel through the PIM. There is no speed penalty incurred by signals traversing the PIM.

Development Tools

Development software for the CY7C372 is available from Cypress's *Warp2*™ and *Warp3*™ software packages. Both of these products are based on the IEEE standard VHDL language. Cypress also supports third-party vendors such as ABEL™, CUPL™, and LOG/iC™. Please contact your local Cypress representative for further information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Program Voltage 12.5V

Output Current into Outputs ..... 16 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Military[1]	−55°C to +125°C	5V ± 10%

Note:

1. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C372 Min.	7C372 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = −3.2 mA (Com'l/Ind)	2.4		V
			I_{OH} = −2.0 mA (Mil)			V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 16 mA (Com'l/Ind)		0.5	V
			I_{OL} = 12 mA (Mil)			V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs[3]		2.0	7.0	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs[3]		−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−50	+50	μA
I_{OS}	Output Short Circuit Current[4, 5]	V_{CC} = Max., V_{OUT} = 0.5V		−30	−90	mA
I_{CC1}	Power Supply Current (Standby)	V_{CC} = Max., I_{OUT} = 0 mA, f = 0 mHz, V_{IN} = GND, V_{CC}	Com'l		250	mA
			Mil		300	
I_{CC2}	Power Supply Current[5]	V_I = V_{CC} or GND, f = 40 MHz	Com'l		280	mA
			Mil		330	

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V at f=1 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V at f = 1 MHz	12	pF

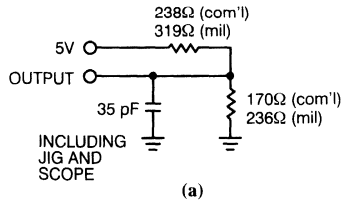
Endurance Characteristics[5]

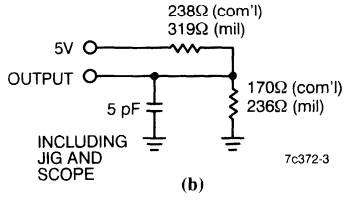
Parameter	Description	Test Conditions	Min.	Max.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions	100		Cycles

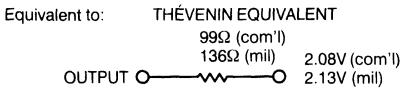
Notes:

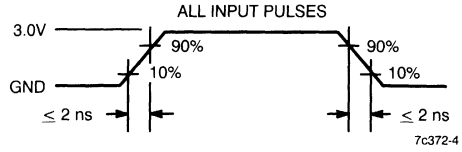
2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms









Switching Characteristics Over the Operating Range[6]

Parameter	Description	7C372–125		7C372–100		7C372–83		7C372–66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters										
t_{PD}	Input to Combinatorial Output		10		12		15		20	ns
t_{PDL}	Input to Output Through Transparent Input or Output Latch		13		15		18		22	ns
t_{PDLL}	Input to Output Through Transparent Input and Output Latches		15		16		19		24	ns
t_{EA}	Input to Output Enable		14		16		19		24	ns
t_{ER}	Input to Output Disable		14		16		19		24	ns
Input Registered/Latched Mode Parameters										
t_{WL}	Clock or Latch Enable Input LOW Time[5]	3		3		4		5		ns
t_{WH}	Clock or Latch Enable Input HIGH Time[5]	3		3		4		5		ns
t_{IS}	Input Register or Latch Set-Up Time	2		2		3		4		ns
t_{IH}	Input Register or Latch Hold Time	2		2		3		4		ns
t_{ICO}	Input Register Clock or Latch Enable to Combinatorial Output		14		16		19		24	ns
t_{ICOL}	Input Register Clock or Latch Enable to Output Through Transparent Output Latch		16		18		21		26	ns
Output Registered/Latched Mode Parameters										
t_{CO}	Clock or Latch Enable to Output		6.5		6.5		8		10	ns
t_S	Set-Up Time from Input to Clock or Latch Enable	5.5		6.5		8		10		ns
t_H	Register or Latch Data Hold Time	0		0		0		0		ns
t_{CO2}	Output Clock or Latch Enable to Output Delay (Through Memory Array)		14		16		19		24	ns
t_{SCS}	Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array)	8		10		12		15		ns
t_{SL}	Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch Enable	10		12		15		20		ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Clock or Latch Enable	0		0		0		0		ns
f_{MAX1}	Maximum Frequency with Internal Feedback in Output Registered Mode (Least of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[5]	125		100		83		66		MHz
f_{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)[5]	153.8		153.8		125		100		MHz
f_{MAX3}	Maximum Frequency with External Feedback (Lesser of $1/(t_{CO} + t_S)$ and $1/(t_{WL} + t_{WH})$)[5]	83.3		77		62.5		50		MHz
$t_{OH}-t_{IH}$ 37x	Output Data Stable from Output clock Minus Input Register Hold Time for 7C37x[5, 7]	0		0		0		0		ns
Pipelined Mode Parameters										
t_{ICS}	Input Register Clock to Output Register Clock	8		10		12		15		ns
f_{MAX4}	Maximum Frequency in Pipelined Mode (Least of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)[5]	125		100		83.3		66.6		MHz

Shaded area contains advanced information.

Note:

6. All AC parameters are measured with 16 outputs switching.
7. This specification is intended to guarantee interface compatibility of the other members of the FLASH370 family with the CY7C372. This specification is met for the devices operating at the same ambient temperature and at the same power supply voltage.

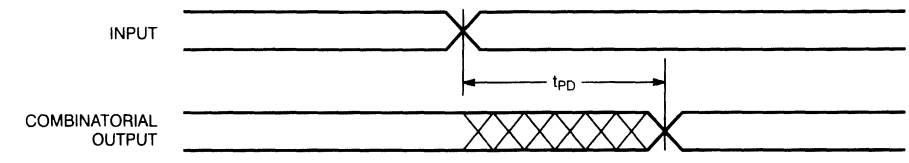
Switching Characteristics Over the Operating Range[6] (continued)

Parameter	Description	7C372–125		7C372–100		7C372–83		7C372–66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Preset Parameters										
t_{RW}	Asynchronous Reset Width[5]	10		12		15		20		ns
t_{RR}	Asynchronous Reset Recovery Time[5]	12		14		17		22		ns
t_{RO}	Asynchronous Reset to Output		16		18		21		26	ns
t_{PW}	Asynchronous Preset Width[5]	10		12		15		20		ns
t_{PR}	Asynchronous Preset Recovery Time[5]	12		14		17		22		ns
t_{PO}	Asynchronous Preset to Output		16		18		21		26	ns
t_{POR}	Power-On Reset[5]		1		1		1		1	µs

Shaded area contains advanced information.

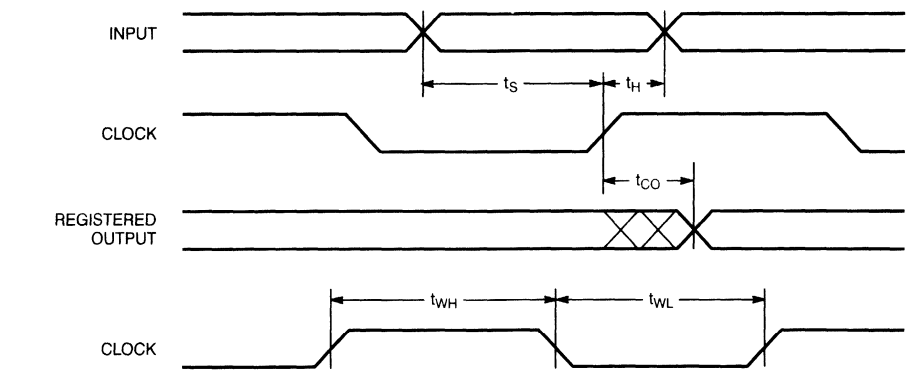
Switching Waveforms

Combinatorial Output



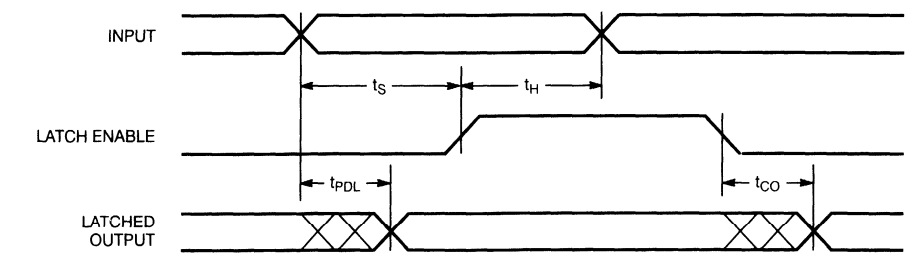
7c372-5

Registered Output



7c372-6

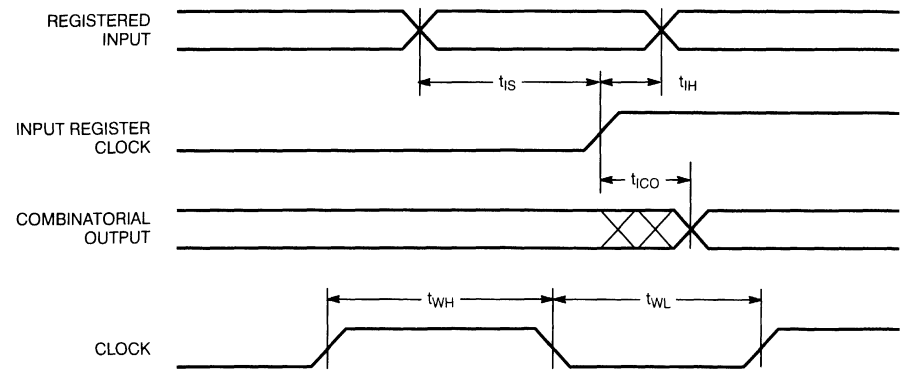
Latched Output



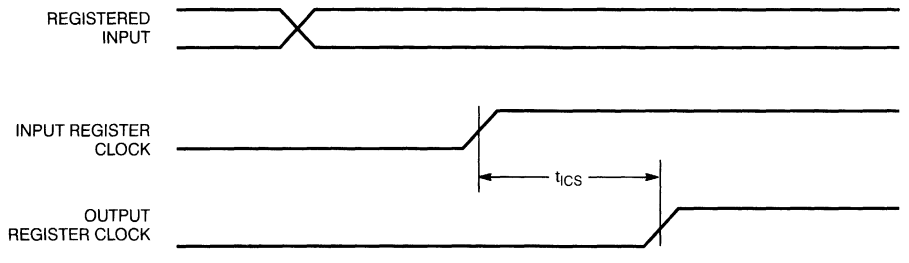
7c372-7

Switching Waveforms (continued)

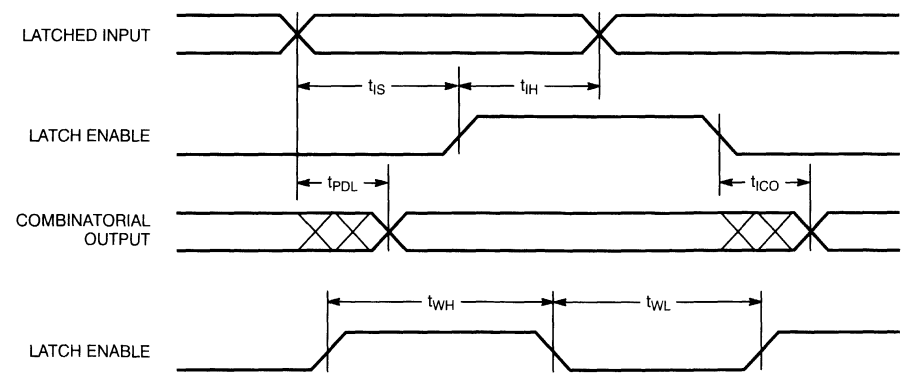
Registered Input



Input Clock to Output Clock

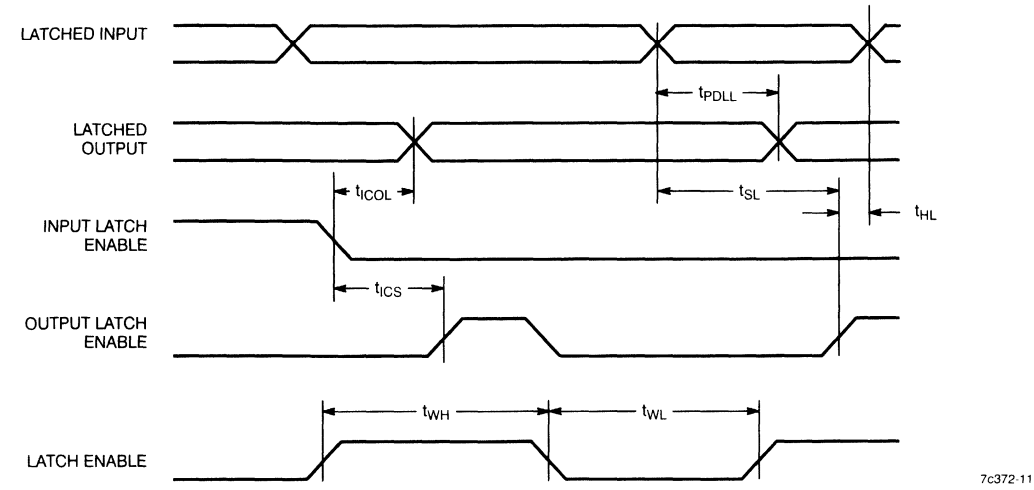


Latched Input

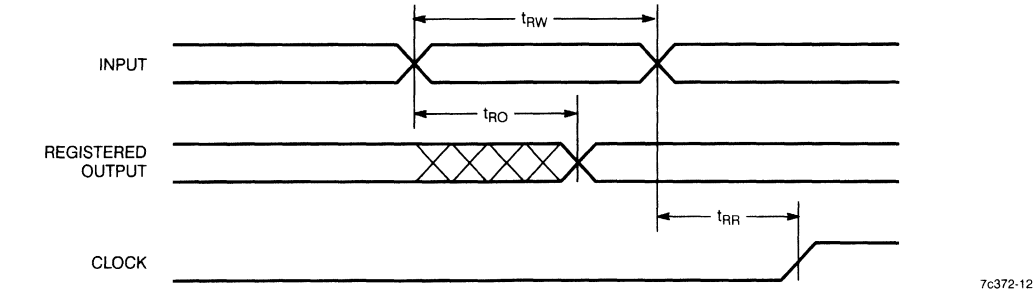


Switching Waveforms (continued)

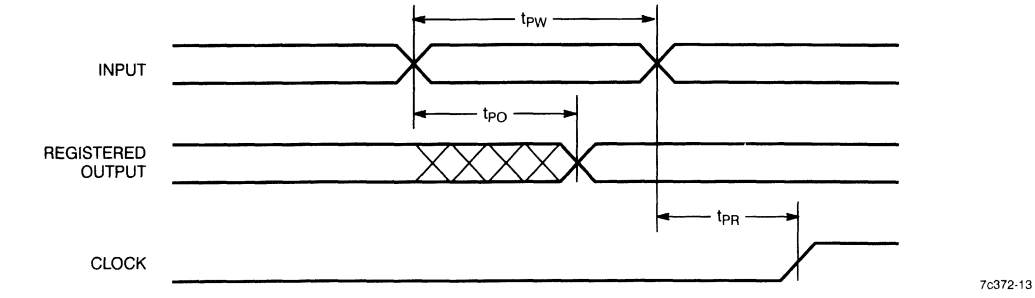
Latched Input and Output



Asynchronous Reset

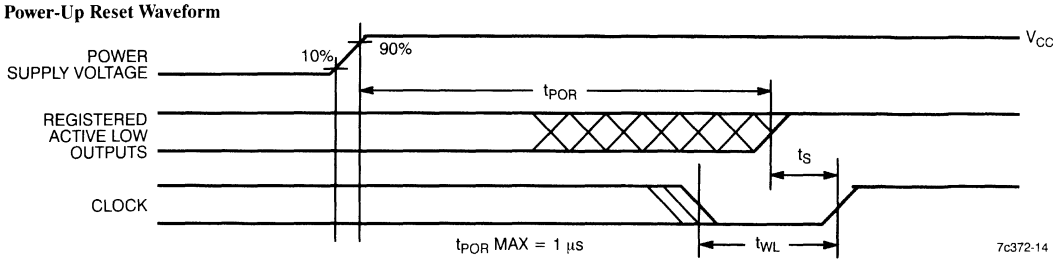


Asynchronous Preset

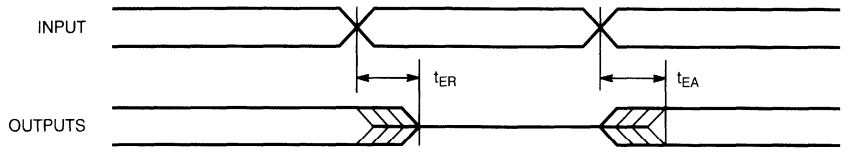


Switching Waveforms (continued)

Power-Up Reset Waveform



Output Enable/Disable



Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
125	CY7C372–125JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
100	CY7C372–100JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
83	CY7C372–83JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C372–83YMB	Y67	44-Lead Ceramic Leaded Chip Carrier	Military
66	CY7C372–66JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C372–66YMB	Y67	44-Lead Ceramic Leaded Chip Carrier	Military

Shaded areas contain advanced information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	9, 10, 11
t_{CO}	9, 10, 11
t_{ICO}	9, 10, 11
t_S	9, 10, 11
t_H	9, 10, 11
t_{IS}	9, 10, 11
t_{IH}	9, 10, 11
t_{ICS}	9, 10, 11

Document #: 38–00213–B

64-Macrocell Flash CPLD

Features

- **64 macrocells in four logic blocks**
- **64 I/O pins**
- **6 dedicated inputs including 4 clock pins**
- **No hidden delays**
- **High speed**
  - **f_{MAX} = 125 MHz**
  - **t_{PD} = 10 ns**
  - **t_S = 5.5 ns**
  - **t_{CO} = 6.5 ns**
- **Electrically alterable Flash technology**
- **Available in 84-pin PLCC, CLCC, and PGA and 100-pin TQFP packages**
- **Pin compatible with the CY7C374**

Functional Description

The CY7C373 is a Flash erasable Complex Programmable Logic Device (CPLD) and is part of the FLASH370™ family of high-density, high-speed CPLDs. Like all members of the FLASH370 family, the CY7C373 is designed to bring the ease of use and high performance of the 22V10 to high-density CPLDs.

The 64 macrocells in the CY7C373 are divided between four logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370 family, the CY7C373 is rich in I/O resources. Every macrocell in the device features an associated I/O pin, resulting in 64 I/O pins on the CY7C373. In addition, there are two dedicated inputs and four input/clock pins.

Finally, the CY7C373 features a very simple timing model. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C373 remain the same.

Logic Block

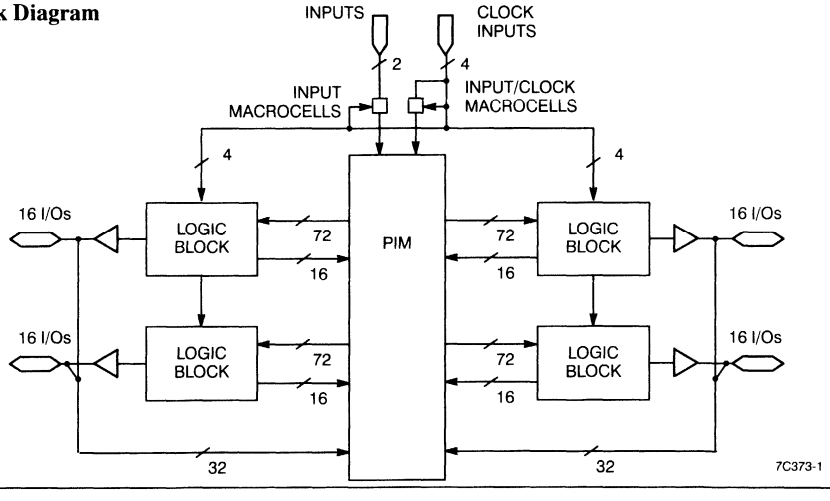
The number of logic blocks distinguishes the members of the FLASH370 family. The CY7C373 includes four logic blocks. Each logic block is constructed of a product term array, a product term allocator, and 16 macrocells.

Product Term Array

The product term array in the FLASH370 logic block includes 36 inputs from the PIM and outputs 86 product terms to the product term allocator. The 36 inputs from the PIM are available in both positive and negative polarity, making the overall array size 72 x 86. This large array in each logic block allows for very complex functions to be implemented in single passes through the device.

3

Logic Block Diagram



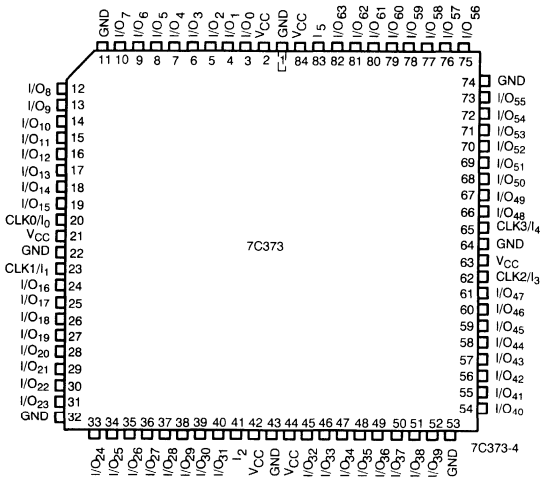
Selection Guide

		7C373–125	7C373–100	7C373–83	7C373–66
Maximum Propagation Delay t_{PD} (ns)		10	12	15	20
Maximum Standby Current, I_{CC1} (mA)	Commercial	250	250	250	250
	Military			300	300
Maximum Operating Current, I_{CC2} (mA)	Commercial	280	280	280	280
	Military			330	330

Shaded area contains advanced information.

Pin Configurations

PLCC/CLCC
Top View

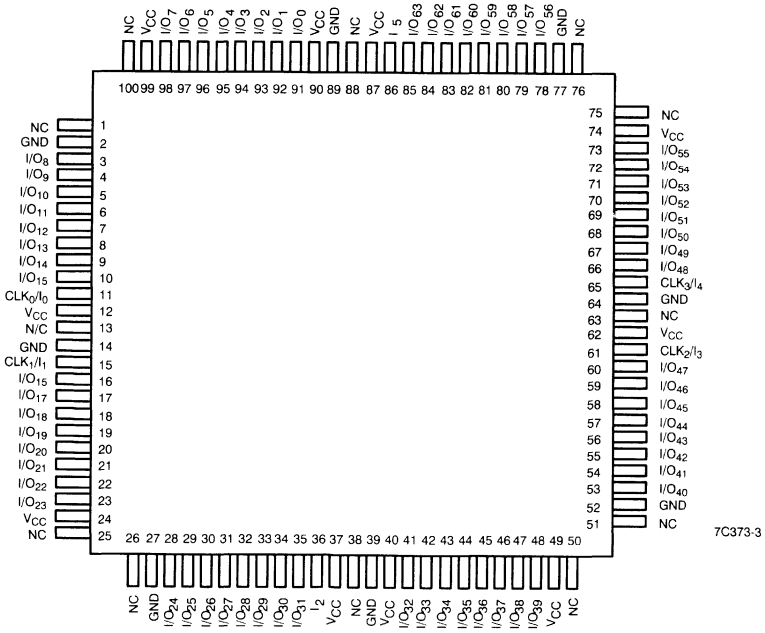


PGA
Bottom View

	1	2	3	4	5	6	7	8	9	10	11
L	I/O23	I/O25	I/O26	I/O28	I/O31	I/O33	VCC	I/O34	I/O36	I/O37	I/O39
K	I/O21	GND	I/O24	I/O27	I/O30	I2	I/O32	I/O35	I/O38	GND	I/O41
J	I/O20	I/O22			I/O29	VCC	GND			I/O40	I/O42
H	I/O18	I/O19								I/O43	I/O44
G	CLK1 /I1	I/O16	GND						CLK2 /I3	I/O46	I/O47
F	I/O17	CLK0 /I0	VCC						VCC	I/O45	GND
E	I/O15	I/O14	I/O13						I/O49	I/O48	CLK3 /I4
D	I/O12	I/O11								I/O51	I/O50
C	I/O10	I/O8	■		I/O1	VCC	I5			I/O54	I/O52
B	I/O9	GND	I/O6	I/O3	I/O0	I/O61	I/O62	I/O59	I/O56	GND	I/O53
A	I/O7	I/O5	I/O4	I/O2	VCC	GND	I/O63	I/O60	I/O58	I/O57	I/O55

7C373-2

TQFP
Top View



Functional Description (continued)

Product Term Allocator

The product term allocator is a dynamic, configurable resource that shifts product term resources to macrocells that require them. Any number of product terms between 0 and 16 inclusive can be assigned to any of the logic block macrocells (this is called product term steering). Furthermore, product terms can be shared among multiple macrocells. This means that product terms that are common to more than one output can be implemented in a single product term. Product term steering and product term sharing help to increase the effective density of the FLASH370 CPLDs. Note that the product term allocator is handled by software and is invisible to the user.

I/O Macrocell

Each of the macrocells on the CY7C373 has a separate I/O pin associated with it. In other words, each I/O pin is shared by two macrocells. The input to the macrocell is the sum of between 0 and 16 product terms from the product term allocator. The macrocell includes a register that can be optionally bypassed, polarity control over the input sum-term, and two global clocks to trigger the register. The macrocell also features a separate feedback path to the PIM so that the register can be buried if the I/O pin is used as an input.

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) connects the four logic blocks on the CY7C373 to the inputs and to each other. All inputs (including feedbacks) travel through the PIM. There is no speed penalty incurred by signals traversing the PIM.

Development Tools

Development software for the CY7C373 is available from Cypress's *Warp2*™ and *Warp3*™ software packages. Both of these products are based on the IEEE standard VHDL language. Cypress also supports third-party vendors such as ABEL™, CUPL™, and LOG/iC™. Please contact your local Cypress representative for further information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Program Voltage 12.5V

Output Current into Outputs ..... 16 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... >2001V

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Military[1]	−55°C to +125°C	5V ± 10%

Note:

1. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions			7C373 Min.	7C373 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = −3.2 mA (Com'l/Ind)		2.4		V
			I_{OH} = −2.0 mA (Mil)				V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 16 mA (Com'l/Ind)			0.5	V
			I_{OL} = 12 mA (Mil)				V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs[3]			2.0	7.0	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs[3]			−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			−50	+50	μA
I_{OS}	Output Short Circuit Current[4, 5]	V_{CC} = Max., V_{OUT} = 0.5V			−30	−90	mA
I_{CC1}	Power Supply Current (Standby)	V_{CC} = Max., I_{OUT} = 0 mA, f = 0 mHz, V_{IN} = GND, V_{CC}		Com'l		250	mA
				Mil		300	
I_{CC2}	Power Supply Current[5]	V_I = V_{CC} or GND, f = 40 MHz		Com'l		280	mA
				Mil		330	

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V at f=1 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V at f = 1 MHz	12	pF

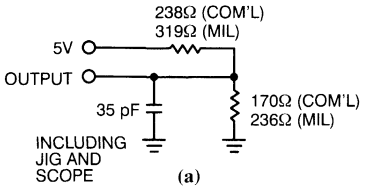
Endurance Characteristics

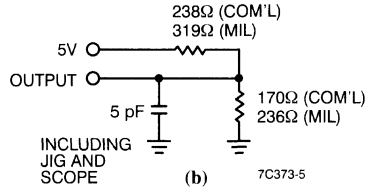
Parameter	Description	Test Conditions	Min.	Max.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions	100		Cycles

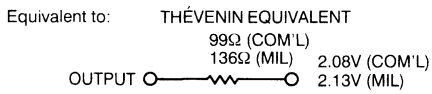
Notes:

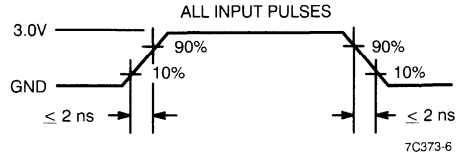
2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms









Switching Characteristics Over the Operating Range[6]

Parameter	Description	7C373–125		7C373–100		7C373–83		7C373–66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters										
t_{PD}	Input to Combinatorial Output		10		12		15		20	ns
t_{PDL}	Input to Output Through Transparent Input or Output Latch		13		15		18		22	ns
t_{PDLL}	Input to Output Through Transparent Input and Output Latches		15		16		19		24	ns
t_{EA}	Input to Output Enable		14		16		19		24	ns
t_{ER}	Input to Output Disable		14		16		19		24	ns
Input Registered/Latched Mode Parameters										
t_{WL}	Clock or Latch Enable Input LOW Time[5]	3		3		4		5		ns
t_{WH}	Clock or Latch Enable Input HIGH Time[5]	3		3		4		5		ns
t_{IS}	Input Register or Latch Set-Up Time	2		2		3		4		ns
t_{IH}	Input Register or Latch Hold Time	2		2		3		4		ns
t_{ICO}	Input Register Clock or Latch Enable to Combinatorial Output		14		16		19		24	ns
t_{ICOL}	Input Register Clock or Latch Enable to Output Through Transparent Output Latch		16		18		21		26	ns
Output Registered/Latched Mode Parameters										
t_{CO}	Clock or Latch Enable to Output		6.5		6.5		8		10	ns
t_S	Set-Up Time from Input to Clock or Latch Enable	5.5		6.5		8		10		ns
t_H	Register or Latch Data Hold Time	0		0		0		0		ns
t_{CO2}	Output Clock or Latch Enable to Output Delay (Through Memory Array)		14		16		19		24	ns
t_{SCS}	Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array)	8		10		12		15		ns
t_{SL}	Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch Enable	10		12		15		20		ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Clock or Latch Enable	0		0		0		0		ns
f_{MAX1}	Maximum Frequency with Internal Feedback (Least of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[5]	125		100		83		66		MHz
f_{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)[5]	153.8		153.8		125		100		MHz
f_{MAX3}	Maximum Frequency of (2) CY7C373s with External Feedback (Lesser of $1/(t_{CO} + t_S)$ and $1/(t_{WL} + t_{WH})$)[5]	83.3		77		62.5		50		MHz
$t_{OH}-t_{IH}$ 37x	Output Data Stable from Output clock Minus Input Register Hold Time for 7C37x[5, 7]	0		0		0		0		ns
Pipelined Mode Parameters										
t_{ICS}	Input Register Clock to Output Register Clock	8		10		12		15		ns
f_{MAX4}	Maximum Frequency in Pipelined Mode (Least of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)[5]	125		83.3		66.6		50.0		MHz

Shaded area contains advanced information.

Note:

6. All AC parameters are measured with 16 outputs switching.
7. This specification is intended to guarantee interface compatibility of the other members of the FLASH370 family with the CY7C373. This specification is met for the devices operating at the same ambient temperature and at the same power supply voltage.

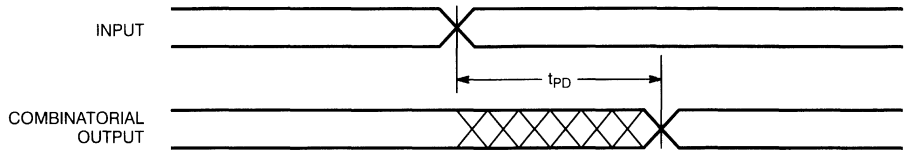
Switching Characteristics Over the Operating Range[6] (continued)

Parameter	Description	7C373–125		7C373–100		7C373–83		7C373–66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Preset Parameters										
t_{RW}	Asynchronous Reset Width[5]	10		12		15		20		ns
t_{RR}	Asynchronous Reset Recovery Time[5]	12		14		17		22		ns
t_{RO}	Asynchronous Reset to Output		16		18		21		26	ns
t_{PW}	Asynchronous Preset Width[5]	10		12		15		20		ns
t_{PR}	Asynchronous Preset Recovery Time[5]	12		14		17		22		ns
t_{PO}	Asynchronous Preset to Output		16		18		21		26	ns
t_{POR}	Power-On Reset[5]		1		1		1		1	µs

Shaded area contains advanced information.

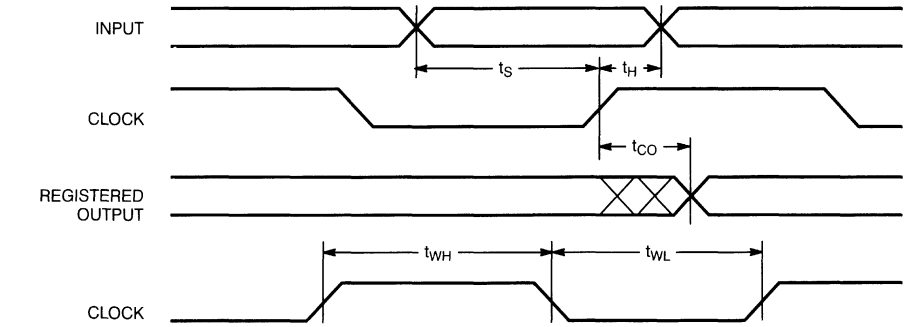
Switching Waveforms

Combinatorial Output



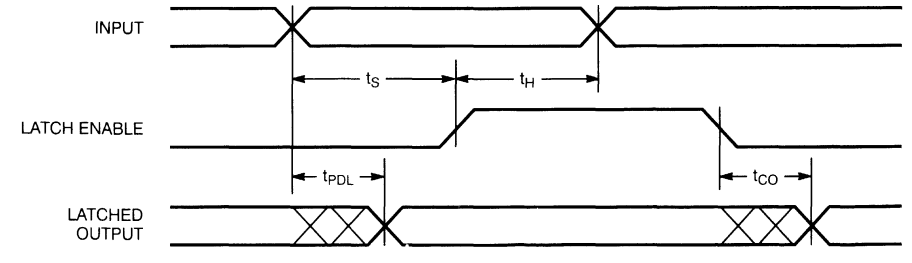
7C373-7

Registered Output



7C373-8

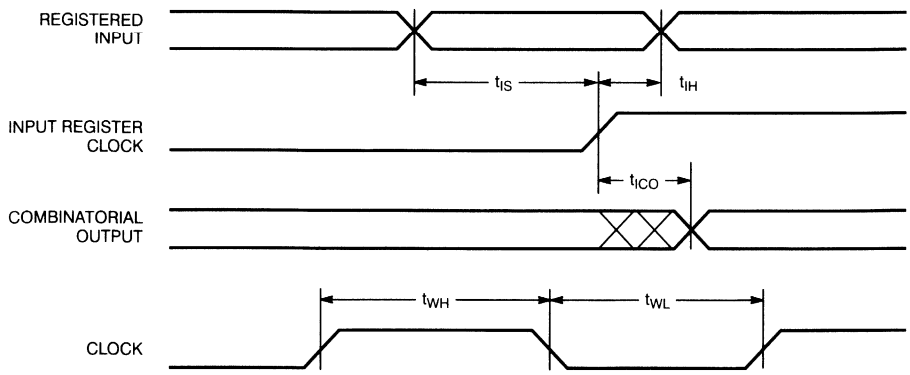
Latched Output



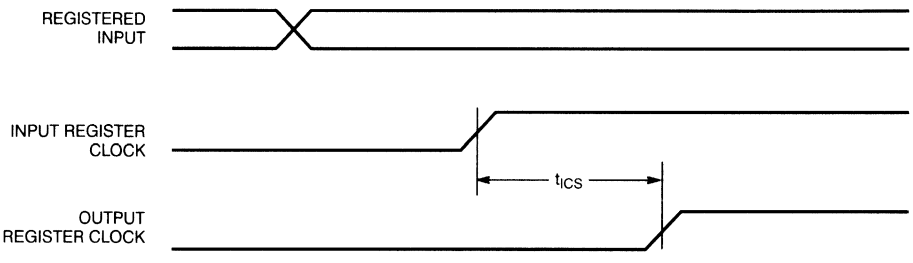
7C373-9

Switching Waveforms (continued)

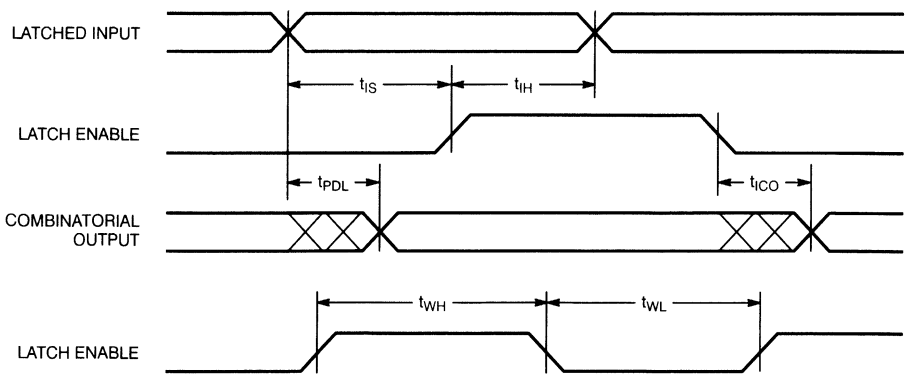
Registered Input



Input Clock to Output Clock

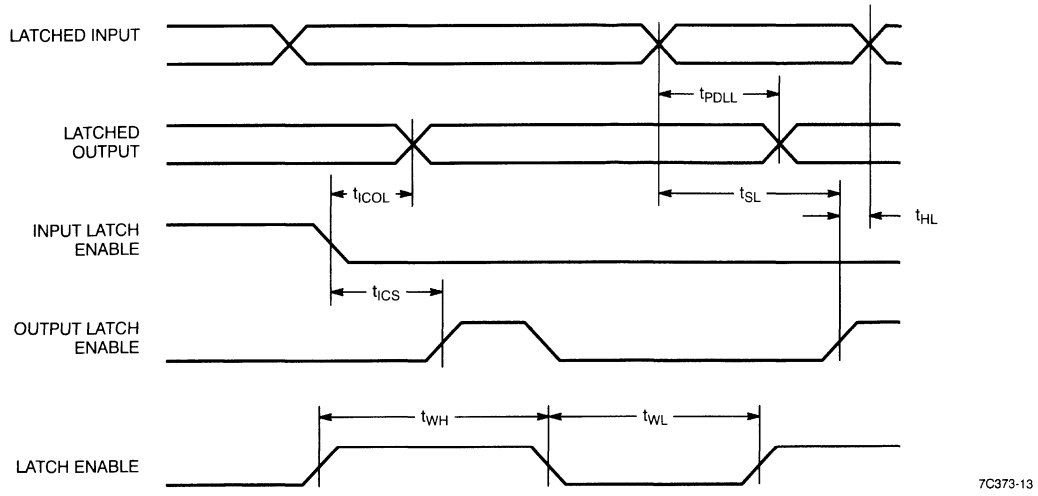


Latched Input

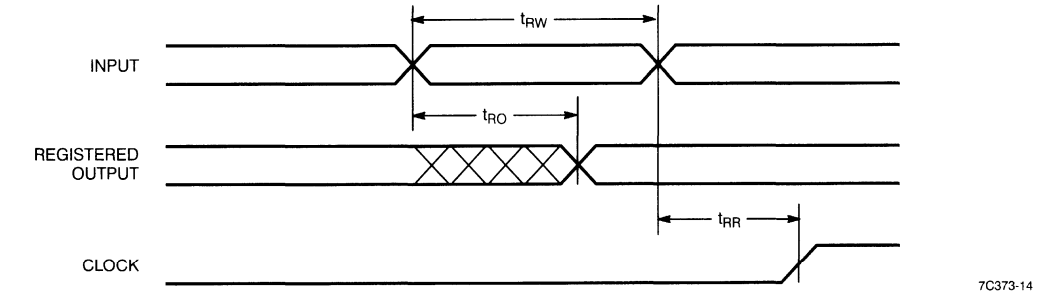


Switching Waveforms (continued)

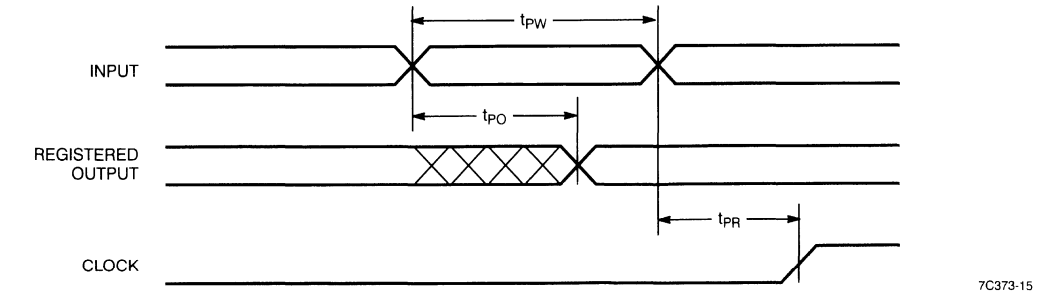
Latched Input and Output



Asynchronous Reset

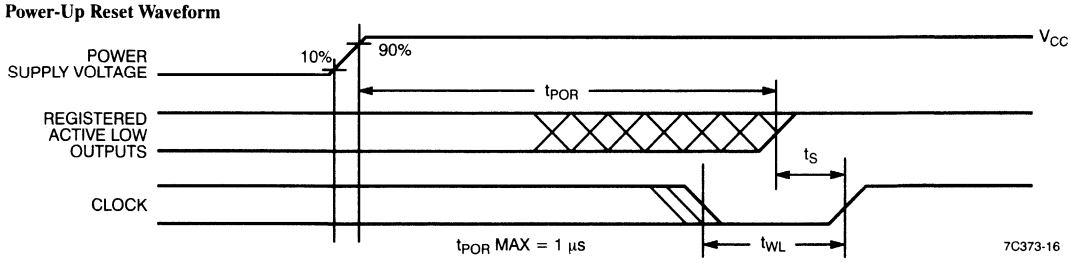


Asynchronous Preset

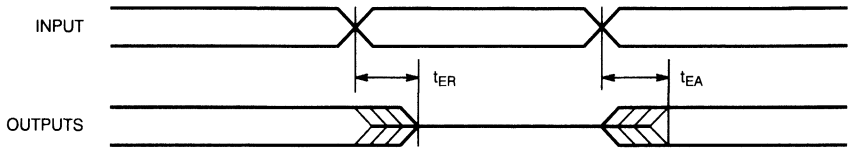


Switching Waveforms (continued)

Power-Up Reset Waveform



Output Enable/Disable



3

Ordering Information

Speed (MHz)	Ordering Code	Package Type	Package Type	Operating Range
110	CY7C373–125AC	A100	100-Pin Thin Quad Flatpack	Commercial
	CY7C373–125GC	G84	84-Pin Grid Array (Cavity Up)	
	CY7C373–125JC	J83	84-Lead Plastic Leaded Chip Carrier	
100	CY7C373–100AC	A100	100-Pin Thin Quad Flatpack	Commercial
	CY7C373–100GC	G84	84-Pin Grid Array (Cavity Up)	
	CY7C373–100JC	J83	84-Lead Plastic Leaded Chip Carrier	
83	CY7C373–83AC	A100	100-Pin Thin Quad Flatpack	Commercial
	CY7C373–83GC	G84	84-Pin Grid Array (Cavity Up)	
	CY7C373–83JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C373–83GMB	G84	84-Pin Grid Array (Cavity Up)	Military
	CY7C373–83YMB	Y84	84-Pin Ceramic Leaded Chip Carrier	
66	CY7C373–66AC	A100	100-Pin Thin Quad Flatpack	Commercial
	CY7C373–66GC	G84	84-Pin Grid Array (Cavity Up)	
	CY7C373–66JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C373–66GMB	G84	84-Pin Grid Array (Cavity Up)	Military
	CY7C373–66YMB	Y84	84-Pin Ceramic Leaded Chip Carrier	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	9, 10, 11
t_{CO}	9, 10, 11
t_{ICO}	9, 10, 11
t_S	9, 10, 11
t_H	9, 10, 11
t_{IS}	9, 10, 11
t_{IH}	9, 10, 11
t_{ICS}	9, 10, 11

Document #: 38-00216-B

128-Macrocell Flash CPLD

Features

- **128 macrocells in eight logic blocks**
- **64 I/O pins**
- **6 dedicated inputs including 4 clock pins**
- **No hidden delays**
- **High speed**
  - **f_{MAX} = 100 MHz**
  - **t_{PD} = 12 ns**
  - **t_S = 7 ns**
  - **t_{CO} = 7 ns**
- **Electrically Alterable Flash technology**
- **Available in 84-pin PLCC, 84-pin CLCC, 100-pin TQFP, and 84-pin PGA packages**
- **Pin compatible with the CY7C373**

Functional Description

The CY7C374 is a Flash erasable Complex Programmable Logic Device (CPLD) and is part of the FLASH370™ family of high-density, high-speed CPLDs. Like all members of the FLASH370 family, the CY7C374 is designed to bring the ease of use and high performance of the 22V10 to high-density CPLDs.

The 128 macrocells in the CY7C374 are divided between eight logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370 family, the CY7C374 is rich in I/O resources. Every two macrocells in the device feature an associated I/O pin, resulting in 64 I/O pins on the CY7C374. In addition, there are two dedicated inputs and four input/clock pins.

Finally, the CY7C374 features a very simple timing model. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C374 remain the same.

Logic Block

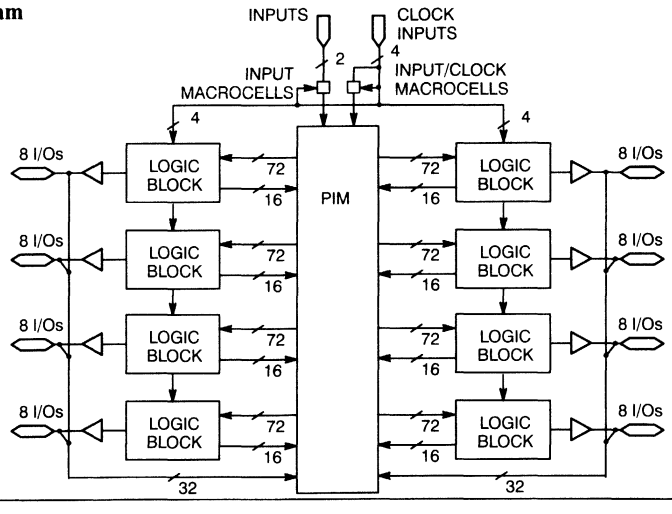
The number of logic blocks distinguishes the members of the FLASH370 family. The CY7C374 includes eight logic blocks. Each logic block is constructed of a product term array, a product term allocator, and 16 macrocells.

Product Term Array

The product term array in the FLASH370 logic block includes 36 inputs from the PIM and outputs 86 product terms to the product term allocator. The 36 inputs from the PIM are available in both positive and negative polarity, making the overall array size 72 x 86. This large array in each logic block allows for very complex functions to be implemented in single passes through the device.

3

Logic Block Diagram

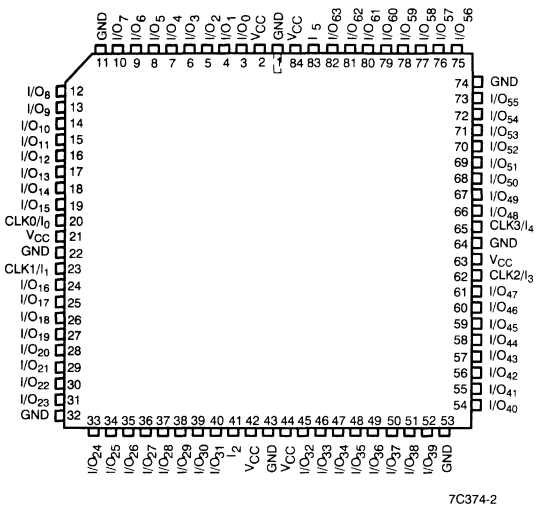


Selection Guide

		7C374–100	7C374–83	7C374–66
Maximum Propagation Delay t_{PD} (ns)		12	15	20
Maximum Standby Current, I_{CC1} (mA)	Commercial	300	300	300
	Military		370	370
Maximum Operating Current, I_{CC2} (mA)	Commercial	330	330	330
	Military		400	400

Pin Configurations

PLCC/CLCC
Top View



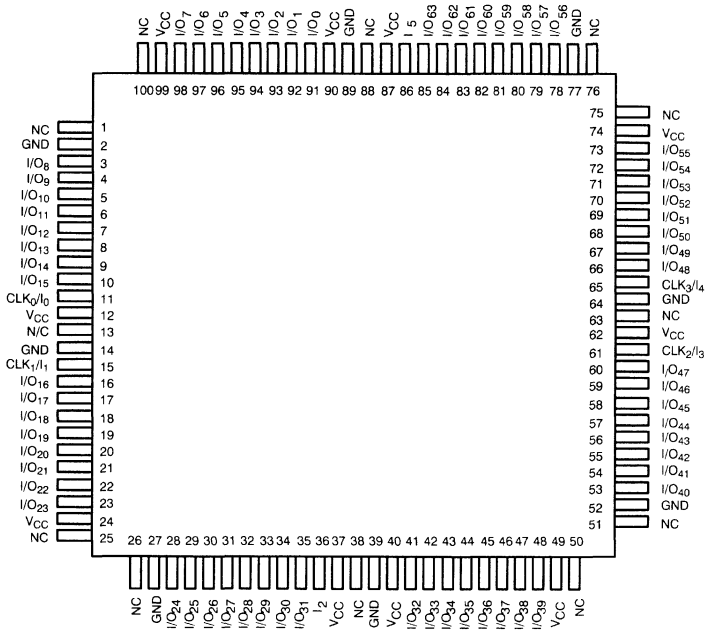
7C374-2

PGA
Bottom View

	1	2	3	4	5	6	7	8	9	10	11
L	I/O23	I/O25	I/O26	I/O28	I/O31	I/O33	VCC	I/O34	I/O36	I/O37	I/O39
K	I/O21	GND	I/O24	I/O27	I/O30	I2	I/O32	I/O35	I/O38	GND	I/O41
J	I/O20	I/O22			I/O29	VCC	GND			I/O40	I/O42
H	I/O18	I/O19								I/O43	I/O44
G	CLK1 /I1	I/O16	GND						CLK2 /I3	I/O46	I/O47
F	I/O17	CLK0 /I0	VCC						VCC	I/O45	GND
E	I/O15	I/O14	I/O13						I/O49	I/O48	CLK3 /I4
D	I/O12	I/O11								I/O51	I/O50
C	I/O10	I/O8	■		I/O1	VCC	I5			I/O54	I/O52
B	I/O9	GND	I/O6	I/O3	I/O0	I/O61	I/O62	I/O59	I/O56	GND	I/O53
A	I/O7	I/O5	I/O4	I/O2	VCC	GND	I/O63	I/O60	I/O58	I/O57	I/O55

7C374-3

TQFP
Top View



7C374-4

Functional Description (continued)

Product Term Allocator

The product term allocator is a dynamic, configurable resource that shifts product terms to macrocells that require them. Any number of product terms between 0 and 16 inclusive can be assigned to any of the logic block macrocells (this is called product term steering). Furthermore, product terms can be shared among multiple macrocells. This means that product terms that are common to more than one output can be implemented in a single product term. Product term steering and product term sharing help to increase the effective density of the FLASH370 CPLDs. Note that product term allocation is handled by software and is invisible to the user.

I/O Macrocell

Half of the macrocells on the CY7C374 have I/O pins associated with them. The input to the macrocell is the sum of between 0 and 16 product terms from the product term allocator. The I/O macrocell includes a register that can be optionally bypassed, polarity control over the input sum-term, and two global clocks to trigger the register. The macrocell also features a separate feedback path to the PIM so that the register can be buried if the I/O pin is used as an input.

Buried Macrocell

The buried macrocell is very similar to the I/O macrocell. Again, it includes a register that can be configured as combinatorial, as a D flip-flop, a T flip-flop, or a latch. The clock for this register has the same options as described for the I/O macrocell. One difference on the buried macrocell is the addition of input register capability. The user can program the buried macrocell to act as an input register (D-type of latch) whose input comes from the I/O pin associated with the neighboring macrocell. The output of all buried macrocells is sent directly to the PIM regardless of its configuration.

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) connects the eight logic blocks on the CY7C374 to the inputs and to each other. All inputs (including feedbacks) travel through the PIM. There is no speed penalty incurred by signals traversing the PIM.

Development Tools

Development software for the CY7C374 is available from Cypress's *Warp2*™ and *Warp3*™ software packages. Both of these products are based on the IEEE standard VHDL language. Cypress also supports third-party vendors such as ABEL™, CUPL™, and LOG/iC™. Please contact your local Cypress representative for further information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Program Voltage 12.5V

Output Current into Outputs ..... 16 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Military[1]	−55°C to +125°C	5V ± 10%

Note:

1. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions			7C374 Min.	7C374 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = −3.2 mA (Com'l/Ind)		2.4		V
			I_{OH} = −2.0 mA (Mil)				V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 16 mA (Com'l/Ind)			0.5	V
			I_{OL} = 12 mA (Mil)				V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH voltage for all inputs[3]			2.0	7.0	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW voltage for all inputs[3]			−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			−50	+50	μA
I_{OS}	Output Short Circuit Current[4, 5]	V_{CC} = Max., V_{OUT} = 0.5V			−30	−90	mA
I_{CC1}	Power Supply Current (Standby)	V_{CC} = Max., I_{OUT} = 0 mA, f = 0 mHz, V_{IN} = GND, V_{CC}		Com'l		300	mA
				Mil		370	
I_{CC2}	Power Supply Current[5]	V_I = V_{CC} or GND, f = 40 MHz		Com'l		330	mA
				Mil		400	

Capacitance[5]

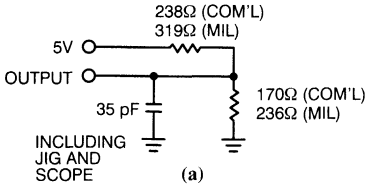
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V at f = 1 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V at f = 1 MHz	12	pF

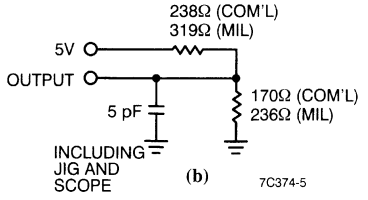
Endurance Characteristics[5]

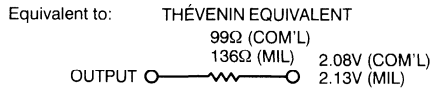
Parameter	Description	Test Conditions	Min.	Max.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions	100		Cycles

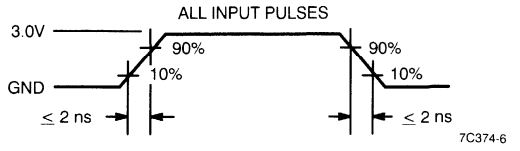
Notes:
2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms









Switching Characteristics Over the Operating Range[6]

Parameter	Description	7C374-100 Min.	7C374-100 Max.	7C374-83 Min.	7C374-83 Max.	7C374-66 Min.	7C374-66 Max.	Unit
Combinatorial Mode Parameters								
t_{PD}	Input to Combinatorial Output		12		15		20	ns
t_{PDL}	Input to Output Through Transparent Input or Output Latch		15		18		22	ns
t_{PDLL}	Input to Output Through Transparent Input and Output Latches		16		19		24	ns
t_{EA}	Input to Output Enable		16		19		24	ns
t_{ER}	Input to Output Disable		16		19		24	ns
Input Registered/Latched Mode Parameters								
t_{WL}	Clock or Latch Enable Input LOW Time[5]	3		4		5		ns
t_{WH}	Clock or Latch Enable Input HIGH Time[5]	3		4		5		ns
t_{IS}	Input Register or Latch Set-Up Time	2		3		4		ns
t_{IH}	Input Register or Latch Hold Time	2		3		4		ns
t_{ICO}	Input Register Clock or Latch Enable to Combinatorial Output		16		19		24	ns
t_{ICOL}	Input Register Clock or Latch Enable to Output Through Transparent Output Latch		18		21		26	ns
Output Registered/Latched Mode Parameters								
t_{CO}	Clock or Latch Enable to Output		7		8		10	ns
t_S	Set-Up Time from Input to Clock or Latch Enable	7		8		10		ns
t_H	Register or Latch Data Hold Time	0		0		0		ns
t_{CO2}	Output Clock or Latch Enable to Output Delay (Through Memory Array)		16		19		24	ns
t_{SCS}	Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array)	10		12		15		ns
t_{SL}	Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch Enable	12		15		20		ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Clock or Latch Enable	0		0		0		ns
f_{MAX1}	Maximum Frequency with Internal Feedback (Least of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[5]	100		83		66		MHz
f_{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)	143		125		100		MHz
f_{MAX3}	Maximum Frequency with External Feedback (Lesser of $1/(t_{CO} + t_S)$ and $1/(t_{WL} + t_{WH})$)	71.4		67.5		50		MHz
$t_{OH}-t_{IH}$ 37x	Output Data Stable from Output clock Minus Input Register Hold Time for 7C37x[5, 7]	0		0		0		ns
Pipelined Mode Parameters								
t_{ICS}	Input Register Clock to Output Register Clock	10		12		15		ns
f_{MAX4}	Maximum Frequency in Pipelined Mode (Least of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)	100		83.3		66.6		MHz

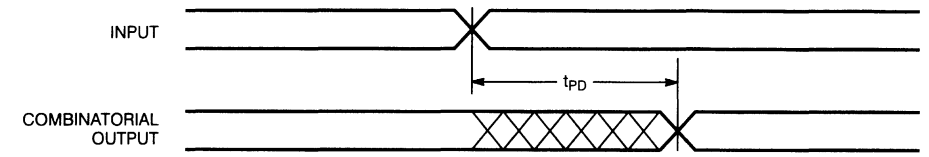
Note:
6. All AC parameters are measured with 16 outputs switching.
7. This specification is intended to guarantee interface compatibility of the other members of the FLASH370 family with the CY7C374. This specification is met for the devices operating at the same ambient temperature and at the same power supply voltage.

Switching Characteristics Over the Operating Range[6] (continued)

Parameter	Description	7C374–100		7C374–83		7C374–66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Preset Parameters								
t_{RW}	Asynchronous Reset Width[5]	12		15		20		ns
t_{RR}	Asynchronous Reset Recovery Time[5]	14		17		22		ns
t_{RO}	Asynchronous Reset to Output		18		21		26	ns
t_{PW}	Asynchronous Preset Width[5]	12		15		20		ns
t_{PR}	Asynchronous Preset Recovery Time[5]	14		17		22		ns
t_{PO}	Asynchronous Preset to Output		18		21		26	ns
t_{POR}	Power-On Reset[5]		1		1		1	µs

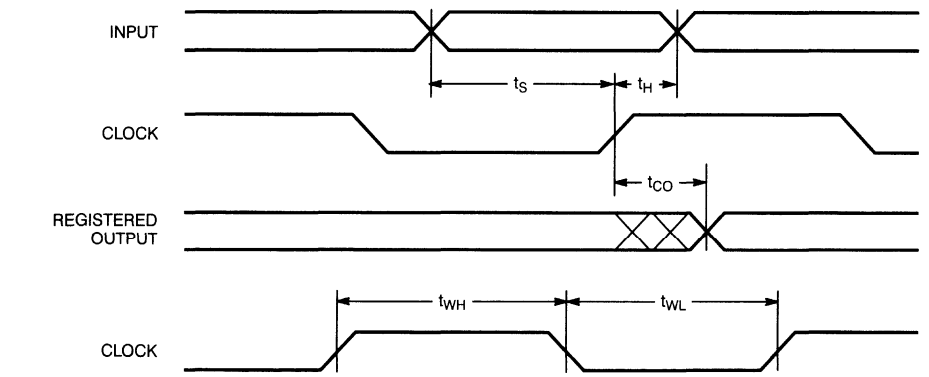
Switching Waveforms

Combinatorial Output



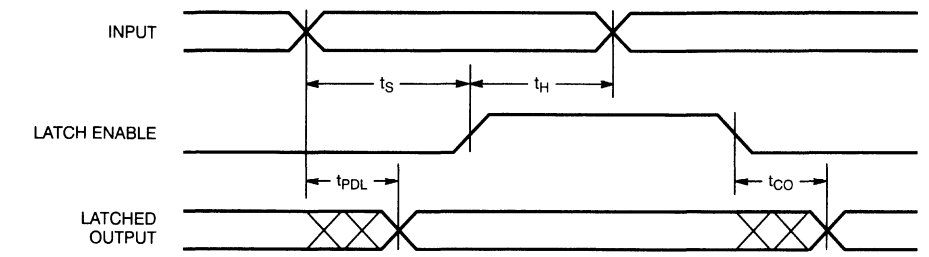
7C374-7

Registered Output



7C374-8

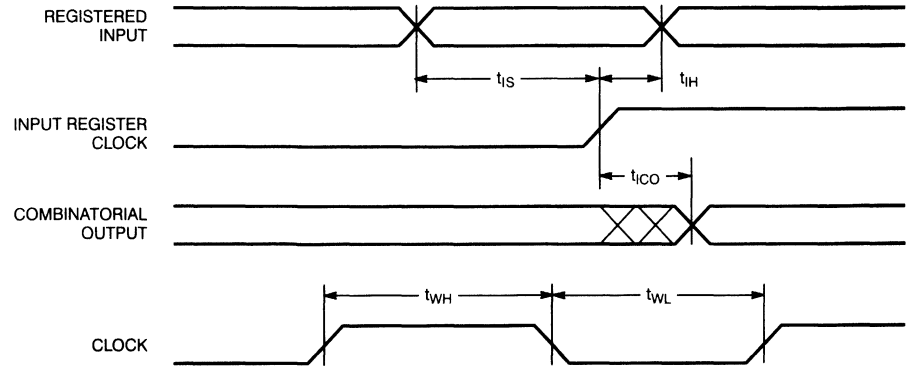
Latched Output



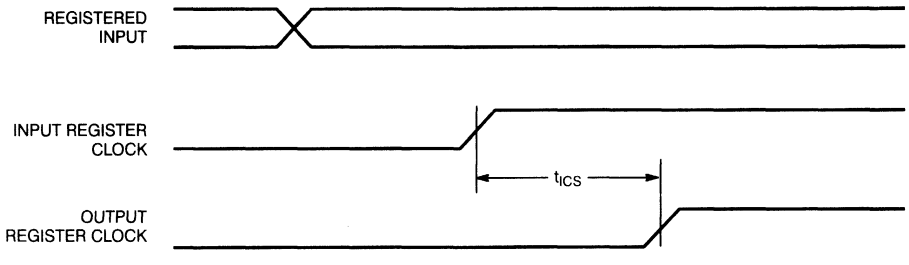
7C374-9

Switching Waveforms (continued)

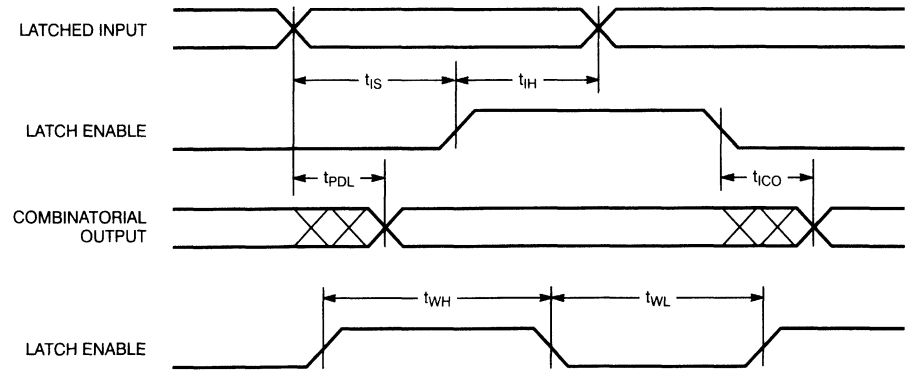
Registered Input



Input Clock to Output Clock

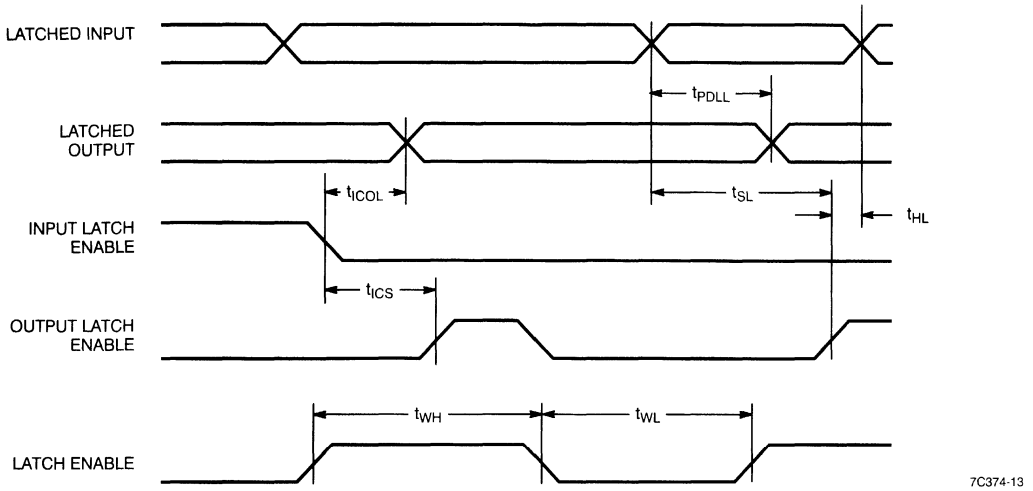


Latched Input

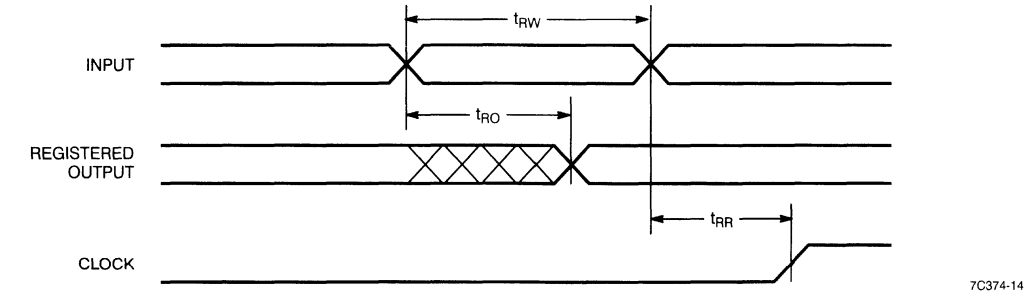


Switching Waveforms (continued)

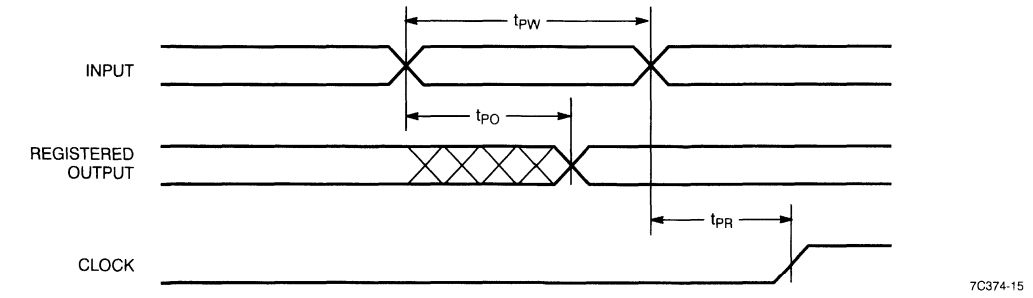
Latched Input and Output



Asynchronous Reset

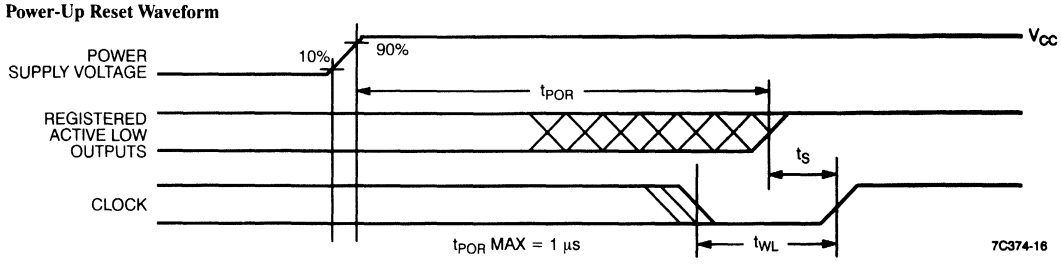


Asynchronous Preset

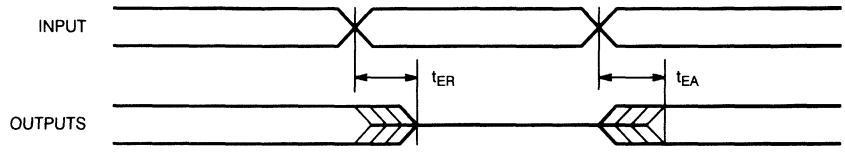


Switching Waveforms (continued)

Power-Up Reset Waveform



Output Enable/Disable



Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
100	CY7C374-100AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C374-100GC	G84	84-Pin Grid Array (Cavity Up)	
	CY7C374-100JC	J83	84-Lead Plastic Leaded Chip Carrier	
83	CY7C374-83AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C374-83GC	G84	84-Pin Grid Array (Cavity Up)	
	CY7C374-83JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C374-83GMB	G84	84-Pin Grid Array (Cavity Up)	Military
	CY7C374-83YMB	Y84	84-Pin Ceramic Leaded Chip Carrier	
66	CY7C374-66AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C374-66GC	G84	84-Pin Grid Array (Cavity Up)	
	CY7C374-66JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C374-66GMB	G84	84-Pin Grid Array (Cavity Up)	Military
	CY7C374-66YMB	Y84	84-Pin Ceramic Leaded Chip Carrier	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3
I_{CC2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	9, 10, 11
t_{PDL}	9, 10, 11
t_{PDLL}	9, 10, 11
t_{CO}	9, 10, 11
t_{ICO}	9, 10, 11
t_{ICOL}	9, 10, 11
t_{S}	9, 10, 11
t_{SL}	9, 10, 11
t_{H}	9, 10, 11
t_{HL}	9, 10, 11
t_{IS}	9, 10, 11
t_{IH}	9, 10, 11
t_{ICS}	9, 10, 11
t_{EA}	9, 10, 11
t_{ER}	9, 10, 11

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128-Macrocell Flash CPLD

Features

- **128 macrocells in eight logic blocks**
- **128 I/O pins**
- **6 dedicated inputs including 4 clock pins**
- **No hidden delays**
- **High speed**
  - f_{MAX} = 100 MHz
  - t_{PD} = 12 ns
  - t_S = 7 ns
  - t_{CO} = 7 ns
- **Electrically alterable Flash technology**
- **Available in 160-pin TQFP, CQFP, and PGA packages**

Functional Description

The CY7C375 is a Flash erasable Complex Programmable Logic Device (CPLD) and is part of the FLASH370™ family of high-density, high-speed CPLDs. Like all members of the FLASH370 family, the CY7C375 is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

The 128 macrocells in the CY7C375 are divided between eight logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

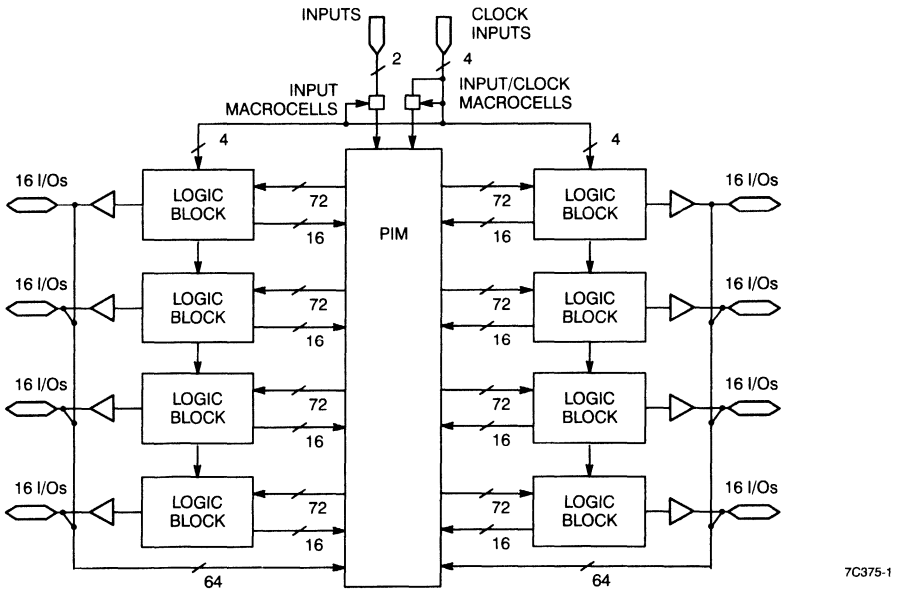
The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370 family, the CY7C375 is rich in I/O resources. Every macrocell in the device features an associated I/O pin, resulting in 128 I/O pins on the CY7C375. In addition, there are two dedicated inputs and four input/clock pins.

Finally, the CY7C375 features a very simple timing model. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C375 remain the same.

3

Logic Block Diagram

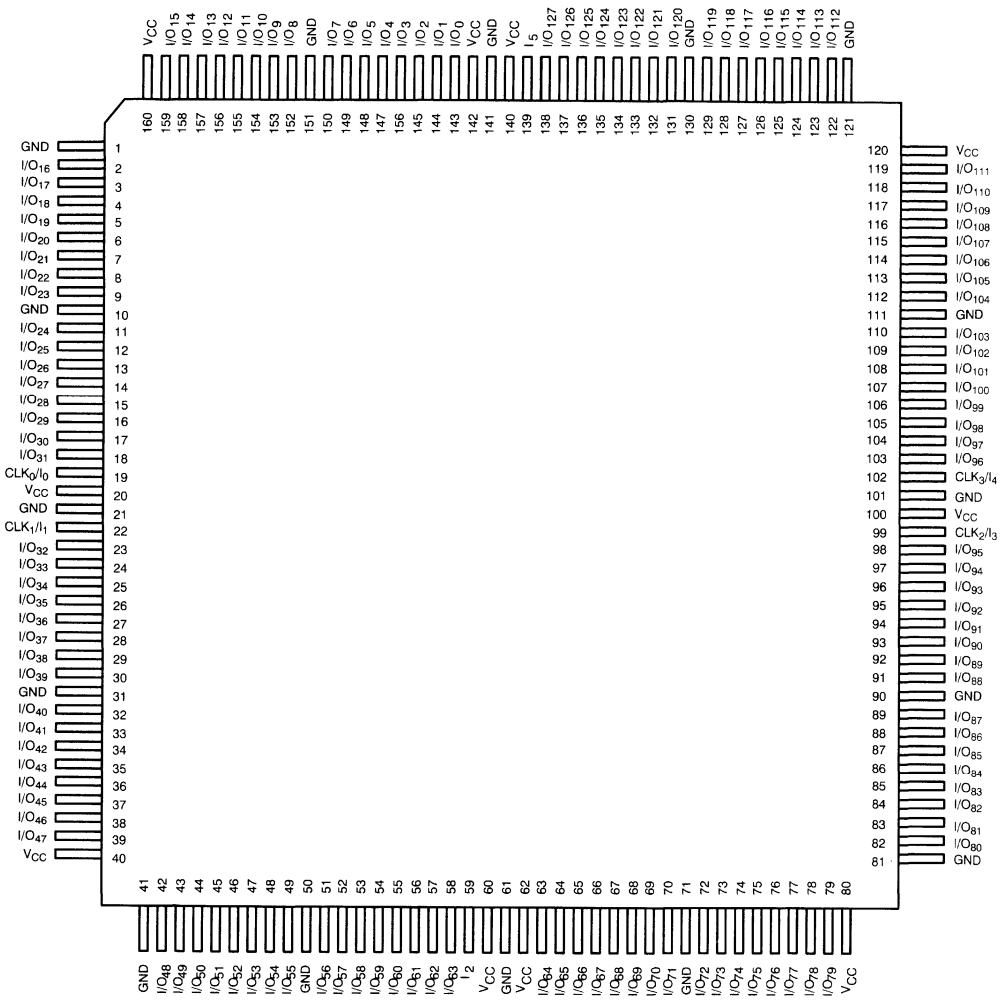


Selection Guide

		7C375–100	7C375–83	7C375–66
Maximum Propagation Delay (ns)		12	15	20
Maximum Standby Current, I_{CC1} (mA)	Commercial	300	300	300
	Military		370	370
Maximum Operating Current, I_{CC2} (mA)	Commercial	330	330	330
	Military		400	400

Pin Configurations

TQFP/CQFP
Top View



7C375-1

Pin Configurations (continued)

PGA
Bottom View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	I/O_{109}	I/O_{112}	I/O_{115}	I/O_{118}	I/O_{121}	I/O_{123}	I/O_{126}	I/O_{127}	I/O_0	I/O_3	I/O_5	I/O_7	I/O_{10}	I/O_{11}	I/O_{14}
P	I/O_{106}	I/O_{110}	I/O_{113}	I/O_{116}	I/O_{119}	I/O_{122}	I/O_{125}	GND	I/O_1	I/O_4	I/O_6	I/O_9	I/O_{13}	NC_{15}	I/O_{16}
N	I/O_{105}	I/O_{108}	I/O_{111}	I/O_{114}	I/O_{117}	I/O_{120}	I/O_{124}	I_5	I/O_2	GND	I/O_8	I/O_{12}	GND	I/O_{17}	I/O_{19}
M	I/O_{102}	I/O_{104}	I/O_{107}	V_{CC}			V_{CC}	GND	V_{CC}			GND	I/O_{18}	I/O_{20}	I/O_{22}
L	I/O_{100}	I/O_{101}	I/O_{103}										I/O_{21}	I/O_{23}	I/O_{25}
K	I/O_{98}	I/O_{99}	GND										I/O_{24}	I/O_{26}	I/O_{27}
J	I/O_{96}	I/O_{97}	CLK3 /I_4	V_{CC}								V_{CC}	I/O_{28}	I/O_{29}	I/O_{30}
H	I/O_{95}	GND	CLK2 /I_3	GND								GND	CLK0 /I_0	GND	I/O_{31}
G	I/O_{94}	I/O_{93}	I/O_{94}	V_{CC}								V_{CC}	CLK1 /I_1	I/O_{33}	I/O_{32}
F	I/O_{91}	I/O_{90}	I/O_{88}										GND	I/O_{35}	I/O_{34}
E	I/O_{89}	I/O_{87}	I/O_{85}										I/O_{39}	I/O_{37}	I/O_{36}
D	I/O_{86}	I/O_{84}	I/O_{82}	GND			V_{CC}	GND	V_{CC}			V_{CC}	I/O_{43}	I/O_{40}	I/O_{38}
C	I/O_{83}	I/O_{81}	GND	I/O_{76}	I/O_{72}	GND	I/O_{66}	I_2	I/O_{60}	I/O_{56}	I/O_{53}	I/O_{50}	I/O_{47}	I/O_{44}	I/O_{41}
B	I/O_{80}	I/O_{79}	I/O_{77}	I/O_{73}	I/O_{70}	I/O_{68}	I/O_{65}	GND	I/O_{61}	I/O_{58}	I/O_{55}	I/O_{52}	I/O_{49}	I/O_{46}	I/O_{42}
A	I/O_{78}	I/O_{75}	I/O_{74}	I/O_{71}	I/O_{69}	I/O_{67}	I/O_{64}	I/O_{63}	I/O_{62}	I/O_{59}	I/O_{57}	I/O_{54}	I/O_{51}	I/O_{48}	I/O_{45}

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Functional Description (continued)

Logic Block

The number of logic blocks distinguishes the members of the FLASH370 family. The CY7C375 includes eight logic blocks. Each logic block is constructed of a product term array, a product term allocator, and 16 macrocells.

Product Term Array

The product term array in the FLASH370 logic block includes 36 inputs from the PIM and outputs 86 product terms to the product term allocator. The 36 inputs from the PIM are available in both positive and negative polarity, making the overall array size 72 x 86. This large array in each logic block allows for very complex functions to be implemented in single passes through the device.

Product Term Allocator

The product term allocator is a dynamic, configurable resource that shifts product terms to macrocells that require them. Any number of product terms between 0 and 16 inclusive can be assigned to any of the logic block macrocells (this is called product term steering). Furthermore, product terms can be shared among multiple macrocells. This means that product terms that are common to more than one output can be implemented in a single product term. Product term steering and product term sharing help to increase the effective density of the FLASH370 PLDs. Note that product term allocation is handled by software and is invisible to the user.

I/O Macrocell

Each of the macrocells on the CY7C375 has a separate I/O pin associated with it. The input to the macrocell is the sum of between 0 and 16 product terms from the product term allocator. The macrocell includes a register that can be optionally bypassed, polarity control over the input sum-term, and four global clocks to trigger the register. The macrocell also features a separate feedback path to the PIM so that the register can be buried if the I/O pin is used as an input.

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) connects the eight logic blocks on the CY7C375 to the inputs and to each other. All inputs (including feedbacks) travel through the PIM. There is no speed penalty incurred by signals traversing the PIM.

Development Tools

Development software for the CY7C375 is available from Cypress's *Warp2*™ and *Warp3*™ software packages. Both of these products are based on the IEEE standard VHDL language. Cypress also supports third-party vendors such as ABEL™, CUPL™, and LOG/iC™. Please contact your local Cypress representative for further information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Program Voltage 12.5V

Output Current into Outputs ..... 16 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Military[1]	−55°C to +125°C	5V ± 10%

Note:

1. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions			7C375 Min.	7C375 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = −3.2 mA (Com'l/Ind)		2.4		V
			I_{OH} = −2.0 mA (Mil)				V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 16 mA (Com'l/Ind)			0.5	V
			I_{OL} = 12 mA (Mil)				V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH voltage for all inputs[3]			2.0	7.0	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW voltage for all inputs[3]			−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			−50	+50	μA
I_{OS}	Output Short Circuit Current[4, 5]	V_{CC} = Max., V_{OUT} = 0.5V			−30	−90	mA
I_{CC1}	Power Supply Current (Standby)	V_{CC} = Max., I_{OUT} = 0 mA, f = 0 mHz, V_{IN} = GND, V_{CC}		Com'l		300	mA
				Mil		370	
I_{CC2}	Power Supply Current[5]	V_I = V_{CC} or GND, f = 40 MHz		Com'l		330	mA
				Mil		400	

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V at f = 1 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V at f = 1 MHz	12	pF

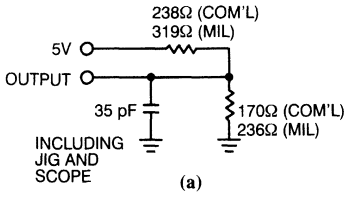
Endurance Characteristics[5]

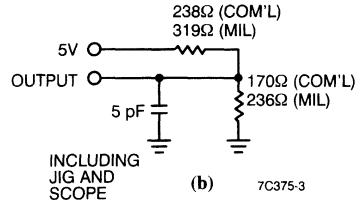
Parameter	Description	Test Conditions	Min.	Max.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions	100		Cycles

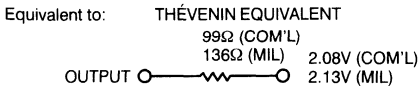
Notes:

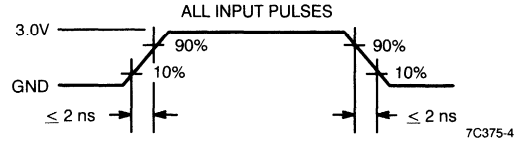
2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms









Switching Characteristics Over the Operating Range[6]

Parameter	Description	7C375–100		7C375–83		7C375–66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters								
t_{PD}	Input to Combinatorial Output		12		15		20	ns
t_{PDL}	Input to Output Through Transparent Input or Output Latch		15		18		22	ns
t_{PDLL}	Input to Output Through Transparent Input and Output Latches		16		19		24	ns
t_{EA}	Input to Output Enable		16		19		24	ns
t_{ER}	Input to Output Disable		16		19		24	ns
Input Registered/Latched Mode Parameters								
t_{WL}	Clock or Latch Enable Input LOW Time[5]	3		4		5		ns
t_{WH}	Clock or Latch Enable Input HIGH Time[5]	3		4		5		ns
t_{IS}	Input Register or Latch Set-Up Time	2		3		4		ns
t_{IH}	Input Register or Latch Hold Time	2		3		4		ns
t_{ICO}	Input Register Clock or Latch Enable to Combinatorial Output		16		19		24	ns
t_{ICOL}	Input Register Clock or Latch Enable to Output Through Transparent Output Latch		18		21		26	ns
Output Registered/Latched Mode Parameters								
t_{CO}	Clock or Latch Enable to Output		7		8		10	ns
t_S	Set-Up Time from Input to Clock or Latch Enable	7		8		10		ns
t_H	Register or Latch Data Hold Time	0		0		0		ns
t_{CO2}	Output Clock or Latch Enable to Output Delay (Through Memory Array)		16		19		24	ns
t_{SCS}	Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array)	10		12		15		ns
t_{SL}	Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch Enable	12		15		20		ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Clock or Latch Enable	0		0		0		ns
f_{MAX1}	Maximum Frequency with Internal Feedback (Least of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[5]	100		83		66		MHz
f_{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)	143		125		100		MHz
f_{MAX3}	Maximum Frequency with External Feedback (Lesser of $1/(t_{CO} + t_S)$ and $1/(t_{WL} + t_{WH})$)	71.4		62.5		50		MHz
$t_{OH} - t_{IH}$ 37x	Output Data Stable from Output clock Minus Input Register Hold Time for 7C37x[5, 7]	0		0		0		ns
Pipelined Mode Parameters								
t_{ICS}	Input Register Clock to Output Register Clock	10		12		15		ns
f_{MAX4}	Maximum Frequency in Pipelined Mode (Least of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)	100		83.3		66.6		MHz

Note:

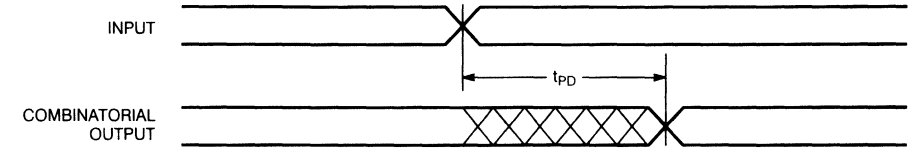
6. All AC parameters are measured with 16 outputs switching.
7. This specification is intended to guarantee interface compatibility of the other members of the FLASH370 family with the CY7C375. This specification is met for the devices operating at the same ambient temperature and at the same power supply voltage.

Switching Characteristics Over the Operating Range[6] (continued)

Parameter	Description	7C375–100		7C375–83		7C375–66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Preset Parameters								
t_{RW}	Asynchronous Reset Width[5]	12		15		20		ns
t_{RR}	Asynchronous Reset Recovery Time[5]	14		17		22		ns
t_{RO}	Asynchronous Reset to Output		18		21		26	ns
t_{PW}	Asynchronous Preset Width[5]	12		15		20		ns
t_{PR}	Asynchronous Preset Recovery Time[5]	14		17		22		ns
t_{PO}	Asynchronous Preset to Output		18		21		26	ns
t_{POR}	Power-On Reset		1		1		1	µs

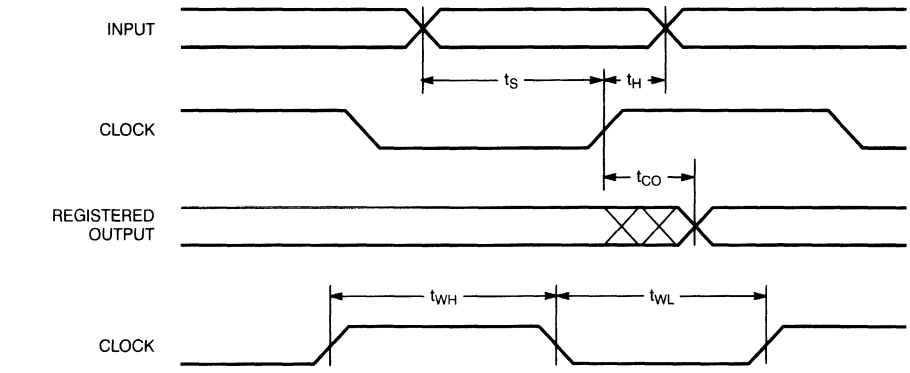
Switching Waveforms

Combinatorial Output



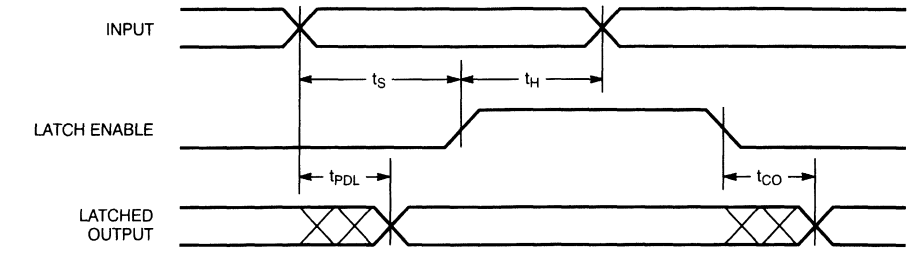
7C375-5

Registered Output



7C375-6

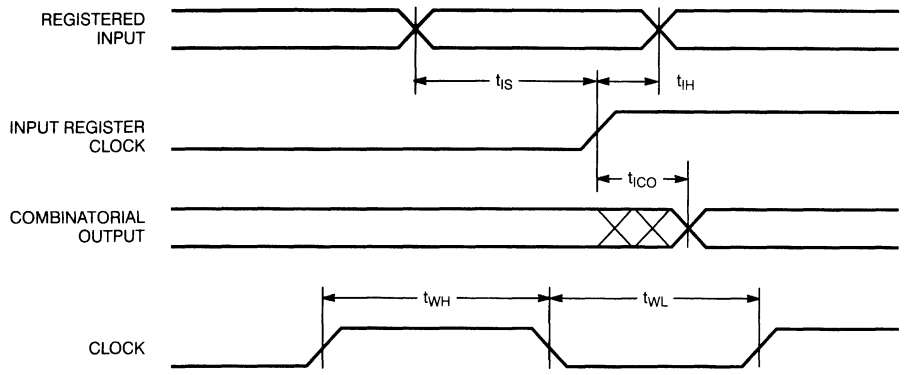
Latched Output



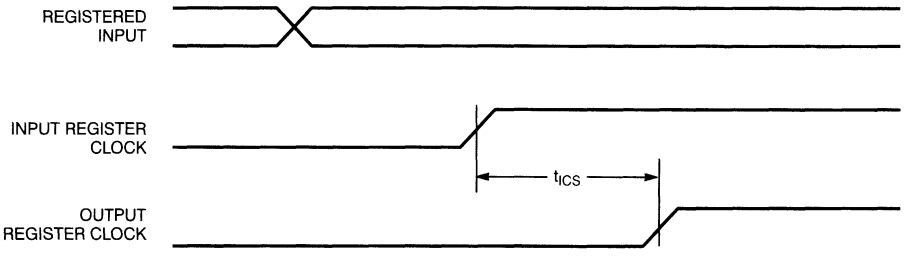
7C375-7

Switching Waveforms (continued)

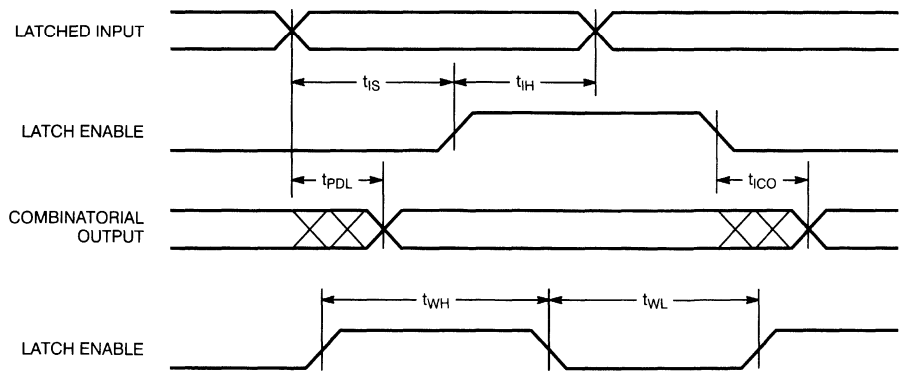
Registered Input



Input Clock to Output Clock

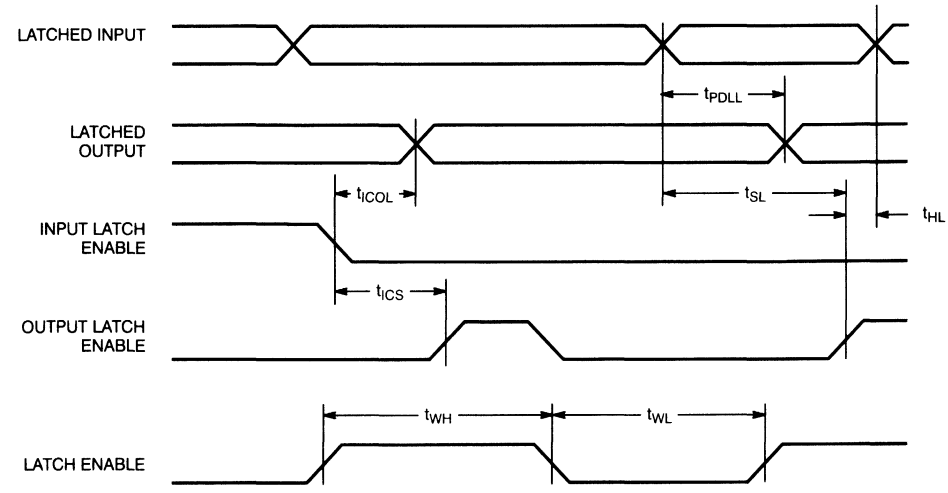


Latched Input

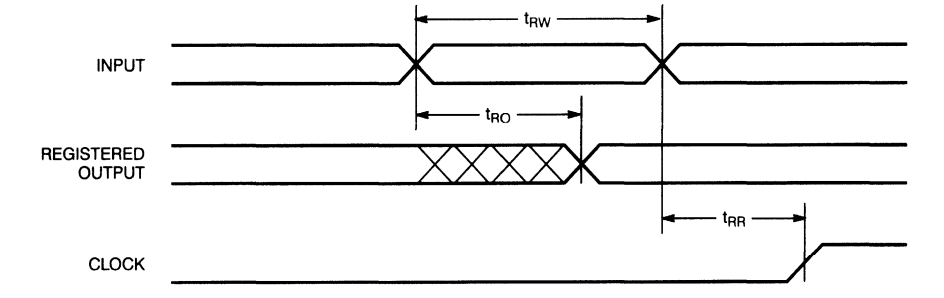


Switching Waveforms (continued)

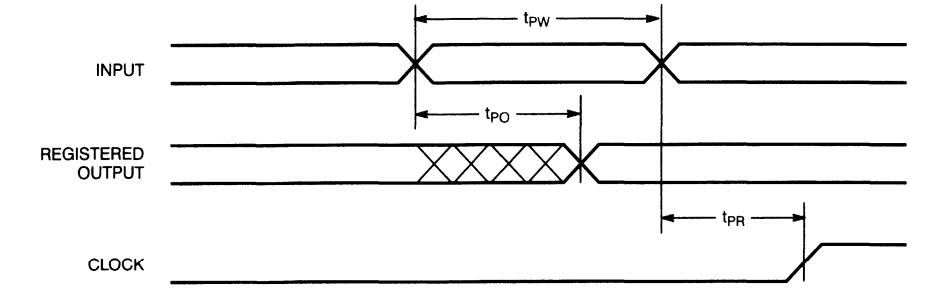
Latched Input and Output



Asynchronous Reset

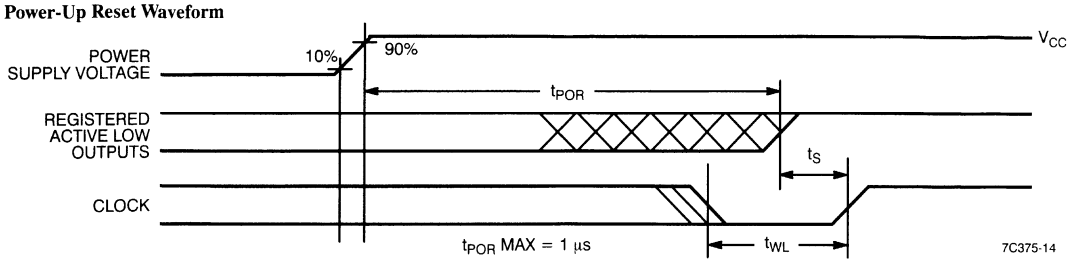


Asynchronous Preset

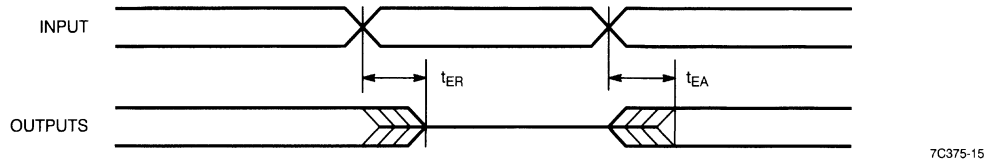


Switching Waveforms (continued)

Power-Up Reset Waveform



Output Enable/Disable



Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
100	CY7C375–100AC	A160	160-Lead Thin Quad Flatpack	Commercial
83	CY7C375–83AC	A160	160-Lead Thin Quad Flatpack	Commercial
	CY7C375–83GMB	G160	160-Pin Grid Array	Military
	CY7C375–83UMB	U162	160-Pin Ceramic Quad Flatpack	
66	CY7C375–66AC	A160	160-Lead Thin Quad Flatpack	Commercial
	CY7C375–66GMB	G160	160-Pin Grid Array	Military
	CY7C375–66UMB	U162	160-Pin Ceramic Quad Flatpack	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3
I_{CC2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	9, 10, 11
t_{PDL}	9, 10, 11
t_{PDLL}	9, 10, 11
t_{CO}	9, 10, 11
t_{ICO}	9, 10, 11
t_{ICOL}	9, 10, 11
t_S	9, 10, 11
t_{SL}	9, 10, 11
t_H	9, 10, 11
t_{HL}	9, 10, 11
t_{IS}	9, 10, 11
t_{IH}	9, 10, 11
t_{ICS}	9, 10, 11
t_{EA}	9, 10, 11
t_{ER}	9, 10, 11

Document #: 38-00217-C

CYPRESS *ADVANCED INFORMATION* **CY7C376**

192-Macrocell Flash CPLD

Features

- **192 macrocells in 12 logic blocks**
- **128 I/O pins**
- **6 dedicated inputs including 4 clock pins**
- **No hidden delays**
- **High speed**
  - t_{MAX} = 83 MHz
  - t_{PD} = 15 ns
  - t_S = 10 ns
  - t_{CO} = 10 ns
- **Electrically alterable Flash technology**
- **Available in 160-pin PGA and TQFP packages**
- **Pin compatible with the CY7C375 and the CY7C378**

Functional Description

The CY7C376 is a Flash erasable Complex Programmable Logic Device (CPLD) and is part of the FLASH370™ family of high-density, high-speed CPLDs. Like all members of the FLASH370 family, the CY7C376 is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

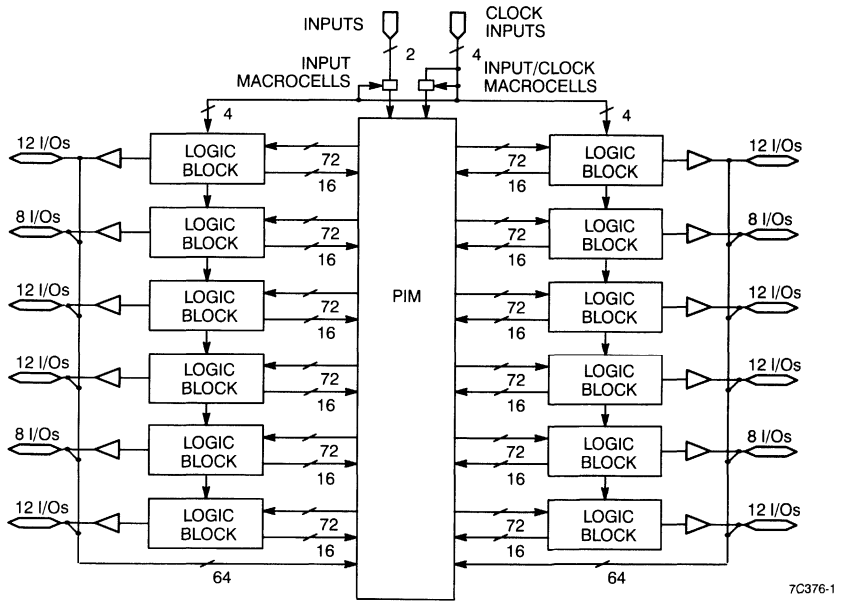
The 192 macrocells in the CY7C376 are divided between twelve logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370 family, the CY7C376 is rich in I/O resources. Two thirds of the macrocells in the device feature an associated I/O pin, resulting in 128 I/O pins on the CY7C376. In addition, there are two dedicated inputs and four input/clock pins.

Finally, the CY7C376 features a very simple timing model. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C376 remain the same.

Logic Block Diagram



Document #: 38-00225-A

FLASH370 is a trademark of Cypress Semiconductor.

192-Macrocell Flash CPLD

Features

- **192 macrocells in 12 logic blocks**
- **192 I/O pins**
- **6 dedicated inputs including 4 clock pins**
- **No hidden delays**
- **High speed**
  - f_{MAX} = 83 MHz
  - t_{PD} = 15 ns
  - t_S = 10 ns
  - t_{CO} = 10 ns
- **Electrically alterable Flash technology**
- **Available in 240-pin PGA , 208-pin PQFP, and 225-pin BGA packages**
- **Pin compatible with the CY7C379**

Functional Description

The CY7C377 is a Flash erasable Complex Programmable Logic Device (CPLD) and is part of the FLASH370™ family of high-density, high-speed CPLDs. Like all members of the FLASH370 family, the CY7C377 is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

The 192 macrocells in the CY7C377 are divided between 12 logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

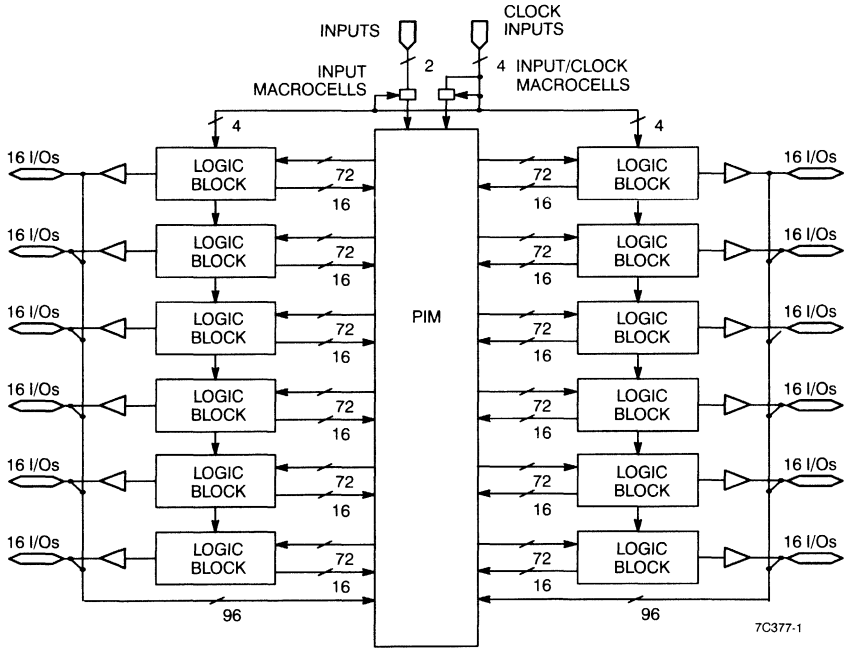
The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370 family, the CY7C377 is rich in I/O resources. Every macrocell in the device features an associated I/O pin, resulting in 192 I/O pins on the CY7C377. In addition, there are two dedicated inputs and four input/clock pins.

Finally, the CY7C377 features a very simple timing model. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C377 remain the same.

3

Logic Block Diagram



Document #: 38-00226-A

FLASH370 is a trademark of Cypress Semiconductor.

ADVANCED INFORMATION

CY7C378

256-Macrocell Flash CPLD

Features

- **256 macrocells in 16 logic blocks**
- **128 I/O pins**
- **6 dedicated inputs including 4 clock pins**
- **No hidden delays**
- **High speed**
  - f_{MAX} = 83 MHz
  - t_{PD} = 15 ns
  - t_S = 10 ns
  - t_{CO} = 10 ns
- **Electrically alterable Flash technology**
- **Available in 160-pin PGA and TQFP packages**
- **Pin compatible with the CY7C375 and the CY7C376**

Functional Description

The CY7C378 is a Flash erasable Complex Programmable Logic Device (CPLD) and is part of the FLASH370™ family of high-density, high-speed CPLDs. Like all members of the FLASH370 family, the CY7C378 is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

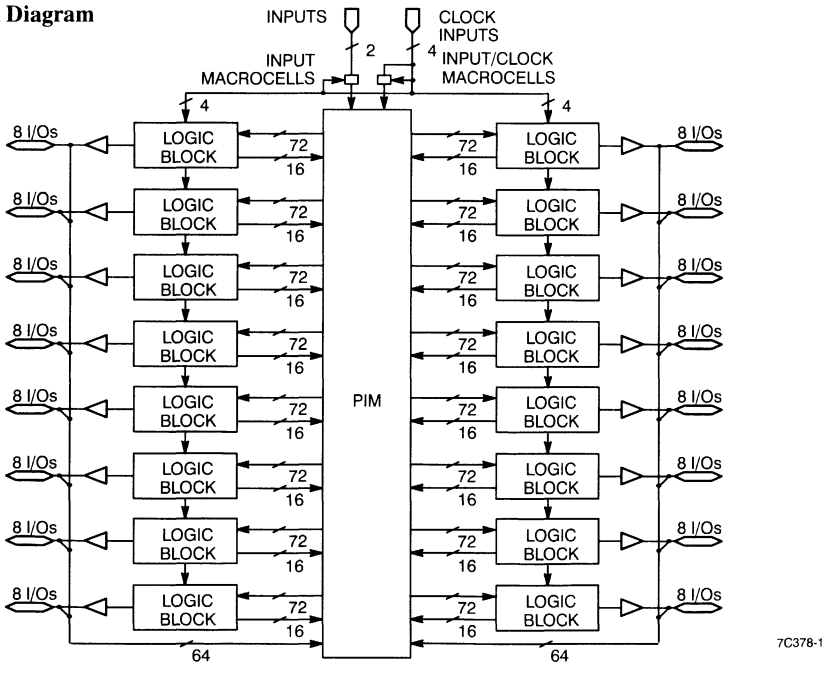
The 256 macrocells in the CY7C378 are divided between 16 logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370 family, the CY7C378 is rich in I/O resources. Every two macrocells in the device feature an associated I/O pin, resulting in 128 I/O pins on the CY7C378. In addition, there are two dedicated inputs and four input/clock pins.

Finally, the CY7C378 features a very simple timing model. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C378 remain the same.

Logic Block Diagram



Document #: 38-00368

FLASH370 is a trademark of Cypress Semiconductor.

CY7C379

256-Macrocell Flash CPLD

Features

- **256 macrocells in 16 logic blocks**
- **192 I/O pins**
- **6 dedicated inputs including 4 clock pins**
- **No hidden delays**
- **High speed**
  - f_{MAX} = 83 MHz
  - t_{PD} = 15 ns
  - t_S = 10 ns
  - t_{CO} = 10 ns
- **Electrically alterable Flash technology**
- **Available in 240-pin PGA, 208-pin PQFP, and 225-pin BGA packages**
- **Pin compatible with the CY7C377**

Functional Description

The CY7C379 is a Flash erasable Complex Programmable Logic Device (CPLD) and is part of the FLASH370™ family of high-density, high-speed CPLDs. Like all members of the FLASH370 family, the CY7C379 is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

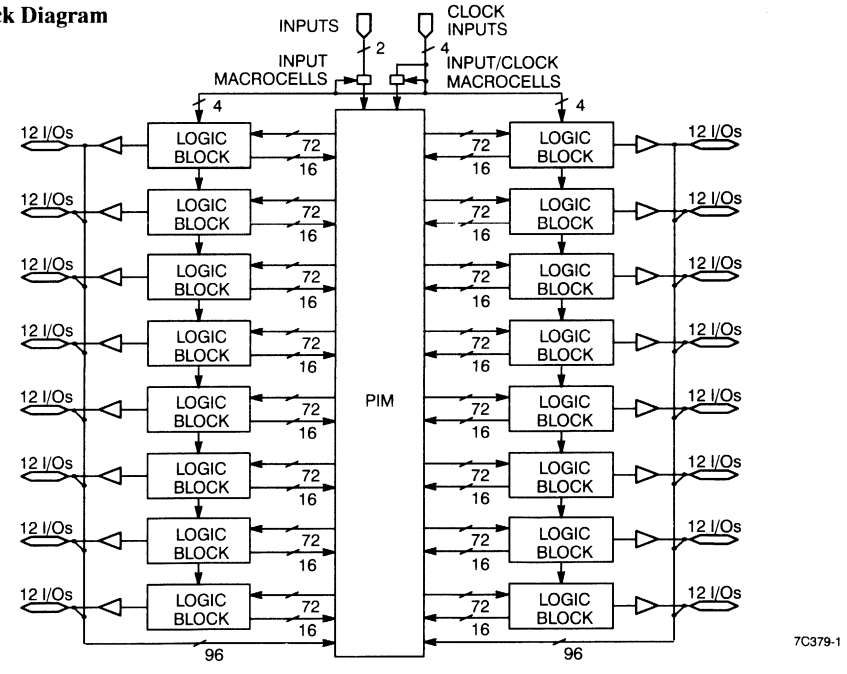
The 256 macrocells in the CY7C379 are divided between sixteen logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370 family, the CY7C379 is rich in I/O resources. Three quarters of the macrocells in the device feature an associated I/O pin, resulting in 192 I/O pins on the CY7C379. In addition, there are two dedicated inputs and four input/clock pins.

Finally, the CY7C379 features a very simple timing model. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C379 remain the same.

Logic Block Diagram



Document #: 38–00336

FLASH370 is a trademark of Cypress Semiconductor.

FPGAs 4

Section Contents

FPGAs (Field Programmable Gate Arrays)

pASIC380 Family

Very High Speed CMOS FPGAs

Features

- **Very high speed**
  - **Loadable counter frequencies greater than 100 MHz**
  - **Chip-to-chip operating frequencies up to 85 MHz**
  - **Input + logic cell + output delays under 9 ns**
- **High usable density**
  - **Up to 12,000 "gate array" gates, equivalent to 36,000 EPLD or LCA gates**
  - **Technology migration path to 20,000 gates and above**
- **Low power, high output drive**
  - **Standby current typically 2 mA**
  - **16-bit counter operating at 100 MHz consumes 50 mA**
  - **Minimum I_{OL} and I_{OH} of 8 mA**
- **Flexible FPGA architecture**
  - **Wide fan-in (up to 14 input gates)**
  - **Multiple outputs in each cell**
  - **Very low cell propagation delay (3.4 ns)**
- **Low-cost, easy-to-use design tools**
  - **Designs entered in VHDL, schematics, or both**
  - **Fast, fully automatic place and route**
  - **Waveform simulation with back annotated net delays**
  - **PC and workstation platforms**
- **Robust routing resources**
  - **Fully automatic place and route of designs using up to 100 percent of logic resources**
- **Input hysteresis provides high noise immunity**
- **Thorough testability**
  - **Built-in scan path permits 100 percent factory testing of logic and I/O cells**
  - **Automatic Test Vector Generation (ATVG) software supports user testing after programming**
- **CMOS process with ViaLink™ programming technology**
  - **High-speed metal-to-metal link**
  - **Non-volatile antifuse technology**

Functional Description

The pASIC380 Family of very high speed CMOS, user-programmable, ASIC devices is based on the first FPGA technology to combine high speed, high density, and low power in a single architecture.

All pASIC380 Family devices are based on an array of highly flexible logic cells that have been optimized for efficient implementation of high-speed arithmetic, counter, data path, state machine, and glue logic functions. Logic cells are configured and interconnected by rows and columns of routing metal lines and ViaLink metal-to-metal programmable-via interconnect elements.

ViaLink technology provides a non-volatile, permanently programmed custom logic function capable of operating at speeds of over 100 MHz. Internal logic cell delays are under 4 ns and total input to output combinatorial logic delays are under 10 ns. This permits high-density programmable devices to be used with today's fastest CISC and RISC microprocessors, while consuming a fraction of the power and board area of PALs™, GALs®, and discrete logic elements.

pASIC380 Family devices range in density from 1000 "gate array" gates (3,000 EPLD/LCA gates) in 44- and 68-pin packages to 12,000 (36,000) gates in 208- and 313-pin packages.

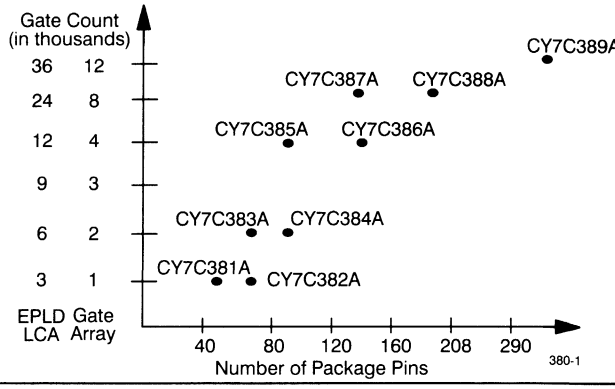
All devices share a common architecture and CAE design software to allow easy transfer of designs from one product to another. The small size of the ViaLink programming element insures a technology migration path to devices of 20,000 gates or more.

Designs are entered into the pASIC380 Family devices on PC or workstation platforms using third-party, general-purpose design-entry and simulation CAE packages, together with Cypress device-specific place and route and programming tools. Sufficient on-chip routing channels are provided to allow fully automatic place and route of designs using up to 100 percent of the available logic cells.

All the necessary hardware, software, documentation and accessories required to complete a design, from entering a schematic to programming a device are included in *Warp3*™ and *Impulse3*™, available from Cypress. *Warp3* includes a schematic capture system together with a waveform-based timing simulator. In addition to schematic entry, users can describe designs using VHDL. All applications run under Microsoft Windows® graphical user interface to insure a highly productive and easy-to-use design environment. Sun workstation UNIX™ platforms are also available.

4

pASIC380 Family Members



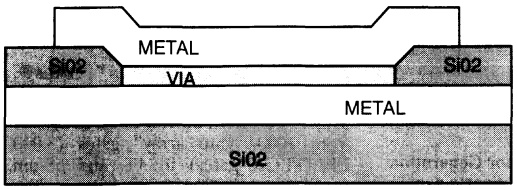


Figure 1. Unprogrammed ViaLink Element

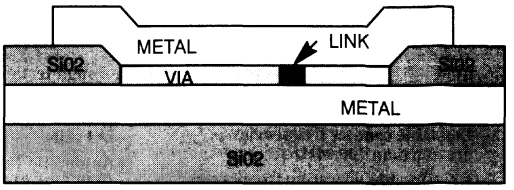


Figure 2. Programmed ViaLink Element

ViaLink Programming Element

Programmable devices implement customer-defined logic functions by interconnecting user-configurable logic cells through a variety of semiconductor switching elements. The maximum speed of operation is determined by the effective impedance of the switch in both programmed, ON, and unprogrammed, OFF, states.

In pASIC380 devices, the switch is called a ViaLink element. The ViaLink element is an antifuse formed in a via between the two layers of metal of a standard CMOS process. The direct metal-to-metal link created as a result of programming achieves a connection with resistance values as a low as 50 ohms. This is less than 5 percent of the resistance of an EPROM or SRAM switch and 10 percent of that of a dielectric antifuse. The capacitance of an unprogrammed ViaLink site is also lower than these alternative approaches. The resulting low RC time constant provides speeds two to three times faster than older generation technologies.

Figure 1 shows an unprogrammed ViaLink site. In a custom metal masked ASIC, such as a gate array, the top and bottom layers of metal make direct contact through the via. In a ViaLink programmable ASIC device, the two layers of metal are initially separated by an insulating semiconductor layer with resistance in excess of 1 gigaohm.

A programming pulse of 10 to 11 volts applied across the via forms a bidirectional conductive link connecting the top and bottom metal layers, as shown in *Figure 2*. The tight distribution of link resistance is shown in *Figure 3*.

Standard CMOS Process

pASIC380 devices are the first FPGA devices to be fabricated on a conventional high-volume CMOS process. The base technology is a 0.65-micron, n-well CMOS technology with a single polysilicon layer and two layers of metal interconnect. The only deviation from the standard process flow occurs when the ViaLink module is inserted between the metal deposition steps.

As the size of a ViaLink is identical to that of a standard metal interconnect via, programmable elements can be packed very densely. The microphotograph in *Figure 4* shows an array of ViaLink elements. The density is limited only by the minimum dimensions of the metal-line pitch. The current Cypress 0.65-micron process allows the development of pASIC380 devices with tens of thousands of usable gates.

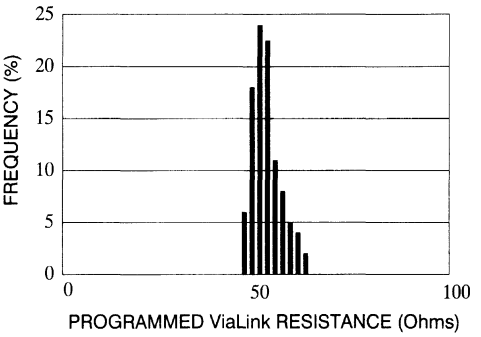


Figure 3. Distribution of Programmed Link Resistance

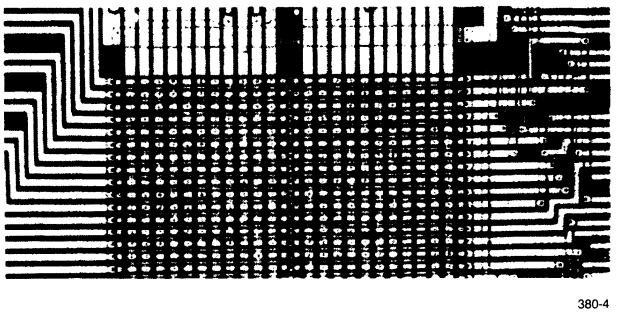


Figure 4. An Array of ViaLink Elements

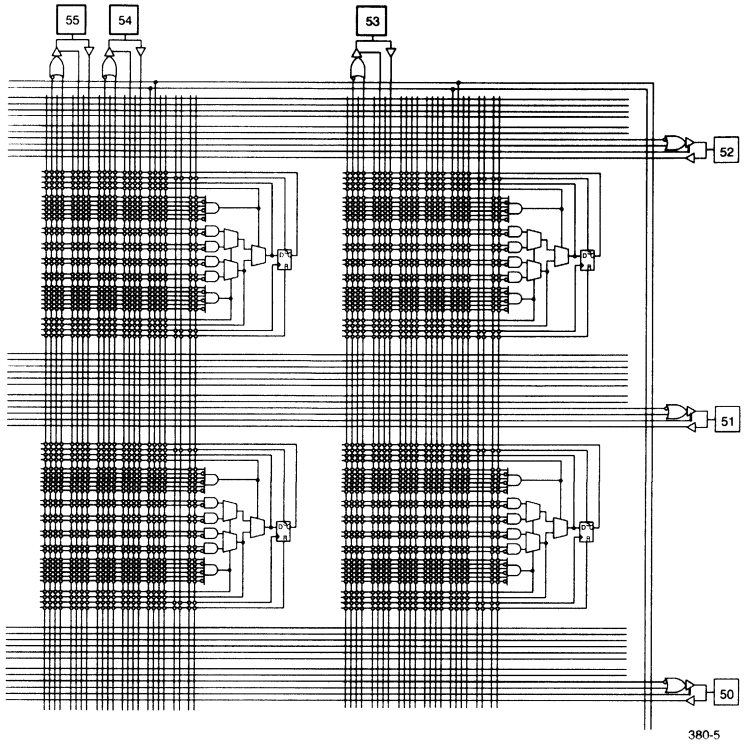


Figure 5. A Matrix of Logic Cells and Wiring Channels

The pASIC380 device architecture consists of an array of user-configurable logic building blocks, called logic cells. *Figure 5* shows a section of a pASIC380 device containing internal logic cells, input/output cells, and dual-layer vertical and horizontal metal routing channels. Through ViaLink elements located at the wire intersections, the output of any cell may be programmed to connect to the input of any other cell.

The regularity and orthogonality of this interconnect, together with the capability to achieve 100 percent routability of logic cells makes the pASIC380 architecture closer in structure and performance to a metal-masked gate array than any other FPGA family. It also makes system operating speed far less sensitive to partitioning and placement decisions, thus minor revisions to a logic design usually result in only small changes in performance. (See *Figure 6.*)

Organization

The pASIC380 Family of very high speed FPGAs contains devices covering a wide spectrum of I/O and density requirements.

The key features of all five pASIC380 devices are listed in *Table 1.* See the individual product datasheets for more specific information on each device.

Individual part numbers indicate unique logic cell and I/O cell combinations. For example, the CY7C383A contains 192 logic cells and 56 I/O cells in a 68-pin package. The CY7C384A also contains 192 logic cells, but it has 68 I/O cells and is packaged in 84- and 100-pin packages. Note that at each pASIC380 density there is a density upgrade available in the same package. In other words, the CY7C383A features 2,000 gates in the same pinout as the 1,000-gate CY7C382A. The same applies to the CY7C385A and CY7C384A.

Gate counts for pASIC380 devices are based on the number of usable or "gate array" gates. Each of the internal logic cells has a total logic capacity of up to 30 gates. As a typical application will use 10 to 12 of these gates, the usable gate count is significantly lower than the total number of available gates. On the pASIC380 product family, Cypress uses the more conservative usable (gate array) gate method of specifying density. Total available gate densities may also be specified as EPLD/LCA gates.

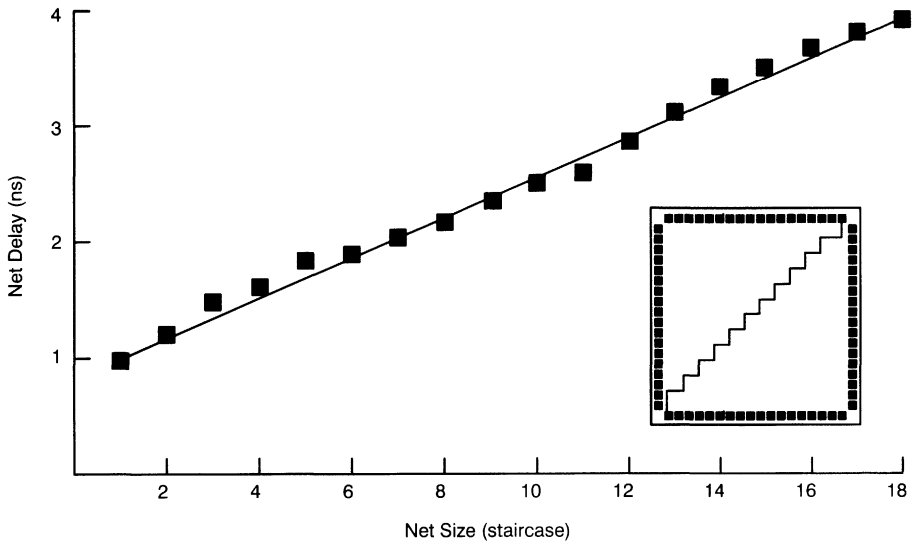


Figure 6. Net Delay vs. Net Size (4 ns "corner to corner")

Table 1. Key Features of pASIC380 Devices

Device	Logic Cells	I/O Cells	Dedicated Inputs	Usable Gates	EPLD/LCA Gates	Packages
7C381A	96	32	8	1000	3000	44-Pin PLCC
7C382A	96	56	8	1000	3000	68-Pin PLCC, PGA 100-Pin TQFP
7C383A	192	56	8	2000	6000	68-Pin PLCC, PGA
7C384A	192	68	8	2000	6000	84-Pin PLCC, PGA 100-Pin TQFP
7C385A	384	68	8	4000	12000	84-Pin PLCC, PGA 100-Pin TQFP
7C386A	384	114	8	4000	12000	144-Pin TQFP 145-Pin PGA 160-Pin CQFP
7C387A	768	114	8	8000	24000	144-Pin TQFP 145-Pin CPGA 160-Pin CQFP
7C388A	768	172	8	8000	24000	208-Pin PQFP, 208-Pin CQFP 245-Pin CPGA
7C389A	1152	200	8	12000	36000	313-Pin BGA 245-Pin CPGA

Shaded area contains advanced information.

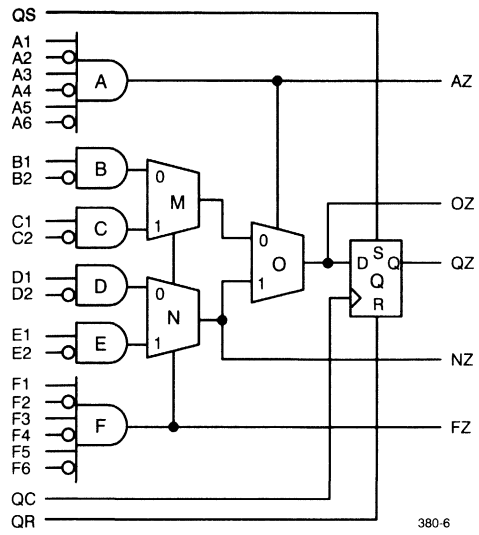


Figure 7. pASIC380 Internal Logic Cell

pASIC380 Internal Logic Cell

The pASIC380 internal logic cell, shown in *Figure 7*, is a general-purpose building block that can implement most TTL and gate array macro library functions. It has been optimized to maintain the inherent speed advantage of the ViaLink technology while insuring maximum logic flexibility.

The logic cell consists of two 6-input AND gates, four 2-input AND gates, three 2-to-1 multiplexers and a D flip-flop. As noted above, each cell represents approximately 30 gate-equivalents of logic capability. The pASIC380 logic cell is unique among FPGA architectures in that it offers up to 14-input-wide gating functions. It can implement all possible Boolean transfer functions of up to three variables as well as many functions of up to 14 variables.

Glitch-free switching of the multiplexer is insured because the internal capacitance of the circuit maintains enough charge to hold the output in a steady state during input transitions. The multiplexer output feeds the D-type flip-flop, which can also be configured to provide JK-, SR-, or T-type functions as well as count with carry-in. Two independent SET and RESET inputs can be used to asynchronously control the output condition. The combination of wide gating capability and a built-in register makes the pASIC380 logic cell particularly well suited to the design of high-speed state machines, shift registers, encoders, decoders, arbitration and arithmetic logic, as well as a wide variety of counters.

Each pASIC380 logic cell features five separate outputs. The existence of multiple outputs makes it easier to pack independent functions into a single logic cell. For example, if one function requires a single register, both 6-input AND gates (A and F) are available for other uses. Logic packing is accomplished automatically by *Warp3* software.

The function of a logic cell is determined by the logic levels applied to the inputs of the AND gates. ViaLink sites located on signal wires tied to the gate inputs perform the dual role of configuring the logic function of a cell and establishing connections between cells.

The pASIC380 macro library contains more than 200 of the most frequently used logic functions already optimized to fit the logic cell architecture. A detailed understanding of the logic cell is therefore not necessary to successfully design with pASIC380 devices. CAE tools will automatically translate a conventional logic schematic and/or VHDL source code into a device and provide excellent performance and utilization.

Three types of input and output structures are provided on pASIC380 devices to configure buffering functions at the external pads. They are called the Bidirectional Input/Output (I/O) cell, the Dedicated Input (I) cell, and the Clock/Dedicated Input (CLK/I) cell.

The bidirectional I/O cell, shown in *Figure 8*, consists of a 2-input OR gate connected to a pin buffer driver. The buffer output is controlled by a three-state enable line to allow the pad to also act as an input. The output may be configured as active HIGH, active LOW, or as an open drain inverting buffer.

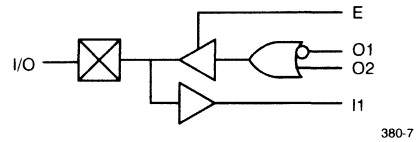


Figure 8. Bidirectional I/O Cell

The Dedicated Input cell, shown in *Figure 9*, conveys true and complement signals from the input pads into the array of logic cells. As these pads have nearly twice the current drive capability of the I/O pads, they are useful for distributing high fanout signals across the device.

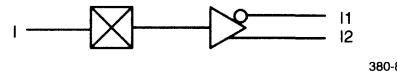


Figure 9. Dedicated Input High-Drive Cell

The Clock/Dedicated Input cell (*Figure 10*) drives a low-skew, fanout-independent clock tree that can connect to the clock, set, or reset inputs of the logic cell flip-flops. The CY7C384A, for example, has 68 I/O cells, 6 I cells, and 2 I/CLK cells.

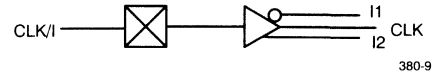


Figure 10. Clock/Dedicated Input Cell

pASIC380 Interconnect Structure

Multiple logic cells are joined together to form a complex logic function by interconnection through the routing channels. To describe the organization of these routing channels, a hypothetical 14-pin device consisting of two logic cells is shown in *Figure 11*. This device contains the same architectural features as the members of the pASIC380 family.

Active logic functions are performed by the internal logic cells, the I/O cells (pins 2, 3, 7, 9, 10, and 14) and the I cells (pins 4, 6, 11, and 13). These cells are connected with vertical and horizontal wiring channels.

Four types of signal wires are employed: segmented wires, quad wires, express wires, and clock wires. Segmented wires are predominantly used for local connections and have ViaLink elements known as a Cross Link (denoted by the open box symbol), at every crossover point. They may also be connected to the segmented wires of cells above and below through ViaLink elements, called Pass Links (denoted by the X symbol). Express lines are similar to segmented wires except that they are not divided by Pass Links. Quad Lines are a compromise between express and segmented lines. Dedicated clock wires are lightly loaded with only three links per cell to distribute high-speed clock edges to the flip-flop CLK, SET, and RESET inputs. Express wires may also be used to deliver clock signals into the multiplexer region of the cell for combinatorial gating. The automatic place and route software allocates signals to the appropriate wires to insure the optimum speed/density combination.

Vertical V_{CC} and GND wires are located close to the logic cell gate inputs to allow any input that is not driven by the output of another cell to be automatically tied to either V_{CC} or GND. All of the vertical wires (segmented, express, quad, clock, and power) considered as a group are called vertical channels. These channels span the full height of the device and run to the left of each column of logic cells.

Horizontal wiring channels, called rows, provide connections, via cross links, to other columns of logic cells and to the periphery of the chip. Appropriate programming of ViaLink elements allows electrical connection to be made from any logic cell output to the input of any other logic or I/O cell. Ample wires are provided in the channels to permit automatic place and route of many designs using up to 100 percent of the device logic cells. Designs can be completed automatically even with a high percentage of fixed user placement of internal cells and pin locations.

This information is presented to provide the user with insight into how a logic function is implemented in pASIC380 devices. However, it is not necessary to develop a detailed understanding of the architecture in order to achieve efficient designs. All routine tasks are fully automatic. No manual wire routing is necessary, nor is it permitted by the software. Fully automatic placement of logic functions is also offered. But if it is necessary to achieve a specific pin configuration or register alignment, for example, manual placement is supported.

Power Consumption

Typical standby power supply current consumption, I_{CC1}, of a pASIC380 device is 2 mA. The worst-case limit for standby current (I_{CC1}) over the full operating range of the pASIC380 devices is 10 mA. Formulas for calculating I_{CC} under AC conditions (I_{CC2}) are provided in the "pASIC380 Power vs. Operating Frequency" section of the Programmable Logic Data Book. As an example of the low-power consumption of pASIC380 devices, the 16-bit counter example detailed in the application note consumes just 50 mA at 100 MHz.

Programming and Testing

pASIC380 devices may be programmed and functionally tested on the Cypress *Impulse3* Programmer. Third-party programmers are also being qualified. See the third party tools section.

All pASIC380 devices have a built-in serial scan path linking the logic cell register functions (*Figure 12*). This is provided to improve factory test coverage and to permit testing by the user with automatically generated test vectors following programming.

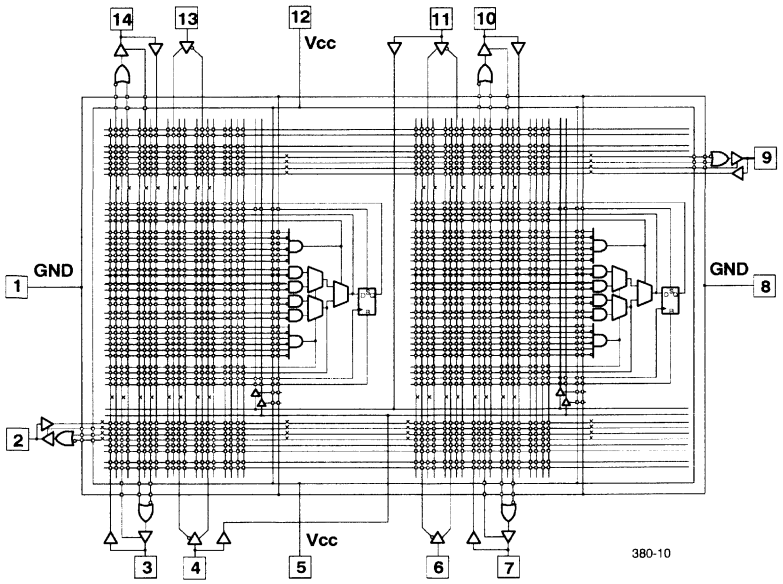


Figure 11. pASIC380 Device Features

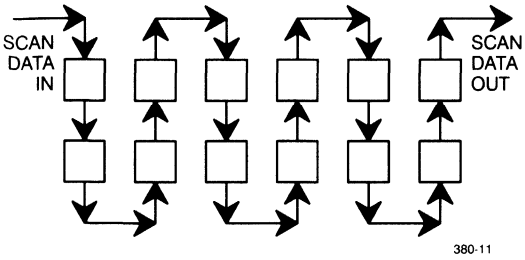


Figure 12. Internal Serial Scan Path

Automatic Test Vector Generation software is included in *Warp3*. The Programmer permits a high degree of test coverage to be achieved conveniently and rapidly using test vectors optimized for the pASIC380 architecture.

Reliability

The pASIC380 Family is based on a 0.65-micron high-volume CMOS fabrication process with the ViaLink programmable-via antifuse technology inserted between the metal deposition steps. The base CMOS process has been qualified to meet the requirements of MIL-STD-883B, Revision C.

The ViaLink element exists in one of two states: a highly resistive unprogrammed state, OFF, and the low-impedance, conductive state, ON. It is connected between the output of one logic cell and the inputs of other logic cells directly or through other links. No DC current flows through either a programmed or an unprogrammed link during operation as a logic device. An unprogrammed link sees a worst-case voltage equal to V_{CC} biased across its terminals. A programmed link carries AC current caused by charging and discharging of device and interconnect capacitances during switching.

Study of test structures and complete pASIC380 devices has shown that an unprogrammed link under V_{CC} bias remains in the unprogrammed state over time. Similar tests on programmed links under current bias exhibit the same stability. The long-term reliability of the combined CMOS and ViaLink structure is similar to that of the base gate array process. For further details, see the pASIC380 Family Reliability Report, contained in the reliability section of the Programmable Logic Data Book.

Document #: 38–00210–B

4

CY7C381A
CY7C382A

Very High Speed 1K (3K) Gate CMOS FPGA

Features

- **Very high speed**
  - **Loadable counter frequencies greater than 150 MHz**
  - **Chip-to-chip operating frequencies up to 120 MHz**
  - **Input + logic cell + output delays at 6.5 ns**
- **Unparalleled FPGA performance for counters, data path, state machines, arithmetic, and random logic**
- **High usable density**
  - **8 x 12 array of 96 logic cells provides 3,000 total available gates**
  - **1,000 typically usable "gate array" gates in 44- and 68-pin PLCC/CPGA packages, 100-pin TQFP**
- **Low power, high output drive**
  - **Standby current typically 2 mA**
  - **16-bit counter operating at 150 MHz consumes 50 mA**
  - **Minimum I_{OL} and I_{OH} of 8 mA**
- **Flexible logic cell architecture**
  - **Wide fan-in (up to 14 input gates)**
  - **Multiple outputs in each cell**
  - **Very low cell propagation delay (1.7 ns)**
- **Powerful design tools—*Warp3*™**
  - **Designs entered in VHDL, schematics, or both**
  - **Fast, fully automatic place and route**
  - **Waveform simulation with back annotated net delays**
  - **PC and workstation platforms**
- **Robust routing resources**
  - **Fully automatic place and route of designs using up to 100 percent of logic resources**
  - **No hand routing required**
- **32 (CY7C381A) to 56 (CY7C382A) bidirectional input/output pins**
- **6 dedicated input/high-drive pins**
- **2 clock/dedicated input pins with fan-out-independent, low-skew nets**
  - **Clock skew <1 ns**
- **Input hysteresis provides high noise immunity**
- **Thorough testability**
  - **Built-in scan path permits 100 percent factory testing of logic and I/O cells**
  - **Automatic Test Vector Generation (ATVG) software supports user testing after programming**
- **0.65µ CMOS process with ViaLink™ programming technology**
  - **High-speed metal-to-metal link**
  - **Non-volatile antifuse technology**
- **68-pin PLCC is compatible with EPLD 1800 and LCA 2064 industry-standard pinouts**
- **100-pin TQFP is pin compatible with CY7C384A and CY7C385A**

Functional Description

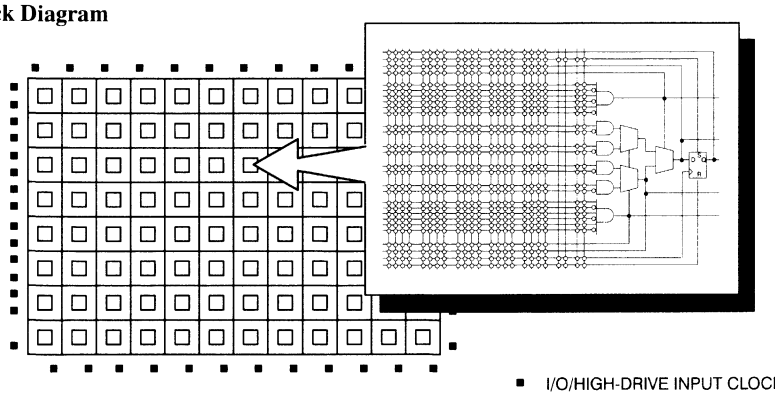
The CY7C381A and CY7C382A are very high speed CMOS user-programmable ASIC (pASIC™) devices. The 96 logic cell field-programmable gate array (FPGA) offers 1,000 typically usable "gate array" gates. This is equivalent to 3,000 EPLD or LCA gates. The CY7C381A is available in a 44-pin PLCC. The CY7C382A is available in a 68-pin PLCC and CPGA and a 100-pin TQFP.

Low-impedance, metal-to-metal ViaLink interconnect technology provides non-volatile custom logic capable of operating at speeds above 150 MHz with input delays under 1.5 ns and output delays under 3 ns. This permits high-density programmable devices to be used with today's fastest CISC and RISC microprocessors.

Designs are entered into the CY7C381A and CY7C382A using Cypress *Warp3* software or one of several third-party tools. *Warp3* is a sophisticated CAE package that features schematic entry, waveform-based timing simulation, and VHDL design synthesis. The CY7C381A and CY7C382A feature ample on-chip routing channels for fast, fully automatic place and route of high gate utilization designs.

For detailed information about the pASIC380 architecture, see the pASIC380 Family datasheet.

Logic Block Diagram



■ I/O/HIGH-DRIVE INPUT CLOCK CELLS

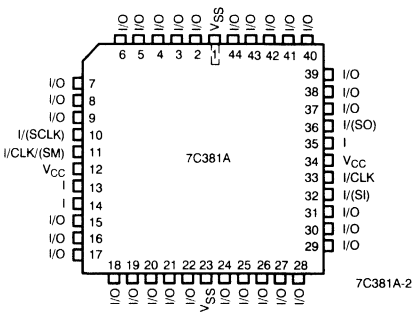
44, 68, or 100 PINS, INCLUDING 56 I/O CELLS, 6 INPUT HIGH-DRIVE CELLS, 2 INPUT/CLK (HIGH-DRIVE) CELLS

7C381A-1

ViaLink and pASIC are trademarks of QuickLogic Corporation.
Warp3 is a trademark of Cypress Semiconductor Corporation.

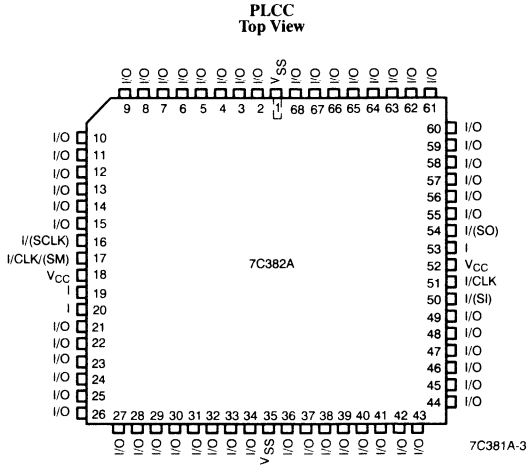
Pin Configurations

PLCC
Top View



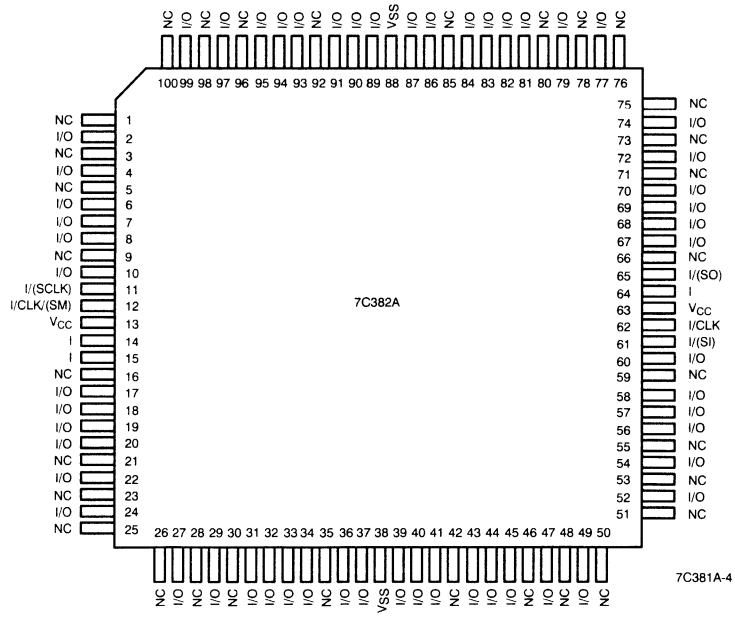
7C381A-2

PLCC
Top View



7C381A-3

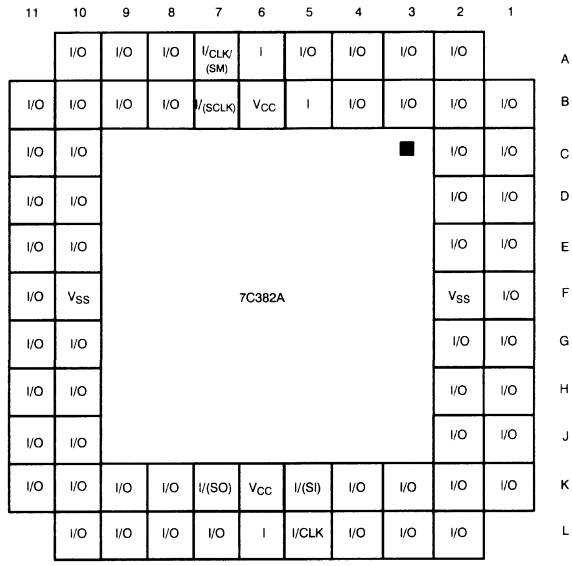
TQFP
Top View



7C381A-4

Pin Configurations (continued)

CPGA
Bottom View



7C381A-5

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature
Ceramic ..... − 65°C to +150°C
Plastic ..... −40°C to +125°C

Lead Temperature ..... 300°C

Supply Voltage ..... − 0.5V to +7.0V

Input Voltage ..... − 0.5V to V_{CC} +0.5V

ESD Pad Protection ..... ±2000 V

DC Input Voltage ..... −0.5V to 7.0V

Latch-Up Current ..... ±200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	−40°C to +85°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Delay Factor (K)

Speed Grade	Military		Industrial		Commercial	
	Min.	Max.	Min.	Max.	Min.	Max.
−0	0.39	1.82	0.4	1.67	0.46	1.55
−1	0.39	1.45	0.4	1.43	0.46	1.33
−2			0.4	1.35	0.46	1.25

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = − 4.0 mA	3.7		V
		I_{OH} = − 8.0 mA	2.4		V
		I_{OH} = − 10.0 µA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA Military/Industrial I_{OL} = 12 mA Commercial		0.4	V
		I_{OL} = 10.0 µA		0.1	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
I_I	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}	− 10	+10	µA
I_{OZ}	Output Leakage Current—Three-State	V_{IN} = V_{CC} or V_{SS}	− 10	+10	µA
I_{OS}	Output Short Circuit Current	V_{OUT} = V_{SS}	−10	− 80	mA
		V_{OUT} = V_{CC}	30	140	mA
I_{CC}	Standby Supply Current	V_{IN}, $V_{I/O}$ = V_{CC} or V_{SS}		10	mA

Capacitance

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance[1]	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		20	pF

Notes:
1. C_I = 20 pF max. on I/(SI).

Switching Characteristics Over the Operating Range

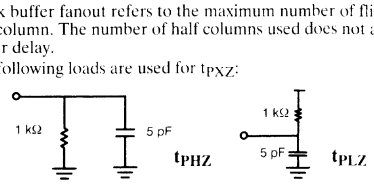
Parameter	Description	Propagation Delays[2] with Fanout of 1	2	3	4	8	Unit
LOGIC CELLS							
t_{PD}	Combinatorial Delay[3]	1.7	2.1	2.6	3.0	4.8	ns
t_{SU}	Set-Up Time[3]	2.1	2.1	2.1	2.1	2.1	ns
t_H	Hold Time	0.0	0.0	0.0	0.0	0.0	ns
t_{CLK}	Clock to Q Delay	1.0	1.5	1.9	2.3	4.2	ns
t_{CWHI}	Clock HIGH Time	2.0	2.0	2.0	2.0	2.0	ns
t_{CWLO}	Clock LOW Time	2.0	2.0	2.0	2.0	2.0	ns
t_{SET}	Set Delay	1.7	2.1	2.6	3.0	4.8	ns
t_{RESET}	Reset Delay	1.5	1.8	2.2	2.5	3.9	ns
t_{SW}	Set Width	1.9	1.9	1.9	1.9	1.9	ns
t_{RW}	Reset Width	1.8	1.8	1.8	1.8	1.8	ns

Parameter	Description	Propagation Delays[2] 1	2	3	4	6	8	Unit
INPUT CELLS								
t_{IN}	Input Delay (HIGH Drive)	2.1	2.2	2.3	2.4	2.6	2.9	ns
t_{INI}	Input, Inverting Delay (HIGH Drive)	2.1	2.2	2.3	2.5	2.8	3.1	ns
t_{IO}	Input Delay (Bidirectional Pad)	1.4	1.8	2.2	2.6	3.4	4.2	ns
t_{GCK}	Clock Buffer Delay[4]	2.7	2.7	2.8	2.9	3.0		ns
t_{GCKHI}	Clock Buffer Min. HIGH[4]	2.0	2.0	2.0	2.0	2.0		ns
t_{GCKLO}	Clock Buffer Min. LOW[4]	2.0	2.0	2.0	2.0	2.0		ns

Parameter	Description	Propagation Delays[2] with Output Load Capacitance (pF) of 30	50	75	100	150	Unit
OUTPUT CELLS							
t_{OUTLH}	Output Delay LOW to HIGH	2.7	3.4	4.2	5.0	6.7	ns
t_{OUTHL}	Output Delay HIGH to LOW	2.8	3.7	4.7	5.6	7.6	ns
t_{PZH}	Output Delay Three-State to HIGH	4.0	4.9	6.1	7.3	9.7	ns
t_{PZL}	Output Delay Three-State to LOW	3.6	4.2	5.0	5.8	7.3	ns
t_{PHZ}	Output Delay HIGH to Three-State[5]	2.9					ns
t_{PLZ}	Output Delay LOW to Three-State[5]	3.3					ns

Notes:

2. Worst-case propagation delay times over process variation at V_{CC} = 5.0V and T_A = 25°C. Multiply by the appropriate delay factor, K, for speed grade to get worst-case parameters over full V_{CC} and temperature range as specified in the operating range. All inputs are TTL with 3-ns linear transition time between 0 and 3 volts.
3. These limits are derived from worst-case values for a representative selection of the slowest paths through the pASIC logic cell including net delays. Guaranteed delay values for specific paths should be determined from simulation results.
4. Clock buffer fanout refers to the maximum number of flip-flops per half column. The number of half columns used does not affect clock buffer delay.
5. The following loads are used for t_{PXZ}:

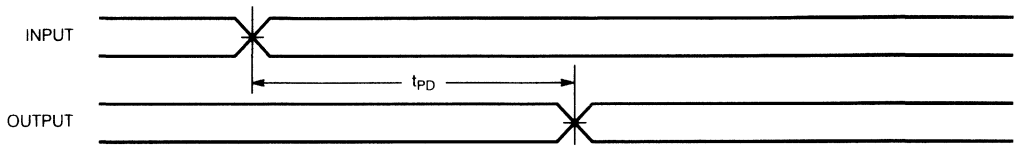


High Drive Buffer

Parameter	Description	# High Drives Wired Together	Propagation Delays[2] with Fanout of 12	24	48	72	96	Unit
t_{IN}	High Drive Input Delay	1	4.0	4.9				ns
		2		3.5	5.0			ns
		3			4.0	4.8	5.6	ns
		4				4.1	4.8	ns
t_{INI}	High Drive Input, Inverting Delay	1	4.2	5.1				ns
		2		3.7	5.2			ns
		3			4.2	5.0	5.8	ns
		4				4.3	5.0	ns

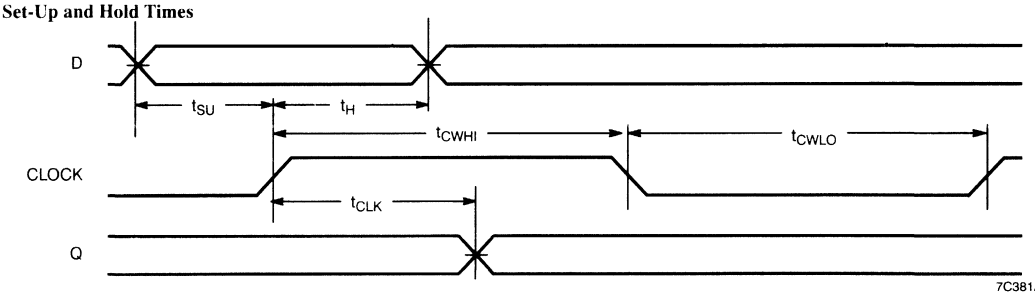
Switching Waveforms

Combinatorial Delay



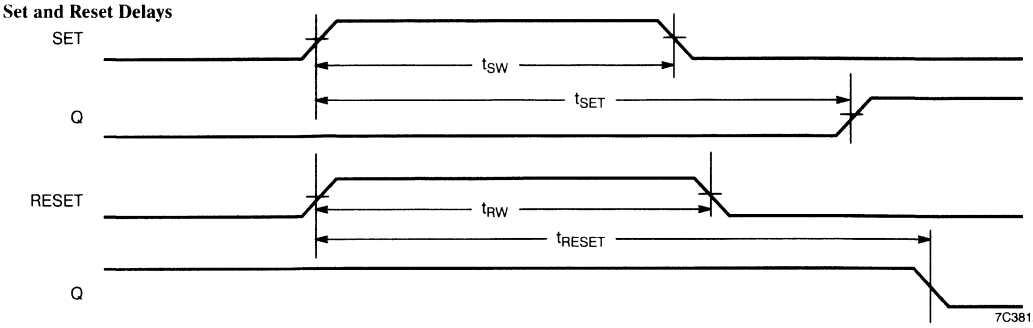
7C381A-6

Set-Up and Hold Times



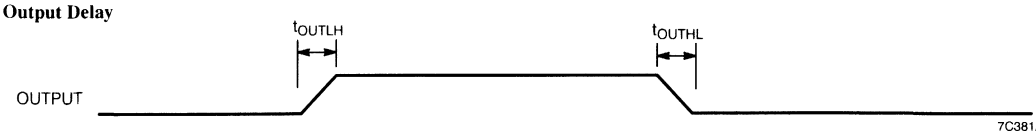
7C381A-7

Set and Reset Delays



7C381A-8

Output Delay



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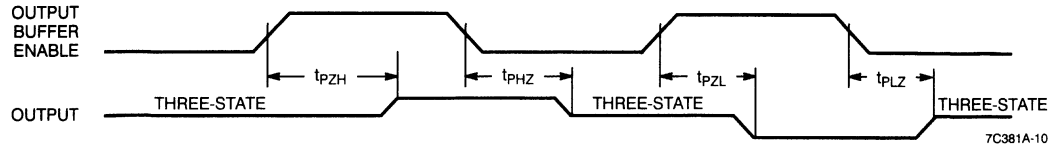
Switching Waveforms (continued)

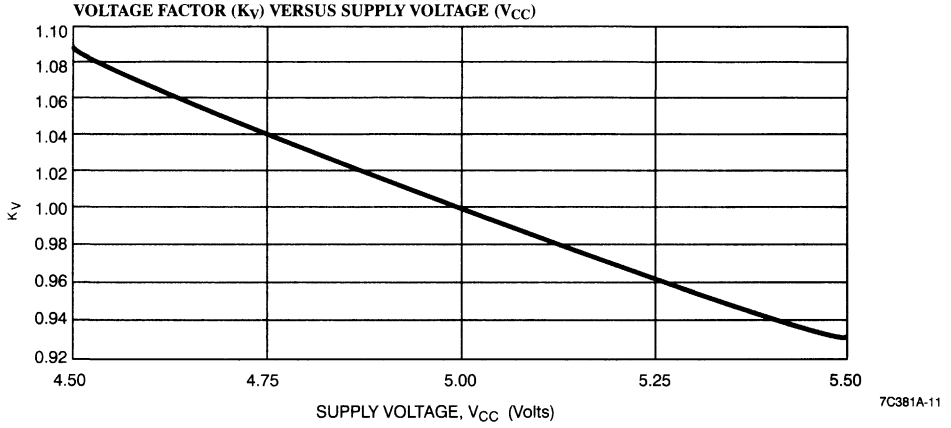
Three-State Delay



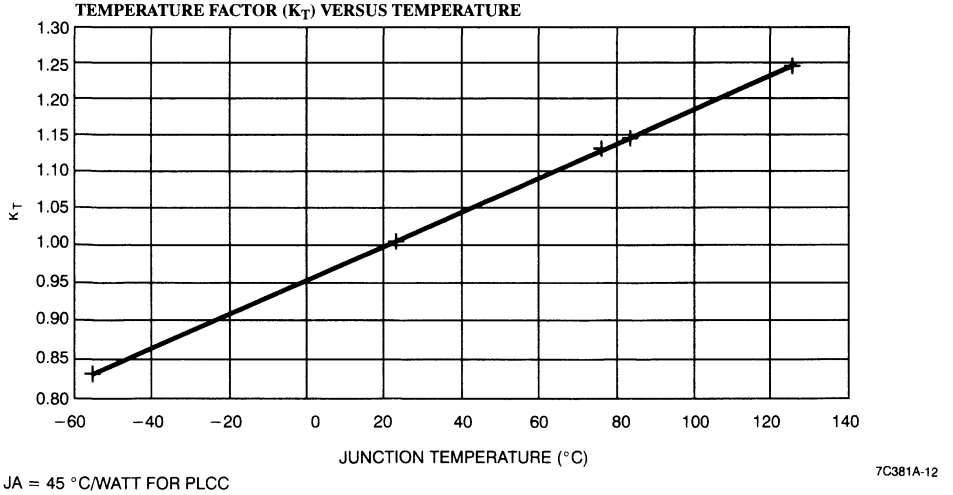
Typical AC Characteristics

Propagation delays depend on routing, fan-out, load capacitance, supply voltage, junction temperature, and process variation. The AC Characteristics are a design guide to provide initial timing estimates at nominal conditions. Worst-case estimates are obtained when nominal propagation delays are multiplied by the appropriate Delay Factor, K, as specified by the speed grade in the Delay Factor table. The effects of voltage and temperature variation are illustrated in the graphs below. *Warp3* incorporates datasheet AC Characteristics into the design database for pre-place-and-route simulations. The *Warp3* Delay Modeler extracts specific timing parameters for precise simulation results following place and route.

VOLTAGE FACTOR (K_V) VERSUS SUPPLY VOLTAGE (V_{CC})

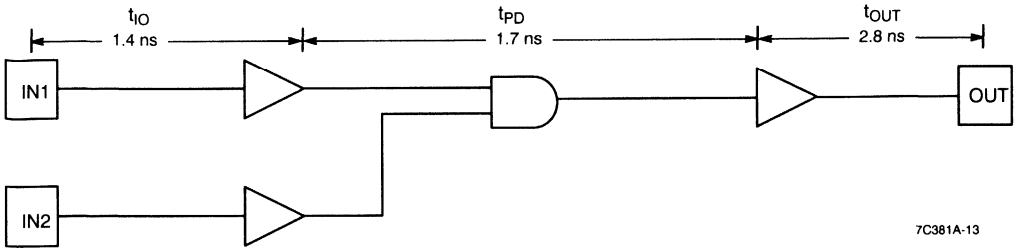


TEMPERATURE FACTOR (K_T) VERSUS TEMPERATURE



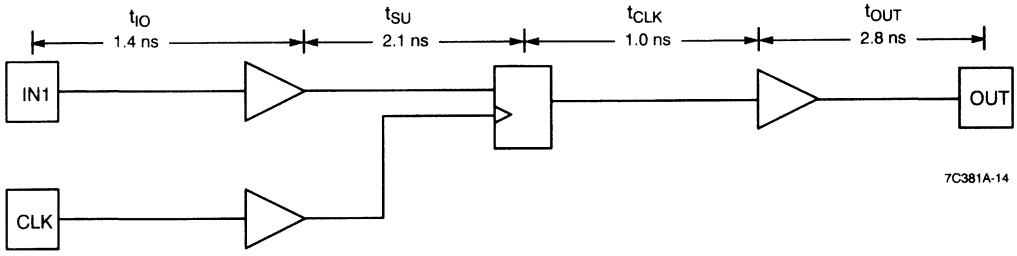
*THETA JA = 45 °C/WATT FOR PLCC

Combinatorial Delay Example (Load = 30 pF)



INPUT DELAY + COMBINATORIAL DELAY + OUTPUT DELAY = 5.9 ns

Sequential Delay Example (Load = 30 pF)



INPUT DELAY + REG SET-UP + CLOCK TO OUTPUT + OUTPUT DELAY = 7.3 ns

4

Ordering Information

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
2	CY7C381A–2JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C381A–2JI	J67	44-Lead Plastic Leaded Chip Carrier	Industrial
1	CY7C381A–1JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C381A–1JI	J67	44-Lead Plastic Leaded Chip Carrier	Industrial
0	CY7C381A–0JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C381A–0JI	J67	44-Lead Plastic Leaded Chip Carrier	Industrial

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
2	CY7C382A–2AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C382A–2GC	G69	69-Pin Grid Array (Cavity Down)	
	CY7C382A–2JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C382A–2AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C382A–2GI	G69	69-Pin Grid Array (Cavity Down)	
	CY7C382A–2JI	J81	68-Lead Plastic Leaded Chip Carrier	
1	CY7C382A–1AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C382A–1GC	G69	69-Pin Grid Array (Cavity Down)	
	CY7C382A–1JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C382A–1AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C382A–1GI	G69	69-Pin Grid Array (Cavity Down)	
	CY7C382A–1JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C382A–1GMB	G69	69-Pin Grid Array (Cavity Down)	Military
0	CY7C382A–0AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C382A–0GC	G69	69-Pin Grid Array (Cavity Down)	
	CY7C382A–0JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C382A–0AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C382A–0GI	G69	69-Pin Grid Array (Cavity Down)	
	CY7C382A–0JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C382A–0GMB	G69	69-Pin Grid Array (Cavity Down)	Military

Shaded area contains advanced information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Document #: 38–00253

PRELIMINARY

CY7C3381A
CY7C3382A

3.3V High Speed 1K (3K) Gate CMOS FPGA

Features

- 3.3V power supply
- Very high speed
  - Loadable counter frequencies greater than 100 MHz at 3.3V
  - Chip-to-chip operating frequencies up to 80 MHz
- Unparalleled FPGA performance for counters, data path, state machines, arithmetic, and random logic
- Low power
  - Standby current typically 1 mA
  - 16-bit counter operating at 100 MHz consumes 25 mA
- High usable density
  - 8 x 12 array of 96 logic cells provides 3,000 total available gates
  - 1,000 typically usable "gate array" gates in 44- and 68-pin PLCC, 69-pin CPGA, and 100-pin TQFP packages
- Flexible logic cell architecture
  - Wide fan-in (up to 14 input gates)
  - Multiple outputs in each cell
  - Very low cell propagation delay
- Powerful design tools—*Warp3*™
  - Designs entered in VHDL, schematics, or both
  - Fast, fully automatic place and route
  - Waveform simulation with back-annotated net delays
  - PC and workstation platforms
- Robust routing resources
  - Fully automatic place and route of designs using up to 100 percent of logic resources
  - No hand routing required
- 32 (CY7C3381A) to 56 (CY7C3382A) bidirectional input/output pins
- 6 dedicated input/high-drive pins
- 2 clock/dedicated input pins with fan-out-independent, low-skew nets
  - Clock skew <1 ns
- Input hysteresis provides high noise immunity
- Thorough testability
  - Built-in scan path permits 100 percent factory testing of logic and I/O cells
  - Automatic Test Vector Generation (ATVG) software supports user testing after programming
- 0.65μ CMOS process with ViaLink™ programming technology
  - High-speed metal-to-metal link
  - Non-volatile antifuse technology
- 68-pin PLCC is compatible with EPLD 1800 and LCA 2064 industry-standard pinouts

Functional Description

The CY7C3381A and CY7C3382A are 3.3V very high speed CMOS user-programmable ASIC (pASIC™) devices. The 96 logic cell field-programmable gate array (FPGA) offers 1,000 typically usable "gate array" gates. This is equivalent to 3,000 EPLD or LCA gates. The CY7C3381A is available in a 44-pin PLCC. The CY7C3382A is available in a 68-pin PLCC and CPGA and a 100-pin TQFP.

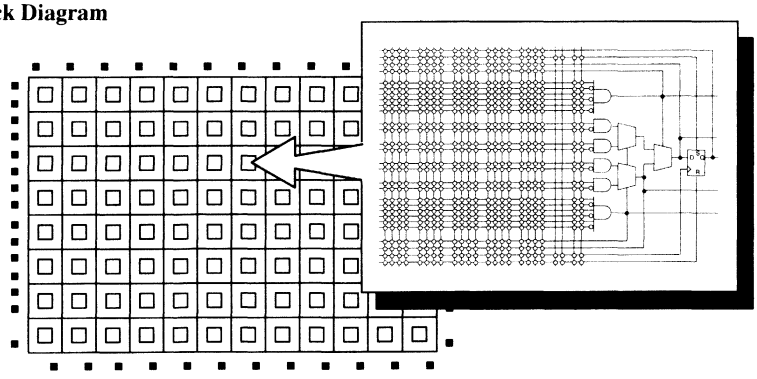
Low-impedance, metal-to-metal ViaLink interconnect technology provides non-volatile custom logic capable of operating at speeds above 100 MHz. This permits high-density programmable devices to be used with today's fastest CISC and RISC microprocessors.

Designs are entered into the CY7C3381A and CY7C3382A using Cypress *Warp3* software or one of several third-party tools. *Warp3* is a sophisticated CAE package that features schematic entry, waveform-based timing simulation, and VHDL design synthesis. The CY7C3381A and CY7C3382A feature ample on-chip routing channels for fast, fully automatic place and route of high gate utilization designs.

For detailed information about the pASIC380 architecture, see the pASIC380 Family datasheet.

4

Logic Block Diagram



■ I/O/HIGH-DRIVE INPUT CLOCK CELLS

44, 68, or 100 PINS, INCLUDING 56 I/O CELLS, 6 INPUT HIGH-DRIVE CELLS, 2 INPUT/CLK (HIGH-DRIVE) CELLS 7c3381A-1

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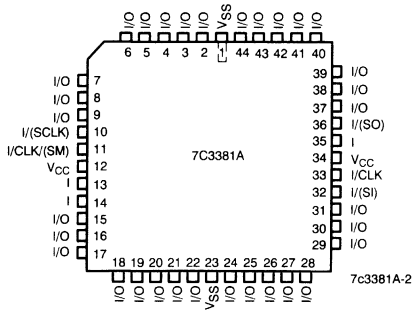
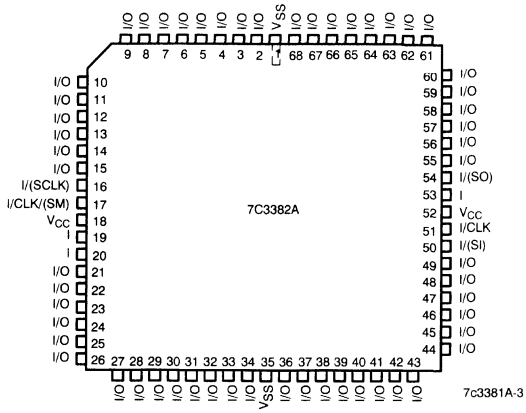
Warp3 is a trademark of Cypress Semiconductor Corporation..

Pin Configurations

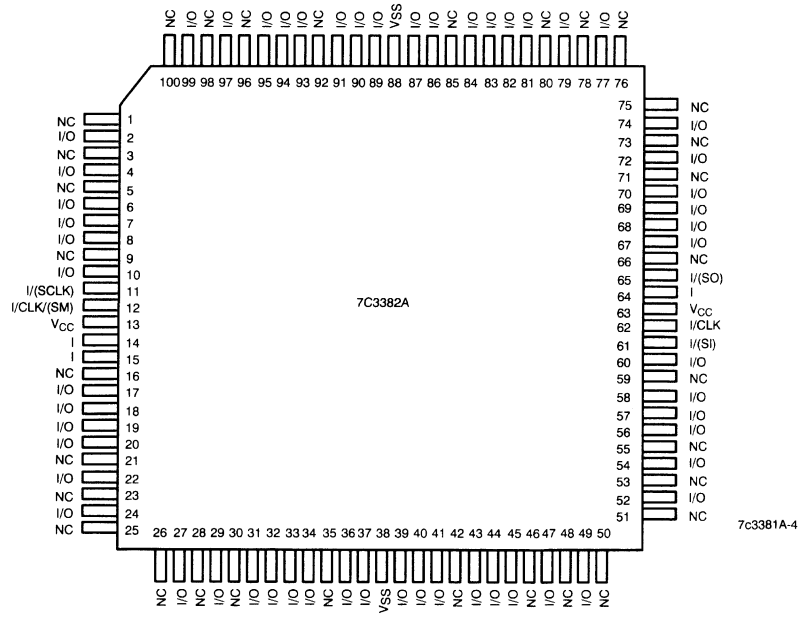
PLCC
Top View



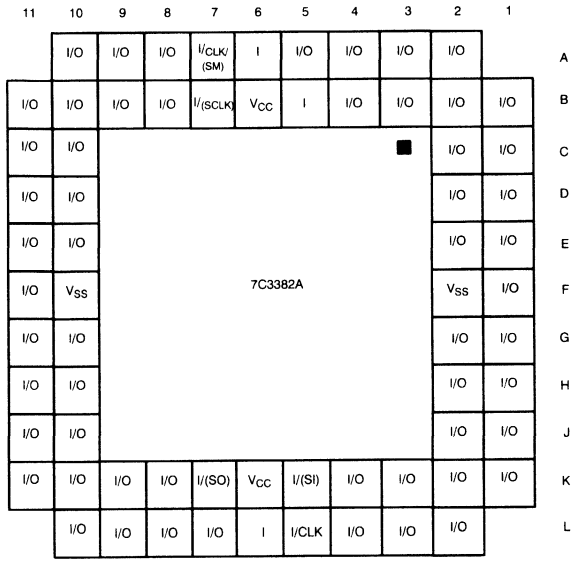
PLCC
Top View



TQFP
Top View



CPGA
Bottom View



7c3381A-5

4

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature
Ceramic ..... −65°C to +150°C
Plastic ..... −40°C to +125°C
Lead Temperature ..... 300°C
Supply Voltage ..... −0.5V to +7.0V
Input Voltage ..... −0.5V to V_{CC} +0.5V
ESD Pad Protection ..... ±2000 V
DC Input Voltage ..... −0.5V to 7.0V
Latch-Up Current ..... ±200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 0.3V

Delay Factor (K)

Speed Grade	Commercial	
	Min.	Max.
−0	0.65	2.90
−1	0.65	2.49

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −4.0 mA	2.4		V
		I_{OH} = −10.0 µA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA		0.4	V
		I_{OL} = 10.0 µA		0.1	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
I_I	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}	−10	+10	µA
I_{OZ}	Output Leakage Current	V_{IN} = V_{CC} or V_{SS}	−10	+10	µA
I_{OS}	Output Short Circuit Current	V_{OUT} = V_{SS}	−10	−80	mA
		V_{OUT} = V_{CC}	30	140	mA
I_{CC}	Standby Supply Current	V_{IN}, $V_{I/O}$ = V_{CC} or V_{SS}		2	mA

Capacitance

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance[1]	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	10	pF
C_{OUT}	Output Capacitance		20	pF

Notes:
1. C_I = 20 pF max. on I/(SI).

Switching Characteristics Over the Operating Range

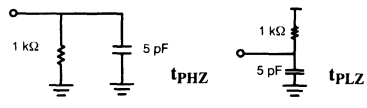
Parameter	Description	Propagation Delays[2] with Fanout of 1	2	3	4	8	Unit
LOGIC CELLS							
t_{PD}	Combinatorial Delay[3]	1.7	2.1	2.6	3.0	4.8	ns
t_{SU}	Set-Up Time[3]	2.1	2.1	2.1	2.1	2.1	ns
t_H	Hold Time	0.0	0.0	0.0	0.0	0.0	ns
t_{CLK}	Clock to Q Delay	1.0	1.5	1.9	3.3	4.2	ns
t_{CWHI}	Clock HIGH Time	2.0	2.0	2.0	2.0	2.0	ns
t_{CWLO}	Clock LOW Time	2.0	2.0	2.0	2.0	2.0	ns
t_{SET}	Set Delay	1.7	2.1	2.6	3.0	4.8	ns
t_{RESET}	Reset Delay	1.5	1.8	2.2	2.5	3.9	ns
t_{SW}	Set Width	1.9	1.9	1.9	1.9	1.9	ns
t_{RW}	Reset Width	1.8	1.8	1.8	1.8	1.8	ns

Parameter	Description	Propagation Delays 1	2	3	4	6	8	Unit
INPUT CELLS								
t_{IN}	Input Delay (HIGH Drive)	2.1	2.2	2.3	2.4	2.6	2.9	ns
t_{INI}	Input, Inverting Delay (HIGH Drive)	2.1	2.2	2.3	2.5	2.8	3.1	ns
t_{IO}	Input Delay (Bidirectional Pad)	1.4	1.8	2.2	2.6	3.4	4.2	ns
t_{GCK}	Clock Buffer Delay[4]	2.7	2.7	2.8	2.9	3.0	3.9	ns
t_{GCKHI}	Clock Buffer Min. HIGH[4]	2.0	2.0	2.0	2.0	2.0		ns
t_{GCKLO}	Clock Buffer Min. LOW[4]	2.0	2.0	2.0	2.0	2.0		ns

Parameter	Description	Propagation Delays[2] with Output Load Capacitance (pF) of 30	50	75	100	150	Unit
OUTPUT CELLS							
t_{OUTLH}	Output Delay LOW to HIGH	2.7	3.4	4.2	5.0	6.7	ns
t_{OUTHL}	Output Delay HIGH to LOW	2.8	3.7	4.7	5.6	7.6	ns
t_{PZH}	Output Delay Three-State to HIGH	4.0	4.9	6.1	7.3	9.7	ns
t_{PZL}	Output Delay Three-State to LOW	3.6	4.2	5.0	5.8	7.3	ns
t_{PHZ}	Output Delay HIGH to Three-State[5]	2.9					ns
t_{PLZ}	Output Delay LOW to Three-State[5]	3.3					ns

Notes:

2. Worst-case propagation delay times over process variation at V_{CC} = 3.3V and T_A = 25°C. Multiply by the appropriate delay factor, K, for speed grade to get worst-case parameters over full V_{CC} and temperature range as specified in the operating range. All inputs are TTL with 3-ns linear transition time between 0 and 3 volts.
3. These limits are derived from worst-case values for a representative selection of the slowest paths through the pASIC logic cell including net delays. Guaranteed delay values for specific paths should be determined from simulation results.
4. Clock buffer fanout refers to the maximum number of flip-flops per half column. The number of half columns used does not affect clock buffer delay.
5. The following loads are used for t_{PXZ}:



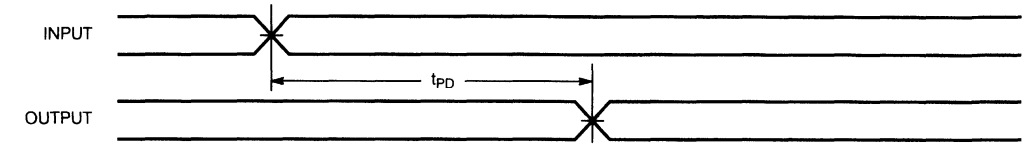
4

High Drive Buffer

Parameter	Description	# High Drives Wired Together	Propagation Delays[2] with Fanout of 12	24	48	72	96	Unit
t_{IN}	High Drive Input Delay	1	4.0	4.9				ns
		2		3.5	5.0			ns
		3			4.0	4.8	5.6	ns
		4				4.1	4.8	ns
t_{INI}	High Drive Input, Inverting Delay	1	4.2	5.1				ns
		2		3.7	5.2			ns
		3			4.2	5.0	5.8	ns
		4				4.3	5.0	ns

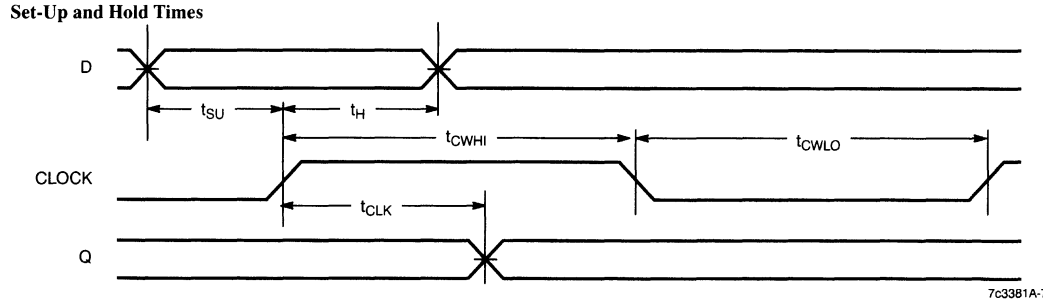
Switching Waveforms

Combinatorial Delay



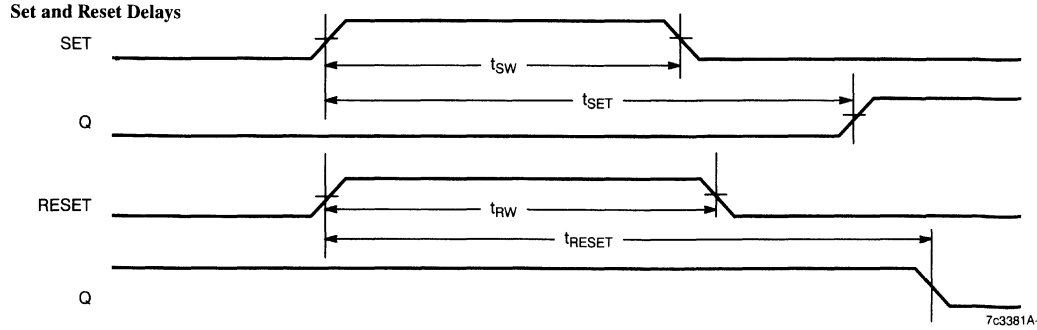
7c3381A-6

Set-Up and Hold Times



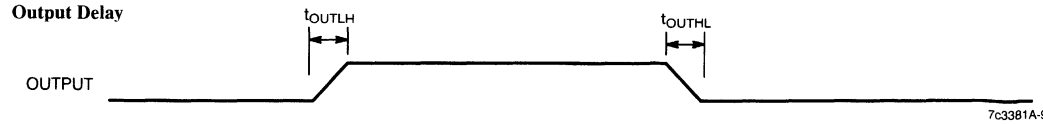
7c3381A-7

Set and Reset Delays



7c3381A-8

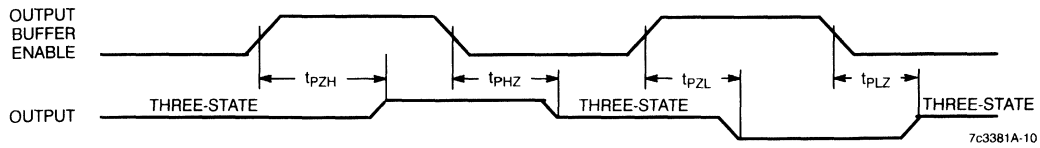
Output Delay



7c3381A-9

Switching Waveforms (continued)

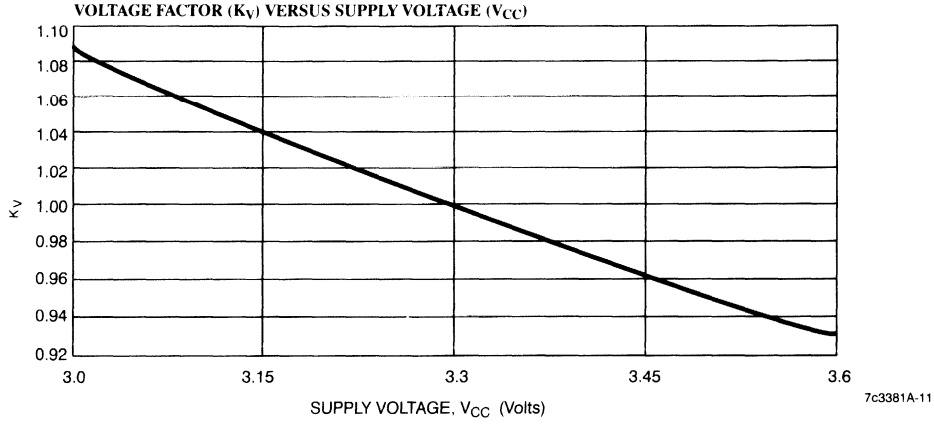
Three-State Delay



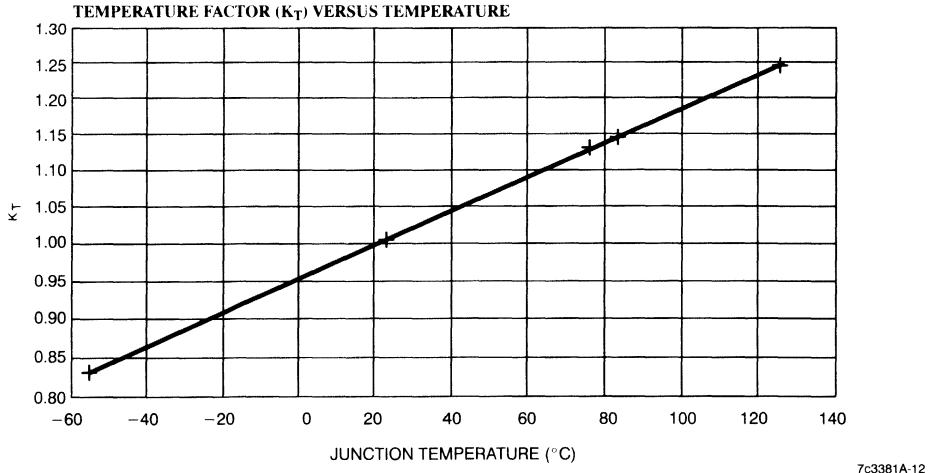
Typical AC Characteristics

Propagation delays depend on routing, fan-out, load capacitance, supply voltage, junction temperature, and process variation. The AC Characteristics are a design guide to provide initial timing estimates at nominal conditions. Worst-case estimates are obtained when nominal propagation delays are multiplied by the appropriate Delay Factor, K, as specified by the speed grade in the Delay Factor table. The effects of voltage and temperature variation are illustrated in the graphs below. *Warp3* incorporates datasheet AC Characteristics into the design database for pre-place-and-route simulations. The *Warp3* Delay Modeler extracts specific timing parameters for precise simulation results following place and route.

VOLTAGE FACTOR (K_V) VERSUS SUPPLY VOLTAGE (V_{CC})



TEMPERATURE FACTOR (K_T) VERSUS TEMPERATURE



*THETA JA = 45 °C/WATT FOR PLCC

Ordering Information

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
1	CY7C3381A–1JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
0	CY7C3381A–0JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
1	CY7C3382A–1AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C3382A–1GC	G69	69-Pin Grid Array (Cavity Down)	
	CY7C3382A–1JC	J81	68-Lead Plastic Leaded Chip Carrier	
0	CY7C3382A–0AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C3382A–0GC	G69	69-Pin Grid Array (Cavity Down)	
	CY7C3382A–0JC	J81	68-Lead Plastic Leaded Chip Carrier	

Document #: 38–00252

CY7C383A
CY7C384A

Very High Speed 2K (6K) Gate CMOS FPGA

Features

- Very high speed
  - Loadable counter frequencies greater than 150 MHz
  - Chip-to-chip operating frequencies up to 85 MHz
  - Input + logic cell + output delays under 9 ns
- Unparalleled FPGA performance for counters, data path, state machines, arithmetic, and random logic
- High usable density
  - 12 x 16 array of 192 logic cells provides 6,000 total available gates
  - 2,000 typically usable "gate array" gates in 68- and 84-pin PLCC, 84-pin CPGA, and 100-pin TQFP packages
- Low power, high output drive
  - Standby current typically 2 mA
  - 16-bit counter operating at 100 MHz consumes 50 mA
  - Minimum I_{OL} of 12 mA and I_{OH} of 8 mA
- Flexible logic cell architecture
  - Wide fan-in (up to 14 input gates)
  - Multiple outputs in each cell
  - Very low cell propagation delay (1.7 ns)
- Powerful design tools—*Warp3*™
  - Designs entered in VHDL, schematics, or both
  - Fast, fully automatic place and route
  - Waveform simulation with back annotated net delays
  - PC and workstation platforms
- Robust routing resources
  - Fully automatic place and route of designs using up to 100 percent of logic resources
  - No hand routing required
- 56 (CY7C383A) to 68 (CY7C384A) bidirectional input/output pins
- 6 dedicated input/high-drive pins
- 2 clock/dedicated input pins with fan-out-independent, low-skew nets
  - Clock skew <1 ns
- Input hysteresis provides high noise immunity
- Thorough testability
  - Built-in scan path permits 100 percent factory testing of logic and I/O cells
  - Automatic Test Vector Generation (ATVG) software supports user testing after programming
- CMOS process with ViaLink™ programming technology
  - High-speed metal-to-metal link
  - Non-volatile antifuse technology
- 68-pin PLCC is compatible with CY7C382A footprint for easy upgrade
- 84-pin PLCC is compatible with ACT1020 power supply and ground pinouts

Functional Description

The CY7C383A and CY7C384A are very high speed CMOS user-programmable ASIC (pASIC™) devices. The 192 logic cell field-programmable gate array (FPGA) offers 2,000 typically usable "gate array" gates. This is equivalent to 6,000 EPLD or LCA gates. The CY7C383A is available in a 68-pin PLCC. The CY7C384A is available in an 84-pin PLCC and CPGA and 100-pin TQFP.

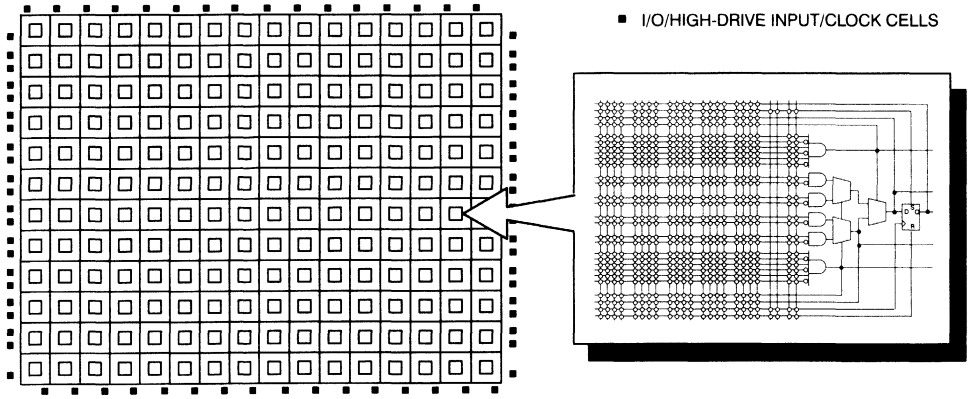
Low-impedance, metal-to-metal ViaLink interconnect technology provides non-volatile custom logic capable of operating at speeds above 150 MHz with input delays under 1.5 ns and output delays under 3 ns. This permits high-density programmable devices to be used with today's fastest CISC and RISC microprocessors.

Designs are entered into the CY7C383A and CY7C384A using Cypress *Warp3* software or one of several third-party tools. *Warp3* is a sophisticated CAE package that features schematic entry, waveform-based timing simulation, and VHDL design synthesis. The CY7C383A and CY7C384A feature ample on-chip routing channels for fast, fully automatic place and route of high gate utilization designs.

For detailed information about the pASIC380 architecture, see the pASIC380 Family datasheet.

4

Logic Block Diagram



68 or 84 PINS, INCLUDING 68 I/O CELLS, 6 INPUT HIGH-DRIVE CELLS, 2 INPUT/CLK (HIGH-DRIVE) CELLS c383A-1

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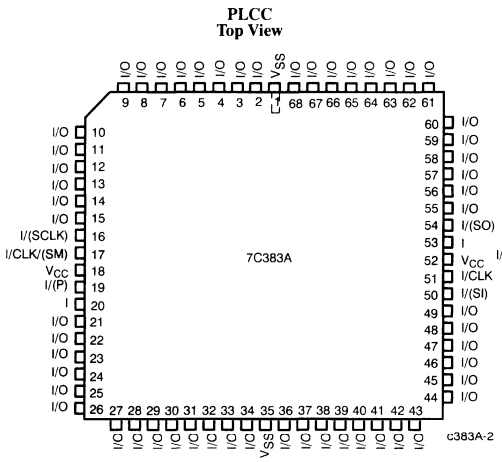
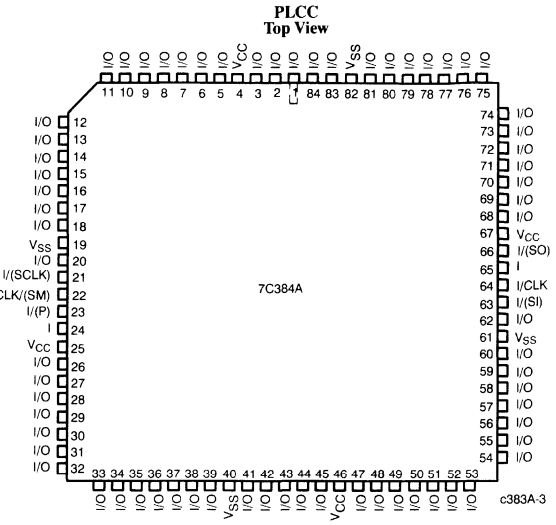
Warp3 is a trademark of Cypress Semiconductor Corporation.

Pin Configurations

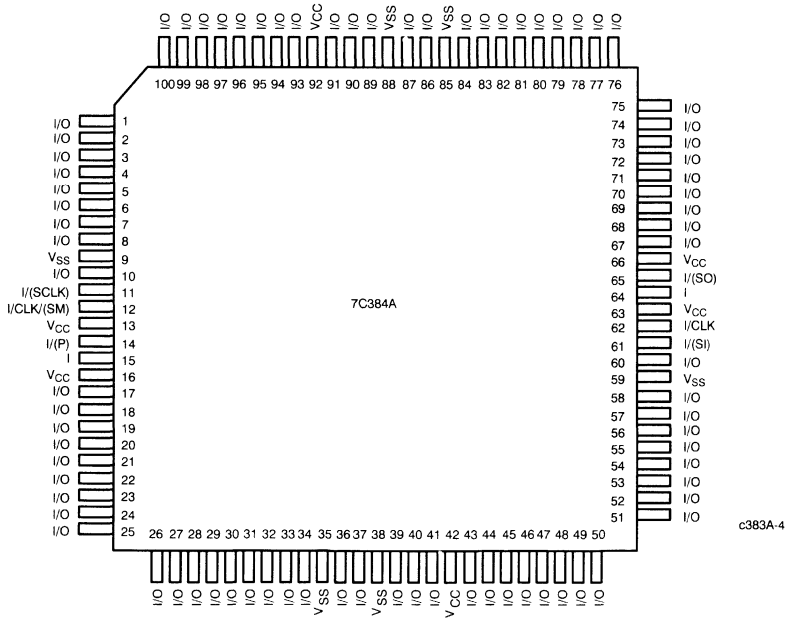
PLCC
Top View



PLCC
Top View



TQFP
Top View



Pin Configurations (continued)

CPGA
Bottom View

11	10	9	8	7	6	5	4	3	2	1	
I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	A
I/O	I/O	I/O	I/O	I/(SCLK)	I/(P)	I	I/O	I/O	I/O	I/O	B
I/O	I/O			V_{SS}	I/CLK/(SM)	V_{CC}		■	I/O	I/O	C
I/O	I/O								I/O	I/O	D
I/O	I/O	V_{CC}						V_{SS}	I/O	I/O	E
I/O	I/O	I/O						I/O	I/O	I/O	F
I/O	I/O	V_{SS}						V_{CC}	I/O	I/O	G
I/O	I/O								I/O	I/O	H
I/O	I/O			V_{CC}	I/CLK	V_{SS}			I/O	I/O	J
I/O	I/O	I/O	I/O	I/(SO)	I	I/(SI)	I/O	I/O	I/O	I/O	K
I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	L

c383A-5

4

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature
Ceramic ..... −65°C to +150°C
Plastic ..... −40°C to +125°C

Lead Temperature ..... 300°C

Supply Voltage ..... −0.5V to +7.0V

Input Voltage ..... −0.5V to V_{CC} +0.5V

ESD Pad Protection ..... ±2000 V

DC Input Voltage ..... ±20 mA

Latch-Up Current ..... ±200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	−40°C to +85°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Delay Factor (K)

Speed Grade	Military		Industrial		Commercial	
	Min.	Max.	Min.	Max.	Min.	Max.
−0	0.39	1.82	0.4	1.67	0.46	1.55
−1	0.39	1.56	0.4	1.43	0.46	1.33
−2			0.4	1.35	0.46	1.25

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −4.0 mA	3.7		V
		I_{OH} = −8.0 mA	2.4		V
		I_{OH} = −10.0 µA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA Commercial I_{OL} = 8.0 mA Military/Industrial		0.4	V
		I_{OL} = 10.0 µA		0.1	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
I_I	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}	−10	+10	µA
I_{OZ}	Output Leakage Current—Three-State	V_{IN} = V_{CC} or V_{SS}	−10	+10	µA
I_{OS}	Output Short Circuit Current	V_{OUT} = V_{SS}	−10	−80	mA
		V_{OUT} = V_{CC}	30	140	mA
I_{CC}	Standby Supply Current	V_{IN}, $V_{I/O}$ = V_{CC} or V_{SS}		10	mA

Capacitance

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance[1]	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		20	pF

Notes:
1. C_{IN} = 40 pF max. on I/(SI) and I/(P).

Switching Characteristics Over the Operating Range

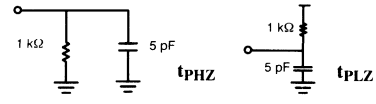
Parameter	Description	Propagation Delays[2] with Fanout of 1	2	3	4	8	Unit
LOGIC CELLS							
t_{PD}	Combinatorial Delay[3]	1.7	2.2	2.6	3.2	5.2	ns
t_{SU}	Set-Up Time[3]	2.1	2.1	2.1	2.1	2.1	ns
t_H	Hold Time	0.0	0.0	0.0	0.0	0.0	ns
t_{CLK}	Clock to Q Delay	1.0	1.5	1.9	2.5	4.6	ns
t_{CWHI}	Clock HIGH Time	2.0	2.0	2.0	2.0	2.0	ns
t_{CWLO}	Clock LOW Time	2.0	2.0	2.0	2.0	2.0	ns
t_{SET}	Set Delay	1.7	2.1	2.6	3.2	5.2	ns
t_{RESET}	Reset Delay	1.5	1.9	2.2	2.7	4.3	ns
t_{SW}	Set Width	1.9	1.9	1.9	1.9	1.9	ns
t_{RW}	Reset Width	1.8	1.8	1.8	1.8	1.8	ns

Parameter	Description	Propagation Delays[2] 1	2	3	4	6	8	Unit
INPUT CELLS								
t_{IN}	Input Delay (HIGH Drive)	2.4	2.5	2.6	2.7	3.0	3.3	ns
t_{INI}	Input, Inverting Delay (HIGH Drive)	2.5	2.6	2.7	2.8	3.1	3.6	ns
t_{IO}	Input Delay (Bidirectional Pad)	1.4	1.9	2.2	2.8	3.7	4.6	ns
t_{GCK}	Clock Buffer Delay[4]	2.7	2.8	2.8	2.9	2.9	3.0	ns
t_{GCKHI}	Clock Buffer Min. HIGH[4]	2.0	2.0	2.0	2.0	2.0	2.0	ns
t_{GCKLO}	Clock Buffer Min. LOW[4]	2.0	2.0	2.0	2.0	2.0	2.0	ns

Parameter	Description	Propagation Delays[2] with Output Load Capacitance (pF) of 30	50	75	100	150	Unit
OUTPUT CELLS							
t_{OUTLH}	Output Delay LOW to HIGH	2.7	3.4	4.2	5.0	6.7	ns
t_{OUTHL}	Output Delay HIGH to LOW	2.8	3.7	4.7	5.6	7.6	ns
t_{PZH}	Output Delay Three-State to HIGH	4.0	4.9	6.1	7.3	9.7	ns
t_{PZL}	Output Delay Three-State to LOW	3.6	4.2	5.0	5.8	7.3	ns
t_{PHZ}	Output Delay HIGH to Three-State[5]	2.9					ns
t_{PLZ}	Output Delay LOW to Three-State[5]	3.3					ns

Notes:

2. Worst-case propagation delay times over process variation at V_{CC} = 5.0V and T_A = 25°C. Multiply by the appropriate delay factor, K, for speed grade to get worst-case parameters over full V_{CC} and temperature range as specified in the operating range. All inputs are TTL with 3-ns linear transition time between 0 and 3 volts.
3. These limits are derived from worst-case values for a representative selection of the slowest paths through the pASIC logic cell including net delays. Guaranteed delay values for specific paths should be determined from simulation results.
4. Clock buffer fanout refers to the maximum number of flip-flops per half column. The number of half columns used does not affect clock buffer delay.
5. The following loads are used for t_{PXZ}:

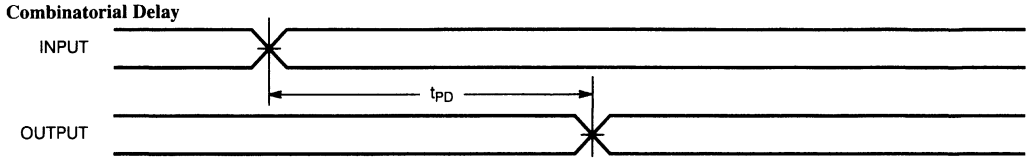


High Drive Buffer

Parameter	Description	# High Drives Wired Together	Propagation Delays[2] with Fanout of 12	24	48	72	96	Unit
t_{IN}	High Drive Input Delay	1	4.5	5.4				ns
		2		3.9	5.6			ns
		3			4.5	5.3	6.3	ns
		4				4.6	5.3	ns
t_{INI}	High Drive Input, Inverting Delay	1	4.7	5.6				ns
		2		4.0	5.8			ns
		3			4.6	5.5	6.4	ns
		4				4.8	5.5	ns

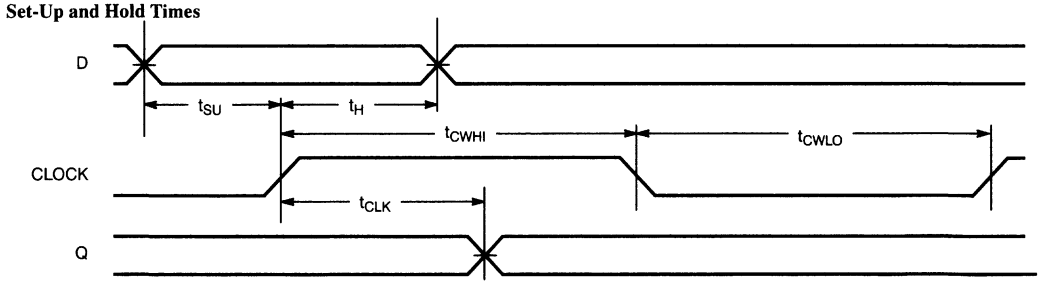
Switching Waveforms

Combinatorial Delay



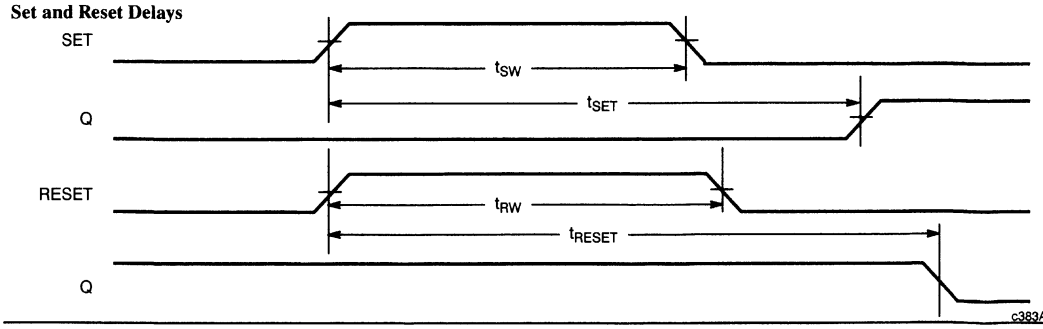
c383A-6

Set-Up and Hold Times



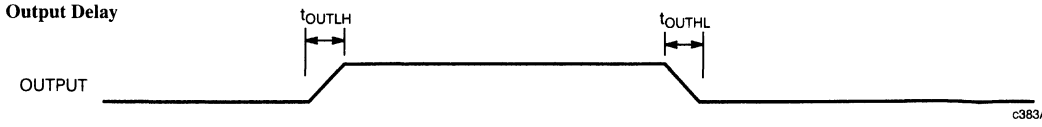
c383A-7

Set and Reset Delays



c383A-8

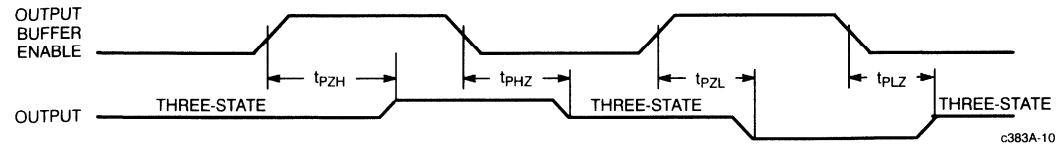
Output Delay



c383A-9

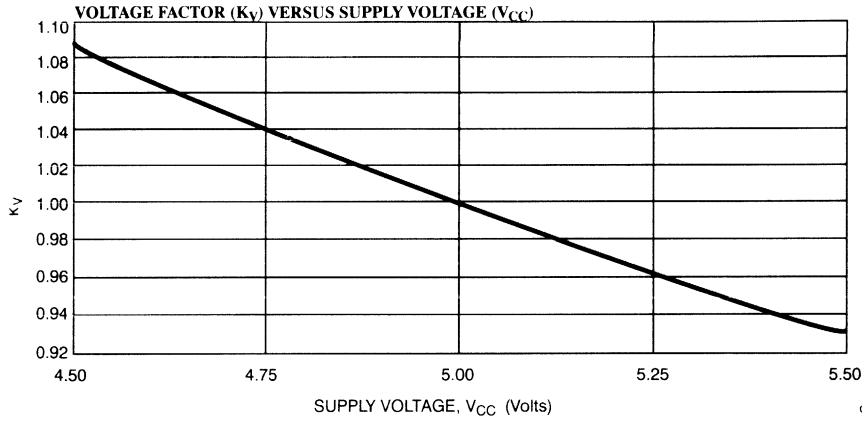
Switching Waveforms (continued)

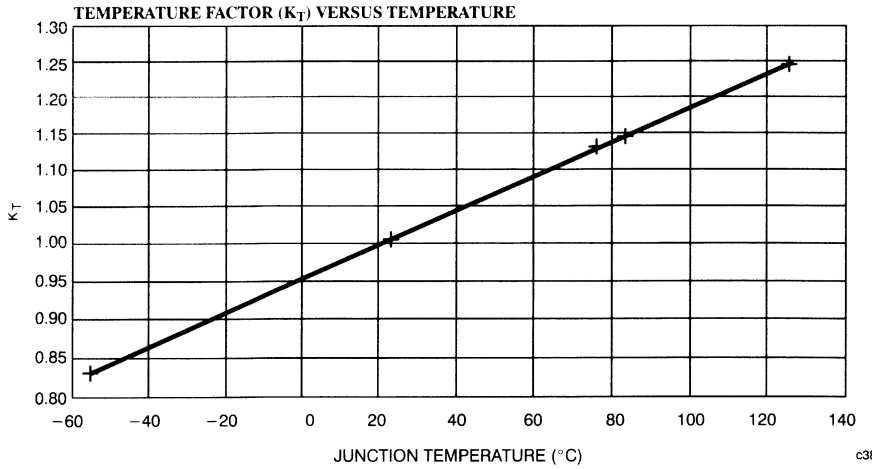
Three-State Delay



Typical AC Characteristics

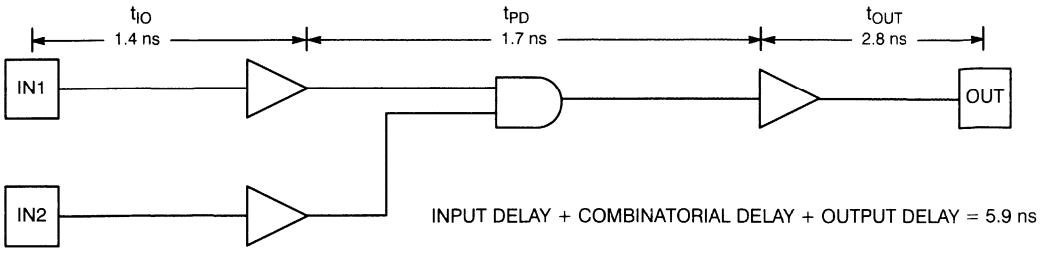
Propagation delays depend on routing, fan-out, load capacitance, supply voltage, junction temperature, and process variation. The AC Characteristics are a design guide to provide initial timing estimates at nominal conditions. Worst-case estimates are obtained when nominal propagation delays are multiplied by the appropriate Delay Factor, K, as specified by the speed grade in the Delay Factor table. The effects of voltage and temperature variation are illustrated in the graphs below. *Warp3* incorporates datasheet AC Characteristics into the design database for pre-place-and-route simulations. The *Warp3* Delay Modeler extracts specific timing parameters for precise simulation results following place and route.



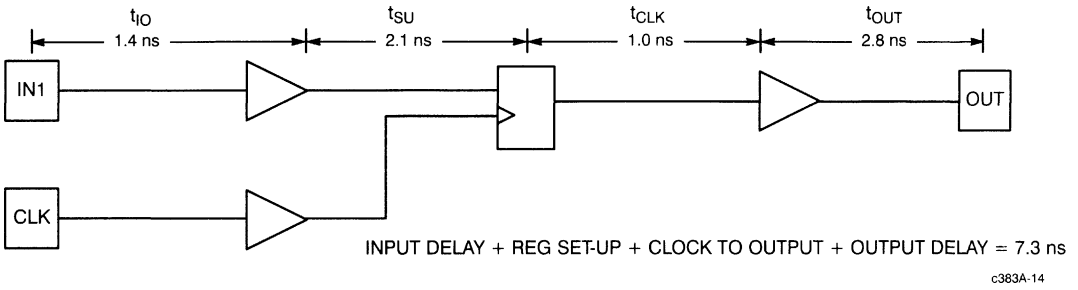


*THETA JA = 45 °C/WATT FOR PLCC

Combinatorial Delay Example (Load = 30 pF)



Sequential Delay Example (Load = 30 pF)



Ordering Information

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
2	CY7C383A–2JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C383A–2JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
1	CY7C383A–1JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C383A–1JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
0	CY7C383A–0JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C383A–0JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
2	CY7C384A–2AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C384A–2GC	**G84**	**84-Pin Grid Array (Cavity Up)**	
	CY7C384A–2JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C384A–2AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C384A–2GI	**G84**	**84-Pin Grid Array (Cavity Up)**	
	CY7C384A–2JI	J83	84-Lead Plastic Leaded Chip Carrier	
1	CY7C384A–1AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C384A–1GC	**G84**	**84-Pin Grid Array (Cavity Up)**	
	CY7C384A–1JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C384A–1AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C384A–1GI	**G84**	**84-Pin Grid Array (Cavity Up)**	
	CY7C384A–1JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C384A–1GMB	**G84**	**84-Pin Grid Array (Cavity Up)**	**Military**
0	CY7C384A–0AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C384A–0GC	**G84**	**84-Pin Grid Array (Cavity Up)**	
	CY7C384A–0JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C384A–0AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C384A–0GI	**G84**	**84-Pin Grid Array (Cavity Up)**	
	CY7C384A–0JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C384A–0GMB	G84	84-Pin Grid Array (Cavity Up)	Military

Shaded area contains advanced information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Document #: 38–00361

4

CY7C385A
CY7C386A

Very High Speed 4K (12K) Gate CMOS FPGA

Features

- **Very high speed**
  - **Loadable counter frequencies greater than 100 MHz**
  - **Chip-to-chip operating frequencies up to 85 MHz**
  - **Input + logic cell + output delays under 7 ns**
- **Unparalleled FPGA performance for counters, data path, state machines, arithmetic, and random logic**
- **High usable density**
  - **16 x 24 array of 384 logic cells provides 12,000 total available gates**
  - **4,000 typically usable "gate array" gates in 84-pin PLCC/CLCC, 100-pin and 144-pin TQFP, 145-pin CPGA, and 160-pin CQFP packages**
- **Low power, high output drive**
  - **Standby current typically 2 mA**
  - **16-bit counter operating at 100 MHz consumes 50 mA**
  - **Minimum I_{OL} and I_{OH} of 8 mA**
- **Flexible logic cell architecture**
  - **Wide fan-in (up to 14 input gates)**
  - **Multiple outputs in each cell**
  - **Very low cell propagation delay (1.7 ns)**
- **Powerful design tools—*Warp3*™**
  - **Designs entered in VHDL, schematics, or both**
  - **Fast, fully automatic place and route**
  - **Waveform simulation with back annotated net delays**
  - **PC and workstation platforms**
- **Robust routing resources**
  - **Fully automatic place and route of designs using up to 100 percent of logic resources**
  - **No hand routing required**
- **88 (7C385A) to 122 (7C386A) bidirectional input/output pins**
- **6 dedicated input/high-drive pins**
- **2 clock/dedicated input pins with fan-out-independent, low-skew nets**
  - **Clock skew <1 ns**
- **Input hysteresis provides high noise immunity**
- **Thorough testability**
  - **Built-in scan path permits 100 percent factory testing of logic and I/O cells**
  - **Automatic Test Vector Generation (ATVG) software supports user testing after programming**
- **0.65μ CMOS process with ViaLink™ programming technology**
  - **High-speed metal-to-metal link**
  - **Non-volatile antifuse technology**
- **100-pin TQFP is pin compatible with the 1K (CY7C381A/2A) and the 2K (CY7C383A/4A) FPGAs**

Functional Description

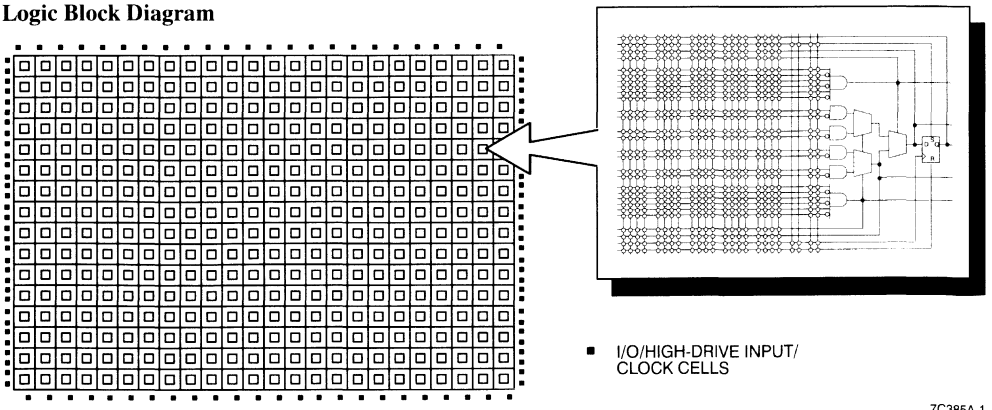
The CY7C385A and CY7C386A are very high speed CMOS user-programmable ASIC (pASIC™) devices. The 384 logic cell field-programmable gate array (FPGA) offers 4,000 typically usable "gate array" gates. This is equivalent to 12,000 EPLD or LCA gates. The CY7C385A is available in a 84-pin PLCC and CPGA and the 100-pin TQFP. The CY7C386A is available in 144-pin TQFP and CPGA packages, and a 160-pin CQFP package.

Low-impedance, metal-to-metal ViaLink interconnect technology provides non-volatile custom logic capable of operating at speeds above 150 MHz with input and output delays under 3 ns. This permits high-density programmable devices to be used with today's fastest CISC and RISC microprocessors.

Designs are entered into the CY7C385A and CY7C386A using Cypress *Warp3* software or one of several third-party tools. *Warp3* is a sophisticated CAE package that features schematic entry, waveform-based timing simulation, and VHDL design synthesis. The CY7C385A and CY7C386A feature ample on-chip routing channels for fast, fully automatic place and route of high gate utilization designs.

For detailed information about the pASIC380 architecture, see the pASIC380 Family datasheet.

Logic Block Diagram



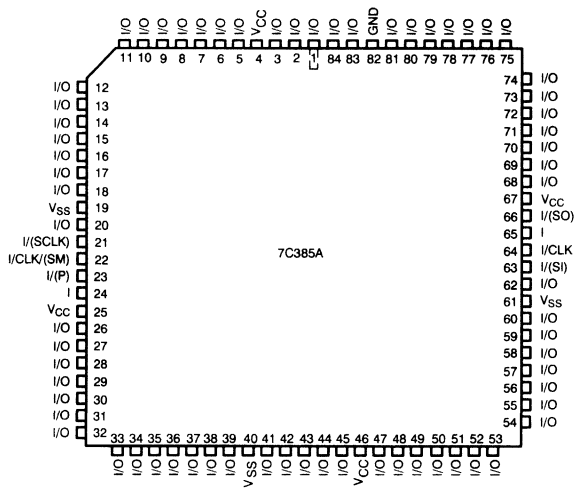
84 and 144 PINS, 114 I/O CELLS, 6 INPUT HIGH DRIVE CELLS, 2 INPUT/CLK (HIGH DRIVE) CELLS

7C385A-1

ViaLink and pASIC are trademarks of QuickLogic Corporation.
Warp3 is a trademark of Cypress Semiconductor Corporation.

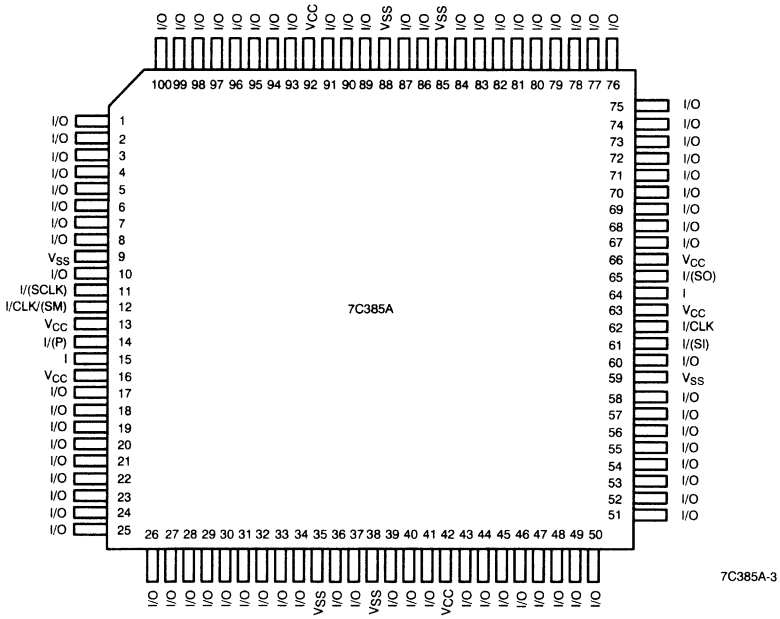
Pin Configurations

PLCC/CLCC
Top View



7C385A-2

TQFP
Top View

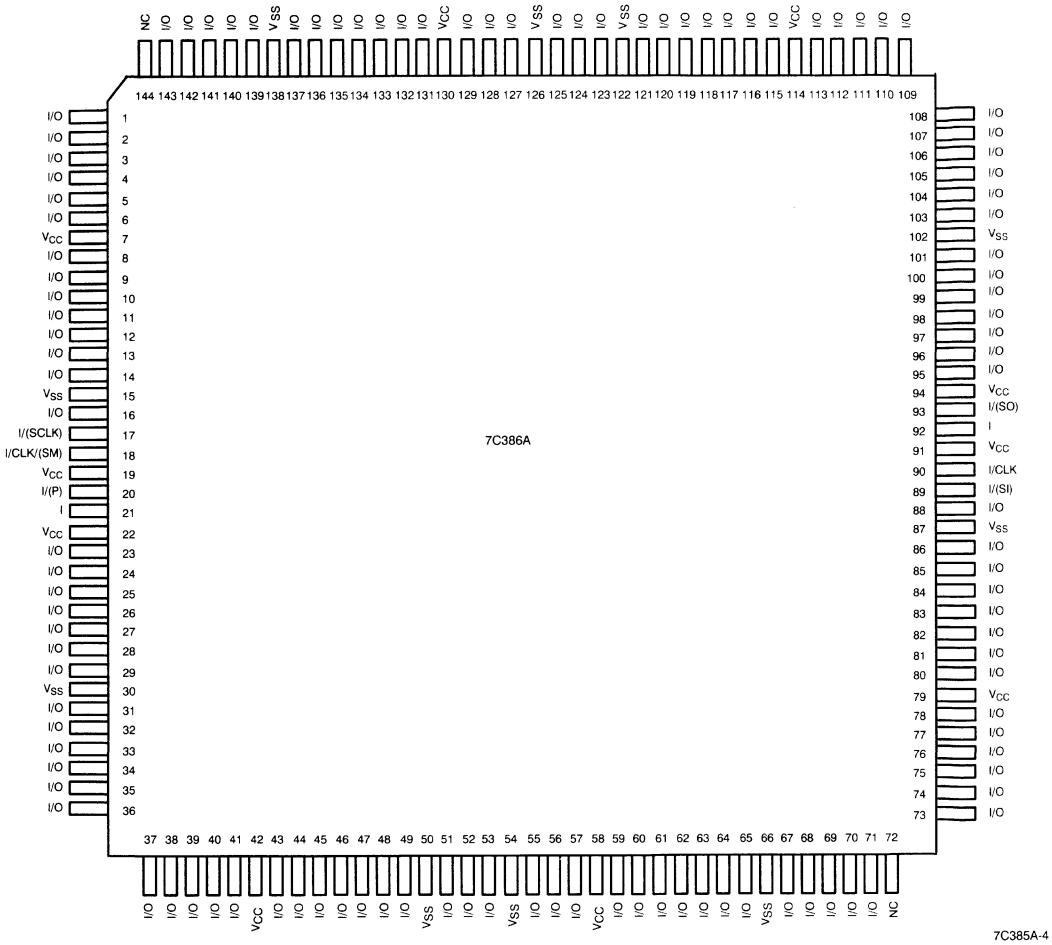


7C385A-3

4

Pin Configurations (continued)

TQFP
Top View



7C385A-4

Pin Configurations (continued)

CPGA
Bottom View

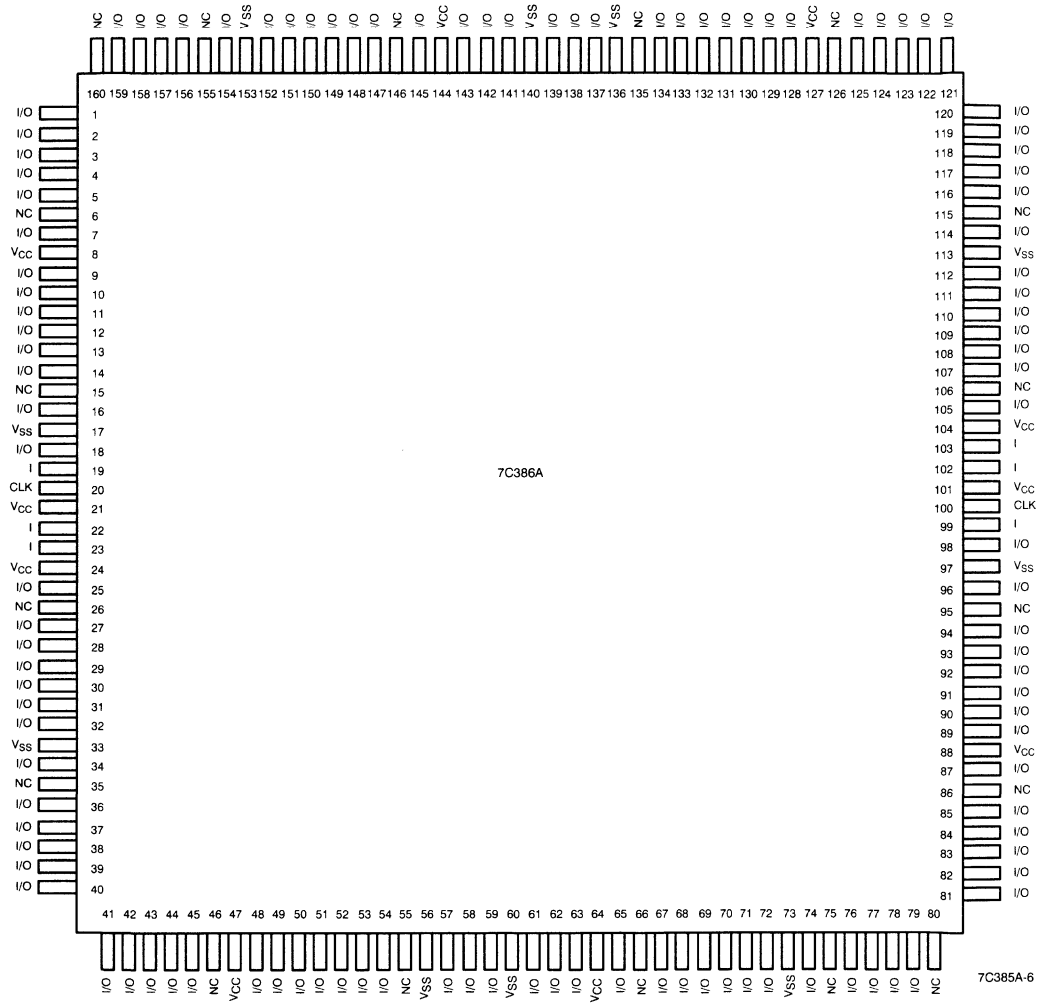
R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	1
I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC	I/O	2
I/O	I/O	V_{SS}	I/O	V_{CC}	I/O	V_{SS}	I/O	V_{CC}	I/O	V_{SS}	I/O	V_{CC}	I/O	I/O	3
I/O	I/O	I/O									■	I/O	I/O	I/O	4
I/O	I/O	V_{CC}										V_{SS}	I/O	I/O	5
I/O	I/O	I/O										I/O	I/O	I/O	6
I	I/(SO)	V_{SS}										V_{CC}	I/O	I/O	7
I/O	I/(SI)	I/CLK					7C386A					$I/_{CLK/(SM)}$	$I/_{(SCLK)}$	I/O	8
I/O	I/O	V_{CC}										V_{SS}	I	I/(P)	9
I/O	I/O	I/O										I/O	I/O	I/O	10
I/O	I/O	V_{SS}										V_{CC}	I/O	I/O	11
I/O	I/O	I/O										I/O	I/O	I/O	12
I/O	I/O	V_{CC}	I/O	V_{SS}	I/O	V_{CC}	I/O	V_{SS}	I/O	V_{CC}	I/O	V_{SS}	I/O	I/O	13
I/O	NC	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	14
I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	15

7C385A-5

4

Pin Configurations (continued)

CQFP
Top View



7C385A-6

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature
Ceramic ..... −65°C to +150°C
Plastic ..... −40°C to +125°C

Lead Temperature ..... 300°C

Supply Voltage ..... −0.5V to +7.0V

Input Voltage ..... −0.5V to V_{CC} +0.5V

ESD Pad Protection ..... ±2000 V

DC Input Voltage ..... −0.5V to 7.0V

Latch-Up Current ..... ±200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	−40°C to +85°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Delay Factor (K)

Speed Grade	Military		Industrial		Commercial	
	Min.	Max.	Min.	Max.	Min.	Max.
−0	0.39	1.82	0.4	1.67	0.46	1.55
−1	0.39	1.56	0.4	1.43	0.46	1.33
−2			0.4	1.35	0.46	1.25

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −4.0 mA	3.7		V
		I_{OH} = −8.0 mA	2.4		V
		I_{OH} = −10.0 µA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA Military/Industrial I_{OL} = 12 mA Commercial		0.4	V
		I_{OL} = 10.0 µA		0.1	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
I_I	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}	−10	+10	µA
I_{OZ}	Three-State Output Leakage Current	V_{IN} = V_{CC} or V_{SS}	−10	+10	µA
I_{OS}	Output Short Circuit Current	V_{OUT} = V_{SS}	−10	−80	mA
		V_{OUT} = V_{CC}	30	140	mA
I_{CC}	Standby Supply Current	V_{IN}, $V_{I/O}$ = V_{CC} or V_{SS}		10	mA

Capacitance

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance[1]	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		20	pF

Notes:
1. C_I = 45 pF max. on I/(SI) and I/(P).

Switching Characteristics Over the Operating Range

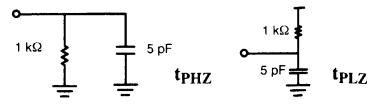
Parameter	Description	Propagation Delays[2] with Fanout of 1	2	3	4	8	Unit
LOGIC CELLS							
t_{PD}	Combinatorial Delay[3]	1.7	2.2	2.6	3.2	5.3	ns
t_{SU}	Set-Up Time[3]	2.1	2.1	2.1	2.1	2.1	ns
t_H	Hold Time	0.0	0.0	0.0	0.0	0.0	ns
t_{CLK}	Clock to Q Delay	1.0	1.5	1.9	2.6	4.7	ns
t_{CWHI}	Clock HIGH Time	2.0	2.0	2.0	2.0	2.0	ns
t_{CWLO}	Clock LOW Time	2.0	2.0	2.0	2.0	2.0	ns
t_{SET}	Set Delay	1.7	2.2	2.6	3.2	5.3	ns
t_{RESET}	Reset Delay	1.5	1.9	2.2	2.7	4.4	ns
t_{SW}	Set Width	1.9	1.9	1.9	1.9	1.9	ns
t_{RW}	Reset Width	1.8	1.8	1.8	1.8	1.8	ns

Parameter	Description	Propagation Delays[2] 1	2	3	4	8	12	Unit
INPUT CELLS								
t_{IN}	Input Delay (HIGH Drive)	2.8	2.9	3.0	3.1	4.0	5.3	ns
t_{INI}	Input, Inverting Delay (HIGH Drive)	3.0	3.1	3.2	3.3	4.1	5.7	ns
t_{IO}	Input Delay (Bidirectional Pad)	1.4	1.9	2.2	2.2	4.7	6.5	ns
t_{GCK}	Clock Buffer Delay[4]	2.7	2.8	2.9	3.0	3.1	3.3	ns
t_{GCKHI}	Clock Buffer Min. HIGH[4]	2.0	2.0	2.0	2.0	2.0	2.0	ns
t_{GCKLO}	Clock Buffer Min. LOW[4]	2.0	2.0	2.0	2.0	2.0	2.0	ns

Parameter	Description	Propagation Delays[2] with Output Load Capacitance (pF) of 30	50	75	100	150	Unit
OUTPUT CELLS							
t_{OUTLH}	Output Delay LOW to HIGH	2.7	3.4	4.2	5.0	6.7	ns
t_{OUTHL}	Output Delay HIGH to LOW	2.8	3.7	4.7	5.6	7.6	ns
t_{PZH}	Output Delay Three-State to HIGH	4.0	4.9	6.1	7.3	9.7	ns
t_{PZL}	Output Delay Three-State to LOW	3.6	4.2	5.0	5.8	7.3	ns
t_{PHZ}	Output Delay HIGH to Three-State[5]	2.9					ns
t_{PLZ}	Output Delay LOW to Three-State[5]	3.3					ns

Notes:

2. Worst-case propagation delay times over process variation at V_{CC} = 5.0V and T_A = 25°C. Multiply by the appropriate delay factor, K, for speed grade to get worst-case parameters over full V_{CC} and temperature range as specified in the operating range. All inputs are TTL with 3-ns linear transition time between 0 and 3 volts.
3. These limits are derived from worst-case values for a representative selection of the slowest paths through the pASIC logic cell including net delays. Guaranteed delay values for specific paths should be determined from simulation results.
4. Clock buffer fanout refers to the maximum number of flip-flops per half column. The number of half columns used does not affect clock buffer delay.
5. The following loads are used for t_{PXZ}:

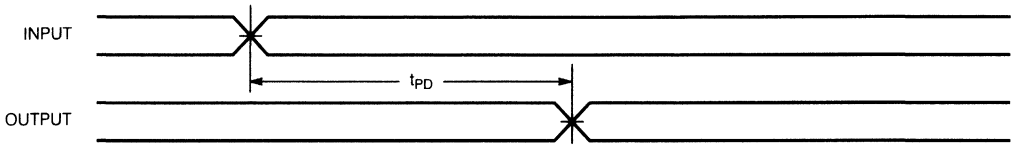


High Drive Buffer

Parameter	Description	# High Drives Wired Together	Propagation Delays[2] with Fanout of 12	24	48	72	96	Unit
t_{IN}	High Drive Input Delay	1	5.3	6.7				ns
		2		4.5	6.6			ns
		3			5.3	6.2	7.2	ns
		4				5.4	6.2	ns
t_{INI}	High Drive Input, Inverting Delay	1	5.7	7.2				ns
		2		4.6	6.8			ns
		3			5.5	6.4	7.4	ns
		4				5.6	6.4	ns

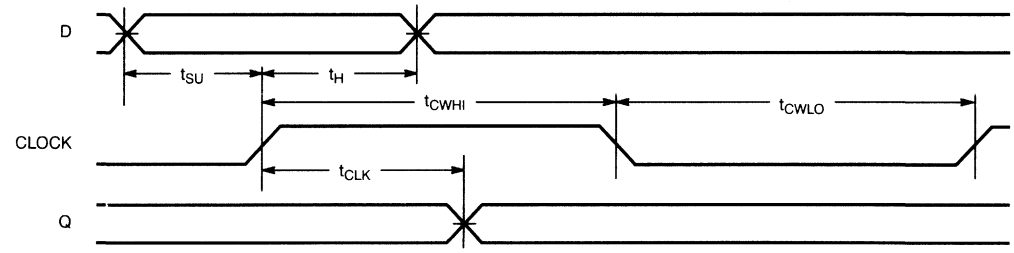
Switching Waveforms

Combinatorial Delay



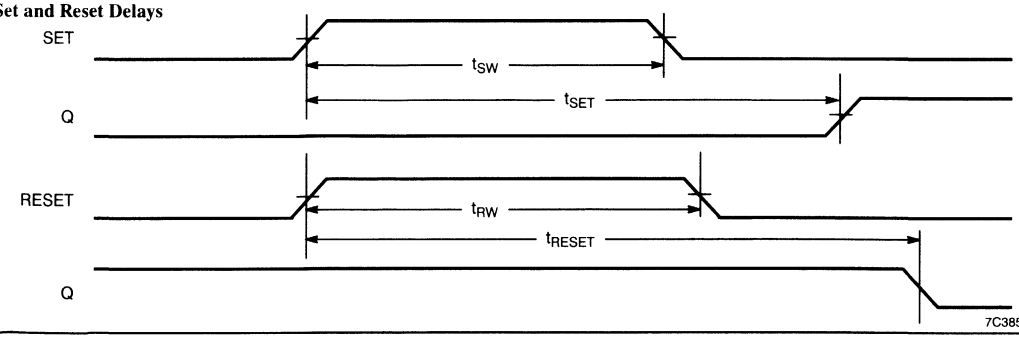
7C385A-7

Set-Up and Hold Times



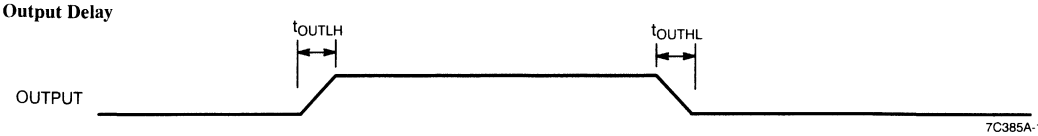
7C385A-8

Set and Reset Delays



7C385A-9

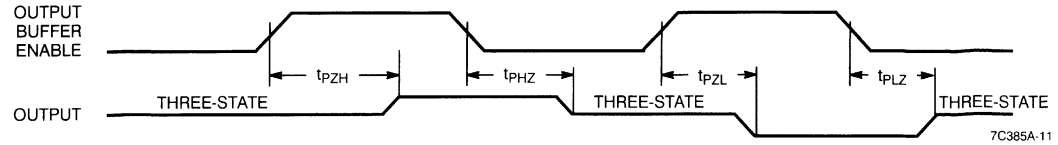
Output Delay



7C385A-10

Switching Waveforms (continued)

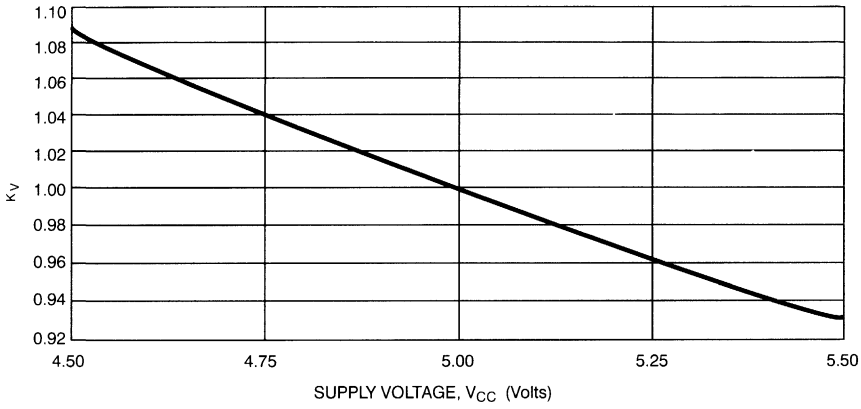
Three-State Delay



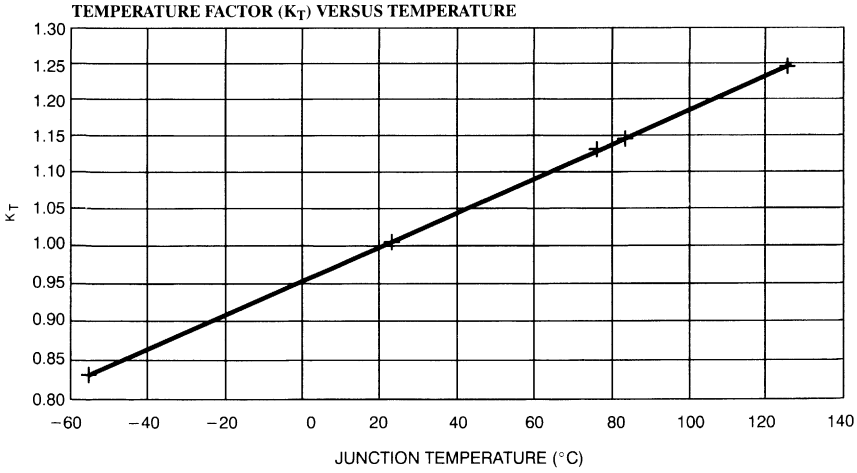
Typical AC Characteristics

Propagation delays depend on routing, fanout, load capacitance, supply voltage, junction temperature, and process variation. The AC Characteristics are a design guide to provide initial timing estimates at nominal conditions. Worst-case estimates are obtained when nominal propagation delays are multiplied by the appropriate Delay Factor, K, as specified by the speed grade in the Delay Factor table. The effects of voltage and temperature variation are illustrated in the graphs below. *Warp3* incorporates datasheet AC Characteristics into the design database for pre-place-and-route simulations. The *Warp3* Delay Modeler extracts specific timing parameters for precise simulation results following place and route.

VOLTAGE FACTOR (K_V) VERSUS SUPPLY VOLTAGE (V_{CC})

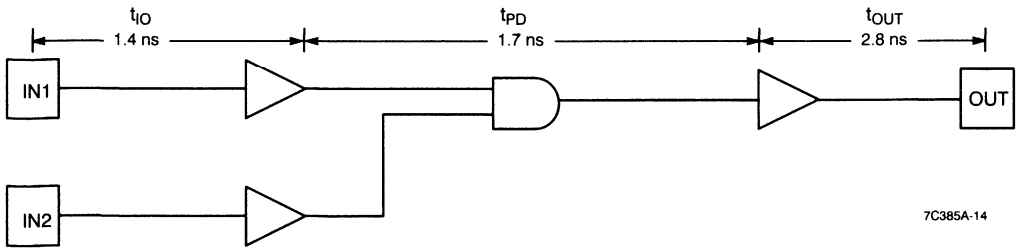


TEMPERATURE FACTOR (K_T) VERSUS TEMPERATURE



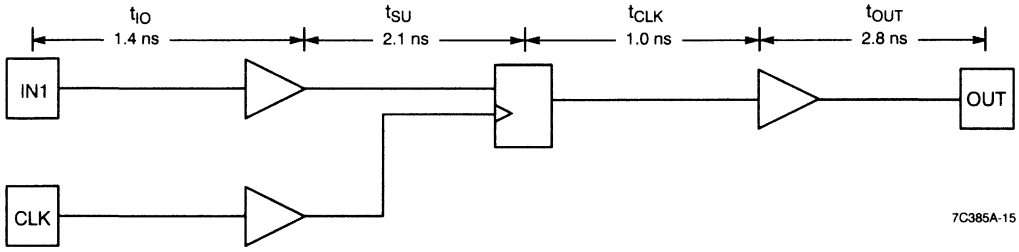
*THETA JA = 45 °C/WATT FOR PLCC

Combinatorial Delay Example (Load = 30 pF)



INPUT DELAY + COMBINATORIAL DELAY + OUTPUT DELAY = 5.9 ns

Sequential Delay Example (Load = 30 pF)



INPUT DELAY + REG SET-UP + CLOCK TO OUTPUT + OUTPUT DELAY = 7.3 ns

4

Ordering Information

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
2	CY7C385A–2AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C385A–2JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C385A–2AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C385A–2JI	J83	84-Lead Plastic Leaded Chip Carrier	
1	CY7C385A–1AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C385A–1JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C385A–1AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C385A–1JI	J83	84-Lead Plastic Leaded Chip Carrier	
0	CY7C385A–0AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C385A–0JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C385A–0AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C385A–0JI	J83	84-Lead Plastic Leaded Chip Carrier	

Ordering Information (continued)

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
2	CY7C386A–2AC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C386A–2GC	G145	145-Pin Grid Array (Cavity Up)	
	CY7C386A–2UC	U162	160-Lead Ceramic Quad Flatpack (Cavity Up)	
	CY7C386A–2AI	A144	144-Pin Thin Quad Flat Pack	Industrial
	CY7C386A–2GI	G145	145-Pin Grid Array (Cavity Up)	
	CY7C386A–2UI	U162	160-Lead Ceramic Quad Flatpack (Cavity Up)	
1	CY7C386A–1AC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C386A–1GC	G145	145-Pin Grid Array (Cavity Up)	
	CY7C386A–1UC	U162	160-Lead Ceramic Quad Flatpack (Cavity Up)	
	CY7C386A–1AI	A144	144-Pin Thin Quad Flat Pack	Industrial
	CY7C386A–1GI	G145	145-Pin Grid Array (Cavity Up)	
	CY7C386A–1UI	U162	160-Lead Ceramic Quad Flatpack (Cavity Up)	
	CY7C386A–1GMB	G145	145-Pin Grid Array (Cavity Up)	Military
	CY7C386A–1UMB	U162	160-Lead Ceramic Quad Flatpack (Cavity Up)	
0	CY7C386A–0AC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C386A–0GC	G145	145-Pin Grid Array (Cavity Up)	
	CY7C386A–0UC	U162	160-Lead Ceramic Quad Flatpack (Cavity Up)	
	CY7C386A–0AI	A144	144-Pin Thin Quad Flat Pack	Industrial
	CY7C386A–0GI	G145	145-Pin Grid Array (Cavity Up)	
	CY7C386A–0UI	U162	160-Lead Ceramic Quad Flatpack (Cavity Up)	
	CY7C386A–0GMB	G145	145-Pin Grid Array (Cavity Up)	Military
	CY7C386A–0UMB	U162	160-Lead Ceramic Quad Flatpack (Cavity Up)	

Shaded area contains advanced information.

Military Specifications
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Document #: 38–00209–C

PRELIMINARY

CY7C387A
CY7C388A

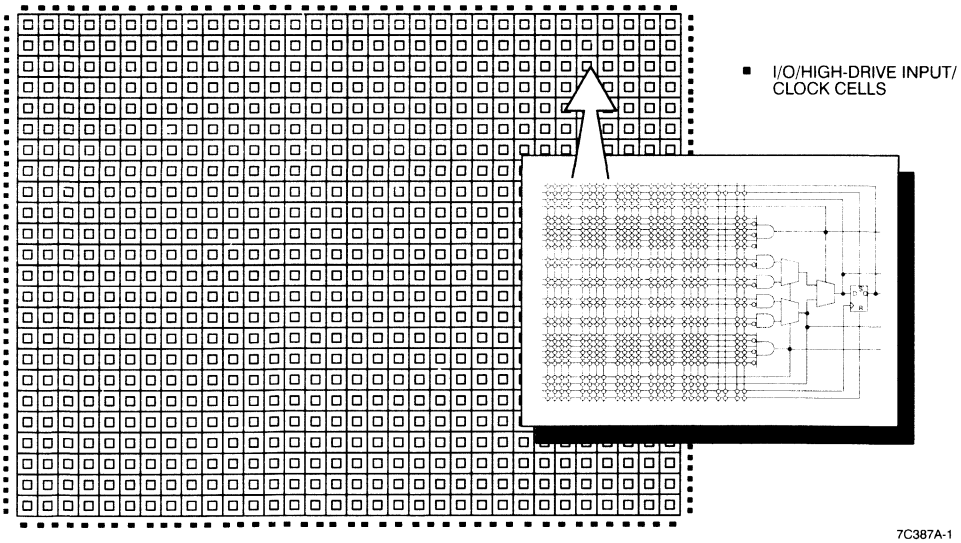
Very High Speed 8K (24K) Gate CMOS FPGA

Features

- Very high speed
  - Loadable counter frequencies greater than 100 MHz
  - Chip-to-chip operating frequencies up to 85 MHz
  - Input + logic cell + output delays under 7 ns
- Unparalleled FPGA performance for counters, data path, state machines, arithmetic, and random logic
- High usable density
  - 24 x 32 array of 768 logic cells provides 24,000 total available gates
  - 8,000 typically usable "gate array" gates in 145-pin and 245-pin CPGA, 144-pin TQFP, 208-pin PQFP, 160-pin CQFP, and 225-pin BGA packages
- PCI compliant I/O pins
- Low power, high output drive
  - Standby current typically 2 mA
  - 16-bit counter operating at 100 MHz consumes 50 mA
  - Minimum I_{OL} of 12 mA and I_{OH} of 8 mA
- Flexible logic cell architecture
  - Wide fan-in (up to 14 input gates)
  - Multiple outputs in each cell
  - Very low cell propagation delay (1.7 ns)
- Powerful design tools—*Warp3* ™
  - Designs entered in VHDL, schematics, or mixed
  - Fast, fully automatic place and route
  - Waveform simulation with back annotated net delays
  - PC and workstation platforms
- Robust routing resources
  - Fully automatic place and route of designs using up to 100 percent of logic resources
  - No hand routing required
- 132 (7C387A) to 172 (7C388A) bidirectional input/output pins
- 6 dedicated input/high-drive pins
- 2 clock/dedicated input pins with fan-out-independent, low-skew nets
  - Clock skew <1 ns
- Input hysteresis provides high noise immunity
- Thorough testability
  - Built-in scan path permits 100 percent factory testing of logic and I/O cells
  - Automatic Test Vector Generation (ATVG) software supports user testing after programming
- 0.65µ CMOS process with ViaLink ™ programming technology
  - High-speed metal-to-metal link
  - Non-volatile antifuse technology
- 144-pin TQFP, 145-pin CPGA, and 160-pin CQFP are pin compatible with the CY7C386A

4

Logic Block Diagram



144 and 208 PINS, 172 I/O CELLS, 6 INPUT HIGH DRIVE CELLS, 2 INPUT/CLK (HIGH DRIVE) CELLS

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Warp3 is a trademark of Cypress Semiconductor Corporation.

Functional Description

The CY7C387A and CY7C388A are very high speed, CMOS, user-programmable ASIC (pASIC™) devices. The 768 logic cell field-programmable gate array (FPGA) offers 8,000 typically usable "gate array" gates. This is equivalent to 24,000 EPLD or LCA gates. The CY7C387A is available in a 145-pin CPGA, 160-pin CQFP, and 144-pin TQFP. The CY7C388A is available in 208-pin PQFP, 245-pin CPGA, and 225-pin BGA packages.

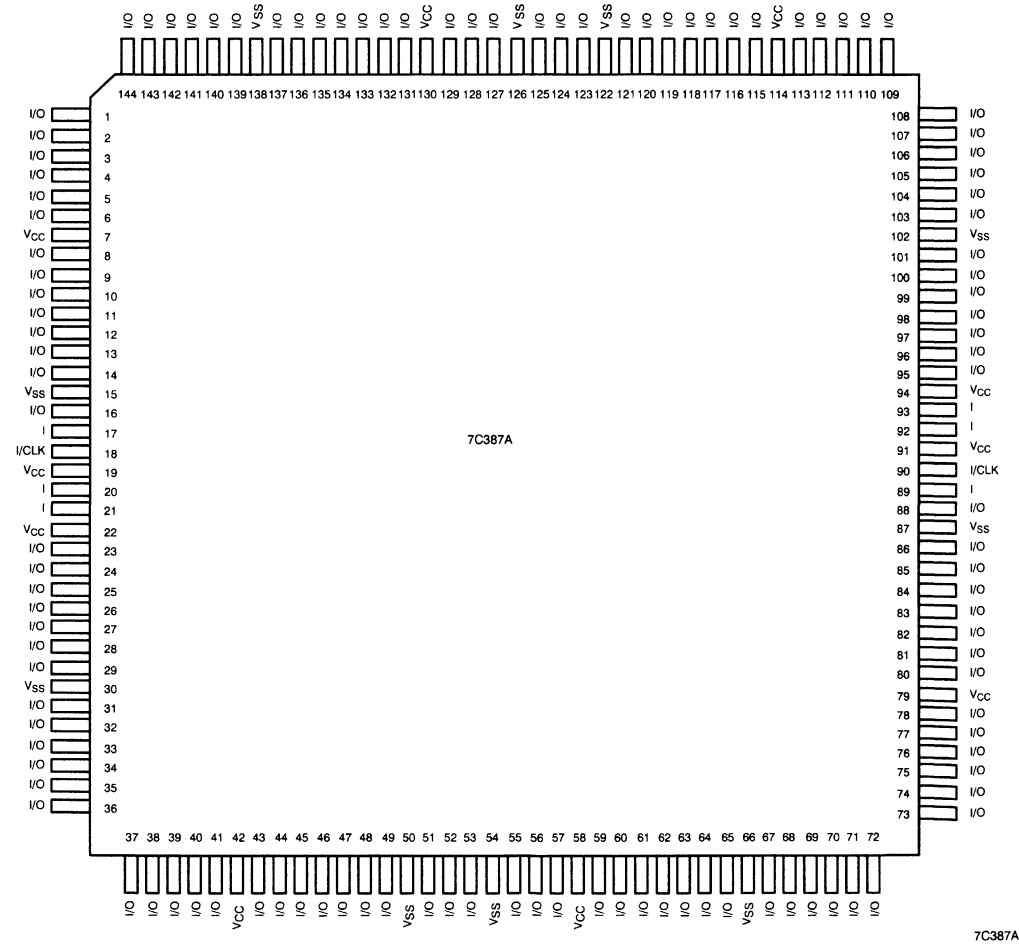
Low-impedance, metal-to-metal ViaLink interconnect technology provides non-volatile custom logic capable of operating at speeds above 150 MHz with input and output delays under 3 ns. This permits high-density programmable devices to be used with today's fastest CISC and RISC microprocessors.

Designs are entered into the CY7C387A and CY7C388A using Cypress *Warp3* software or one of several third-party tools. *Warp3* is a sophisticated CAE package that features schematic entry, waveform-based timing simulation, and VHDL design synthesis. The CY7C387A and CY7C388A feature ample on-chip routing channels for fast, fully automatic place and route of high gate utilization designs.

For detailed information about the pASIC380 architecture, see the pASIC380 Family datasheet.

Pin Configurations

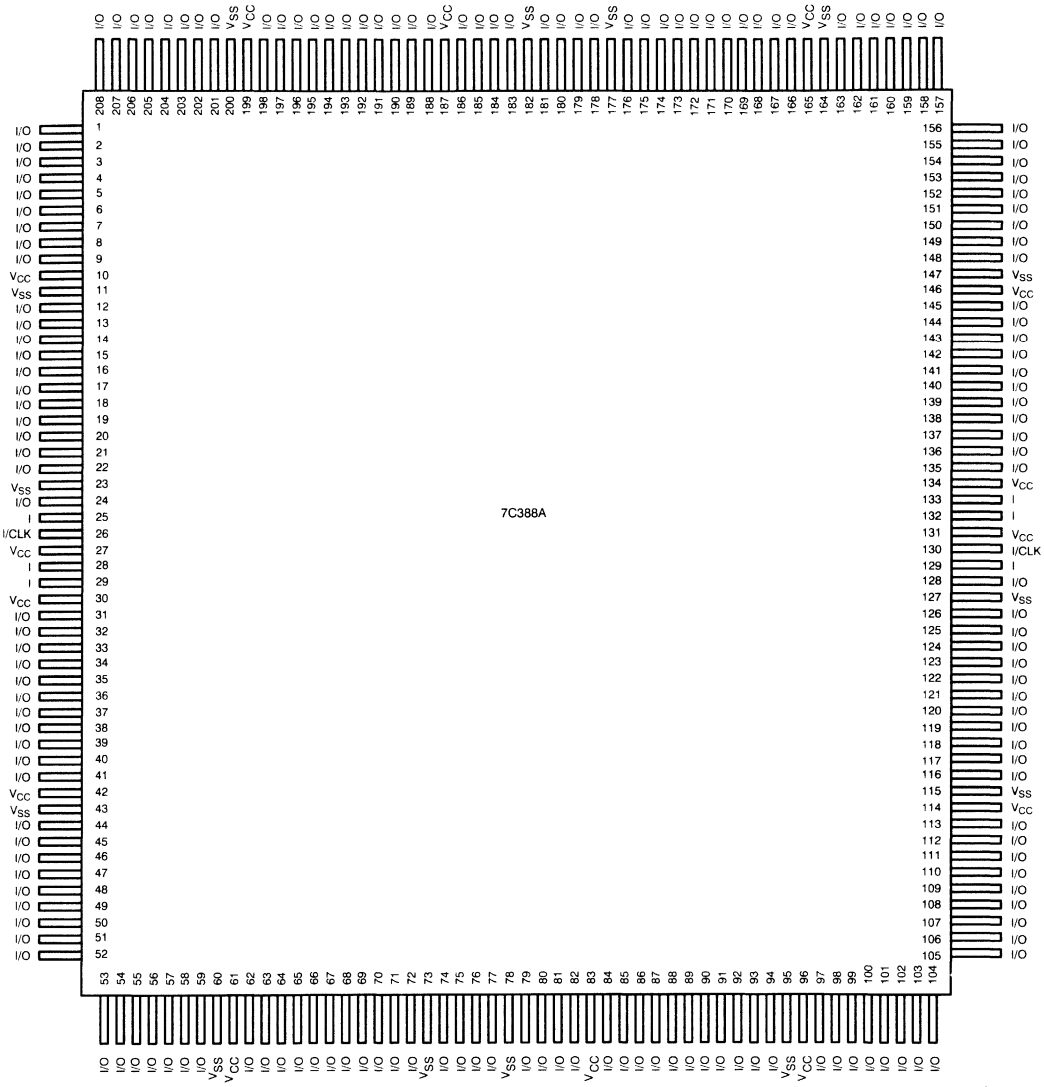
144-Pin Thin Quad Flat Pack (TQFP)
Top View



7C387A-2

Pin Configurations (continued)

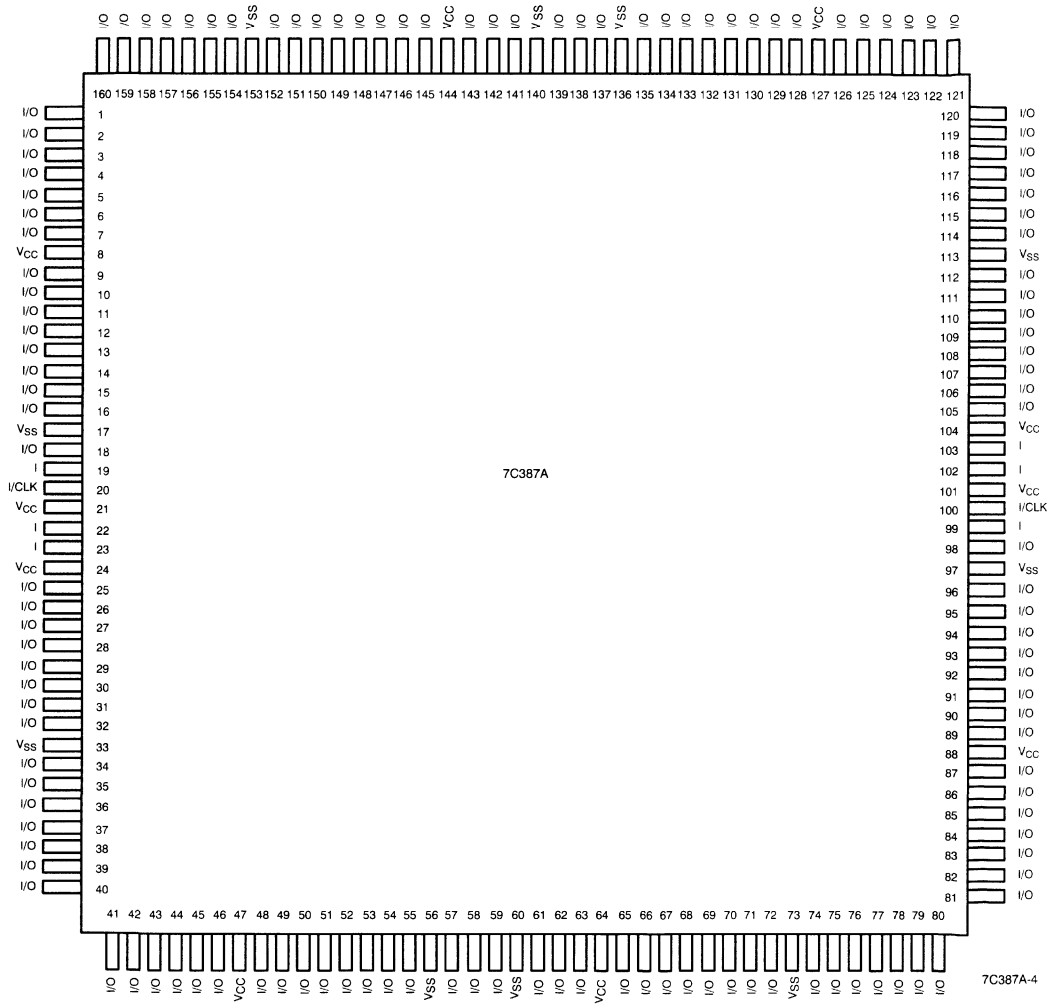
208-Pin Plastic Quad Flat Pack (PQFP)
Top View



7C387A-3

Pin Configurations (continued)

160-Pin CQFP
Top View



Pin Configurations (continued)

145-Pin CPGA
Bottom View

R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	1
I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	2
I/O	I/O	V_{SS}	I/O	V_{CC}	I/O	V_{SS}	I/O	V_{CC}	I/O	V_{SS}	I/O	V_{CC}	I/O	I/O	3
I/O	I/O	I/O									■	I/O	I/O	I/O	4
I/O	I/O	V_{CC}										V_{SS}	I/O	I/O	5
I/O	I/O	I/O										I/O	I/O	I/O	6
I	I	V_{SS}										V_{CC}	I/O	I/O	7
I/O	I	I/CLK					7C387A					I/CLK	I	I/O	8
I/O	I/O	V_{CC}										V_{SS}	I	I	9
I/O	I/O	I/O										I/O	I/O	I/O	10
I/O	I/O	V_{SS}										V_{CC}	I/O	I/O	11
I/O	I/O	I/O										I/O	I/O	I/O	12
I/O	I/O	V_{CC}	I/O	V_{SS}	I/O	V_{CC}	I/O	V_{SS}	I/O	V_{CC}	I/O	V_{SS}	I/O	I/O	13
I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	14
I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	15

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature
Ceramic ..... −65°C to +150°C
Plastic ..... −40°C to +125°C
Lead Temperature ..... 300°C
Supply Voltage ..... −0.5V to +7.0V
Input Voltage ..... −0.5V to V_{CC} +0.5V
ESD Pad Protection ..... ±2000 V
DC Input Voltage ..... −0.5V to 7.0V
Latch-Up Current ..... ±200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	−40°C to +85°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Delay Factor (K)

Speed Grade	Military		Industrial		Commercial	
	Min.	Max.	Min.	Max.	Min.	Max.
−0	0.39	1.82	0.4	1.67	0.46	1.55
−1	0.39	1.56	0.4	1.43	0.46	1.33
−2			0.4	1.35	0.46	1.25

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −4.0 mA	3.7		V
		I_{OH} = −8.0 mA	2.4		V
		I_{OH} = −10.0 µA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA Military/Industrial I_{OL} = 12 mA Commercial		0.4	V
		I_{OL} = 10.0 µA		0.1	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
I_I	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}	−10	+10	µA
I_{OZ}	Three-State Output Leakage Current	V_{IN} = V_{CC} or V_{SS}	−10	+10	µA
I_{OS}	Output Short Circuit Current	V_{OUT} = V_{SS}	−10	−80	mA
		V_{OUT} = V_{CC}	30	140	mA
I_{CC}	Standby Supply Current	V_{IN}, $V_{I/O}$ = V_{CC} or V_{SS}		10	mA

Capacitance

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Switching Characteristics Over the Operating Range

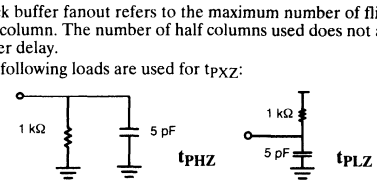
Parameter	Description	Propagation Delays[1] with Fanout of 1	2	3	4	8	Unit
LOGIC CELLS							
t_{PD}	Combinatorial Delay[2]	1.7	2.2	2.6	3.2	5.3	ns
t_{SU}	Set-Up Time[2]	2.1	2.1	2.1	2.1	2.1	ns
t_H	Hold Time	0.0	0.0	0.0	0.0	0.0	ns
t_{CLK}	Clock to Q Delay	1.0	1.5	1.9	2.6	4.7	ns
t_{CWHI}	Clock HIGH Time	2.0	2.0	2.0	2.0	2.0	ns
t_{CWLO}	Clock LOW Time	2.0	2.0	2.0	2.0	2.0	ns
t_{SET}	Set Delay	1.7	2.2	2.6	3.2	5.3	ns
t_{RESET}	Reset Delay	1.5	1.9	2.2	2.7	4.4	ns
t_{SW}	Set Width	1.9	1.9	1.9	1.9	1.9	ns
t_{RW}	Reset Width	1.8	1.8	1.8	1.8	1.8	ns

Parameter	Description	Propagation Delays[1] with Fanout of 1	2	3	4	8	12	Unit
INPUT CELLS								
t_{IN}	Input Delay (HIGH Drive)	2.8	2.9	3.0	3.1	4.0	5.3	ns
t_{INI}	Input, Inverting Delay (HIGH Drive)	3.0	3.1	3.2	3.3	4.1	5.7	ns
t_{IO}	Input Delay (Bidirectional Pad)	1.4	1.9	2.2	2.2	4.7	6.5	ns
t_{GCK}	Clock Buffer Delay[3]	2.7	2.8	2.9	3.0	3.1	3.3	ns
t_{GCKHI}	Clock Buffer Min. HIGH[3]	2.0	2.0	2.0	2.0	2.0	2.0	ns
t_{GCKLO}	Clock Buffer Min. LOW[3]	2.0	2.0	2.0	2.0	2.0	2.0	ns

Parameter	Description	Propagation Delays[1] with Output Load Capacitance (pF) of 30	50	75	100	150	Unit
OUTPUT CELLS							
t_{OUTLH}	Output Delay LOW to HIGH	2.7	3.4	4.2	5.0	6.7	ns
t_{OUTHL}	Output Delay HIGH to LOW	2.8	3.7	4.7	5.6	7.6	ns
t_{PZH}	Output Delay Three-State to HIGH	4.0	4.9	6.1	7.3	9.7	ns
t_{PZL}	Output Delay Three-State to LOW	3.6	4.2	5.0	5.8	7.3	ns
t_{PHZ}	Output Delay HIGH to Three-State[4]	2.9					ns
t_{PLZ}	Output Delay LOW to Three-State[4]	3.3					ns

Notes:

1. Worst-case propagation delay times over process variation at V_{CC} = 5.0V and T_A = 25°C. Multiply by the appropriate delay factor, K, for speed grade to get worst-case parameters over full V_{CC} and temperature range as specified in the operating range. All inputs are TTL with 3-ns linear transition time between 0 and 3 volts.
2. These limits are derived from worst-case values for a representative selection of the slowest paths through the pASIC logic cell including net delays. Guaranteed delay values for specific paths should be determined from simulation results.
3. Clock buffer fanout refers to the maximum number of flip-flops per half column. The number of half columns used does not affect clock buffer delay.
4. The following loads are used for t_{PXZ}:

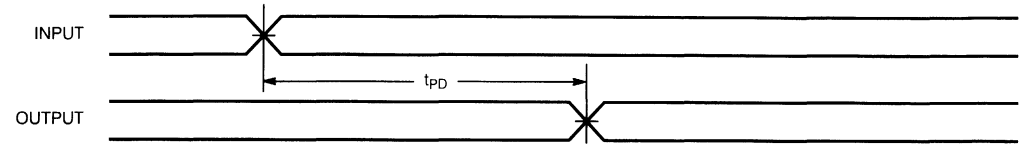


High Drive Buffer

Parameter	Description	# High Drives Wired Together	Propagation Delays[1] with Fanout of 12	24	48	72	96	Unit
t_{IN}	High Drive Input Delay	1	5.3	6.7				ns
		2		4.5	6.6			ns
		3			5.3	6.2	7.2	ns
		4				5.4	6.2	ns
t_{INI}	High Drive Input, Inverting Delay	1	5.7	7.2				ns
		2		4.6	6.8			ns
		3			5.5	6.4	7.4	ns
		4				5.6	6.4	ns

Switching Waveforms

Combinatorial Delay



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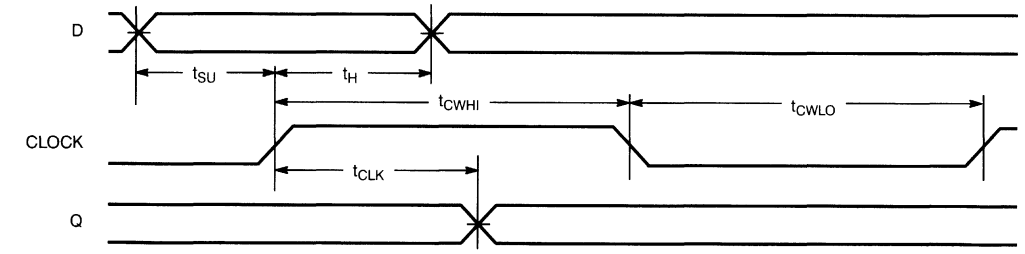
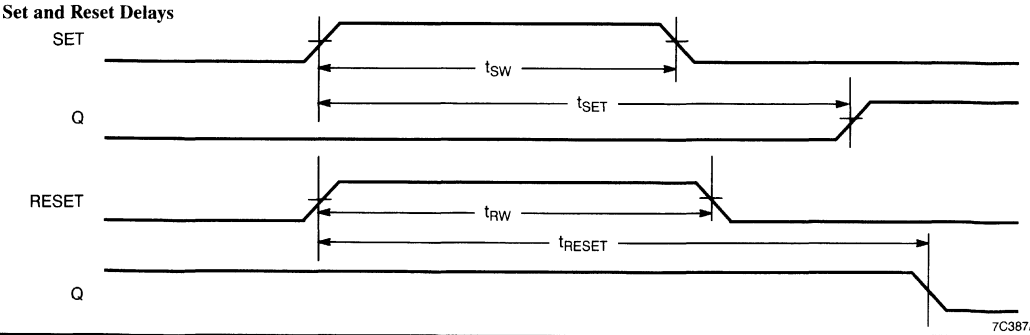
Set-Up and Hold Times



7C387A-7

Set and Reset Delays



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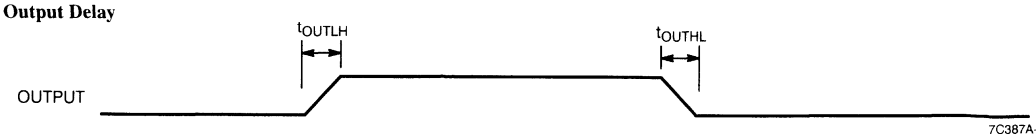
Output Delay



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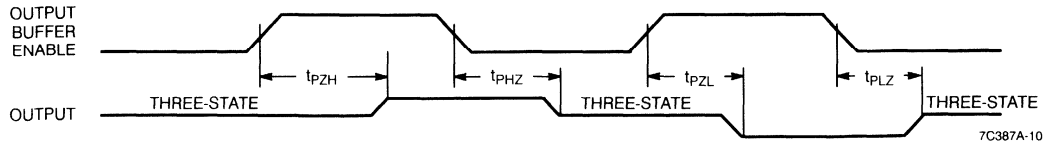
Switching Waveforms (continued)

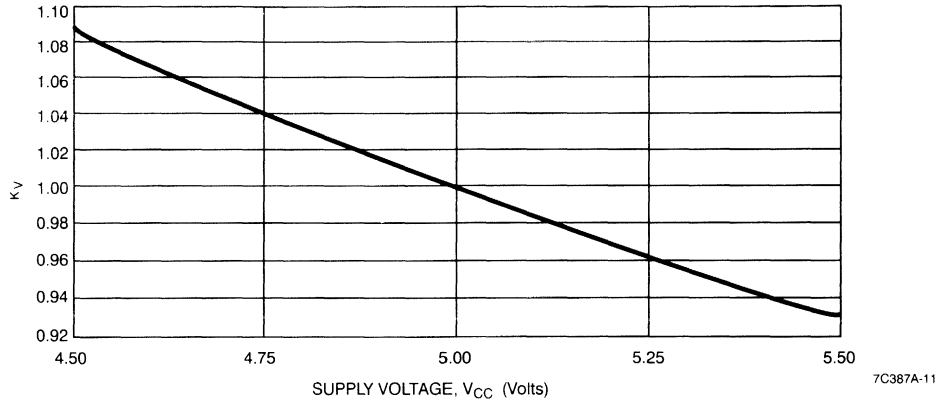
Three-State Delay



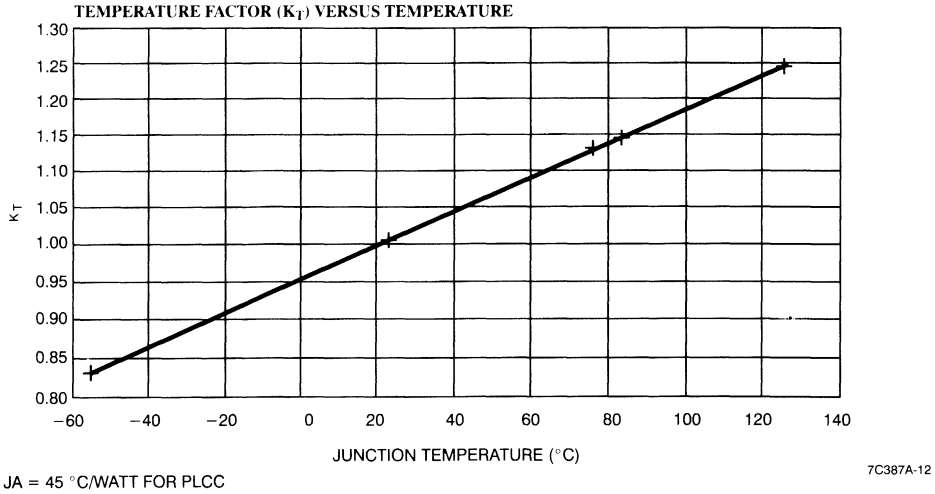
Typical AC Characteristics

Propagation delays depend on routing, fanout, load capacitance, supply voltage, junction temperature, and process variation. The AC Characteristics are a design guide to provide initial timing estimates at nominal conditions. Worst-case estimates are obtained when nominal propagation delays are multiplied by the appropriate Delay Factor, K, as specified by the speed grade in the Delay Factor table. The effects of voltage and temperature variation are illustrated in the graphs below. *Warp3* incorporates datasheet AC Characteristics into the design database for pre-place-and-route simulations. The *Warp3* Delay Modeler extracts specific timing parameters for precise simulation results following place and route.

VOLTAGE FACTOR (K_V) VERSUS SUPPLY VOLTAGE (V_{CC})

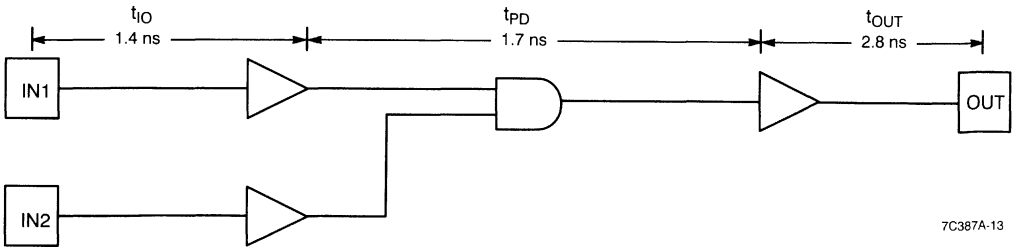


TEMPERATURE FACTOR (K_T) VERSUS TEMPERATURE



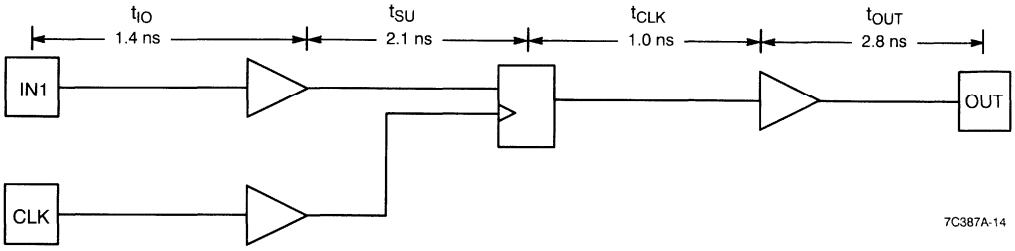
*THETA JA = 45 °C/WATT FOR PLCC

Combinatorial Delay Example (Load = 30 pF)



INPUT DELAY + COMBINATORIAL DELAY + OUTPUT DELAY = 5.9 ns

Sequential Delay Example (Load = 30 pF)



INPUT DELAY + REG SET-UP + CLOCK TO OUTPUT + OUTPUT DELAY = 7.3 ns

Ordering Information

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
2	CY7C387A–2AC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C387A–2GC	G145	145-Pin Grid Array (Cavity Up)	
	CY7C387A–2AI	A144	144-Pin Thin Quad Flat Pack	Industrial
	CY7C387A–2GI	G145	145-Pin Grid Array (Cavity Up)	
1	CY7C387A–1AC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C387A–1GC	G145	145-Pin Grid Array (Cavity Up)	
	CY7C387A–1AI	A144	144-Pin Thin Quad Flat Pack	Industrial
	CY7C387A–1GI	G145	145-Pin Grid Array (Cavity Up)	
	CY7C387A–1GMB	G145	145-Pin Grid Array (Cavity Up)	Military
	CY7C387A–1UMB	U162	160-Lead Ceramic Quad Flatpack (Cavity Up)	
0	CY7C387A–0AC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C387A–0GC	G145	145-Pin Grid Array (Cavity Up)	
	CY7C387A–0AI	A144	144-Pin Thin Quad Flat Pack	Industrial
	CY7C387A–0GI	G145	145-Pin Grid Array (Cavity Up)	
	CY7C387A–0GMB	G145	145-Pin Grid Array (Cavity Up)	Military
	CY7C387A–0UMB	U162	160-Lead Ceramic Quad Flatpack (Cavity Up)	

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
2	CY7C388A–2AC	A208	208-Pin Thin Quad Flat Pack	Commercial
	CY7C388A–2BGC	B225	225-Pin Ball Grid Array	
	CY7C388A–2GC	G245	245-Pin Grid Array (Cavity Up)	
	CY7C388A–2AI	A208	208-Pin Thin Quad Flat Pack	Industrial
	CY7C388A–2GI	G245	245-Pin Grid Array (Cavity Up)	
1	CY7C388A–1AC	A208	208-Pin Thin Quad Flat Pack	Commercial
	CY7C388A–1BGC	B225	225-Pin Ball Grid Array	
	CY7C388A–1GC	G245	245-Pin Grid Array (Cavity Up)	
	CY7C388A–1AI	A208	208-Pin Thin Quad Flat Pack	Industrial
	CY7C388A–1GI	G245	245-Pin Grid Array (Cavity Up)	
	CY7C388A–1GMB	G245	245-Pin Grid Array (Cavity Up)	Military
0	CY7C388A–0AC	A208	208-Pin Thin Quad Flat Pack	Commercial
	CY7C388A–0BGC	B225	225-Pin Ball Grid Array	
	CY7C388A–0GC	G245	245-Pin Grid Array (Cavity Up)	
	CY7C388A–0AI	A208	208-Pin Thin Quad Flat Pack	Industrial
	CY7C388A–0GI	G245	245-Pin Grid Array (Cavity Up)	
	CY7C388A–0GMB	G245	245-Pin Grid Array (Cavity Up)	Military

Shaded area contains advanced information.

Military Specifications
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Document #: 38–00373

CYPRESS

ADVANCED INFORMATION

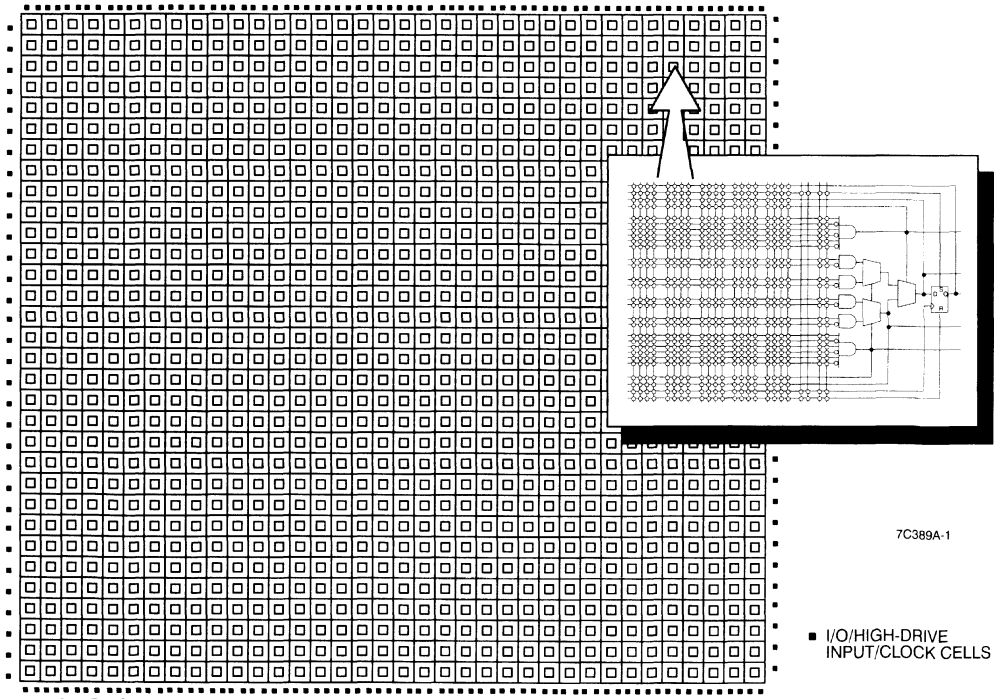
CY7C389A

Very High Speed 12K (36K) Gate CMOS FPGA

Features

- Very high speed
  - Loadable counter frequencies greater than 100 MHz
  - Chip-to-chip operating frequencies up to 85 MHz
  - Input + logic cell + output delays under 7 ns
- Unparalleled FPGA performance for counters, data path, state machines, arithmetic, and random logic
- High usable density
  - 32 x 36 array of 1152 logic cells provides 36,000 total available gates
  - 12,000 typically usable "gate array" gates in 208-pin PQFP, 313-pin BGA, and 245-pin CQFP packages
- Low power, high output drive
  - Standby current typically 2 mA
  - 16-bit counter operating at 100 MHz consumes 50 mA
  - Minimum I_{OL} and I_{OH} of 8 mA
- Flexible logic cell architecture
  - Wide fan-in (up to 14 input gates)
  - Multiple outputs in each cell
  - Very low cell propagation delay (1.7 ns)
- PCI compliant I/O pins
- Powerful design tools—*Warp3*™
  - Designs entered in VHDL, schematics, or both
  - Fast, fully automatic place and route
  - Waveform simulation with back annotated net delays
  - PC and workstation platforms
- Robust routing resources
  - Fully automatic place and route of designs using up to 100 percent of logic resources
  - No hand routing required
- Input hysteresis provides high noise immunity
- Thorough testability
  - Built-in scan path permits 100 percent factory testing of logic and I/O cells
  - Automatic Test Vector Generation (ATVG) software supports user testing after programming
- 0.65µ CMOS process with ViaLink™ programming technology
  - High-speed metal-to-metal link
  - Non-volatile antifuse technology

Logic Block Diagram



313 PINS, 242 I/O CELLS, 6 INPUT HIGH DRIVE CELLS, 2 INPUT/CLK (HIGH DRIVE) CELLS

ViaLink is a trademark of QuickLogic Corporation.
Warp3 is a trademark of Cypress Semiconductor Corporation.

Software 5

Section Contents

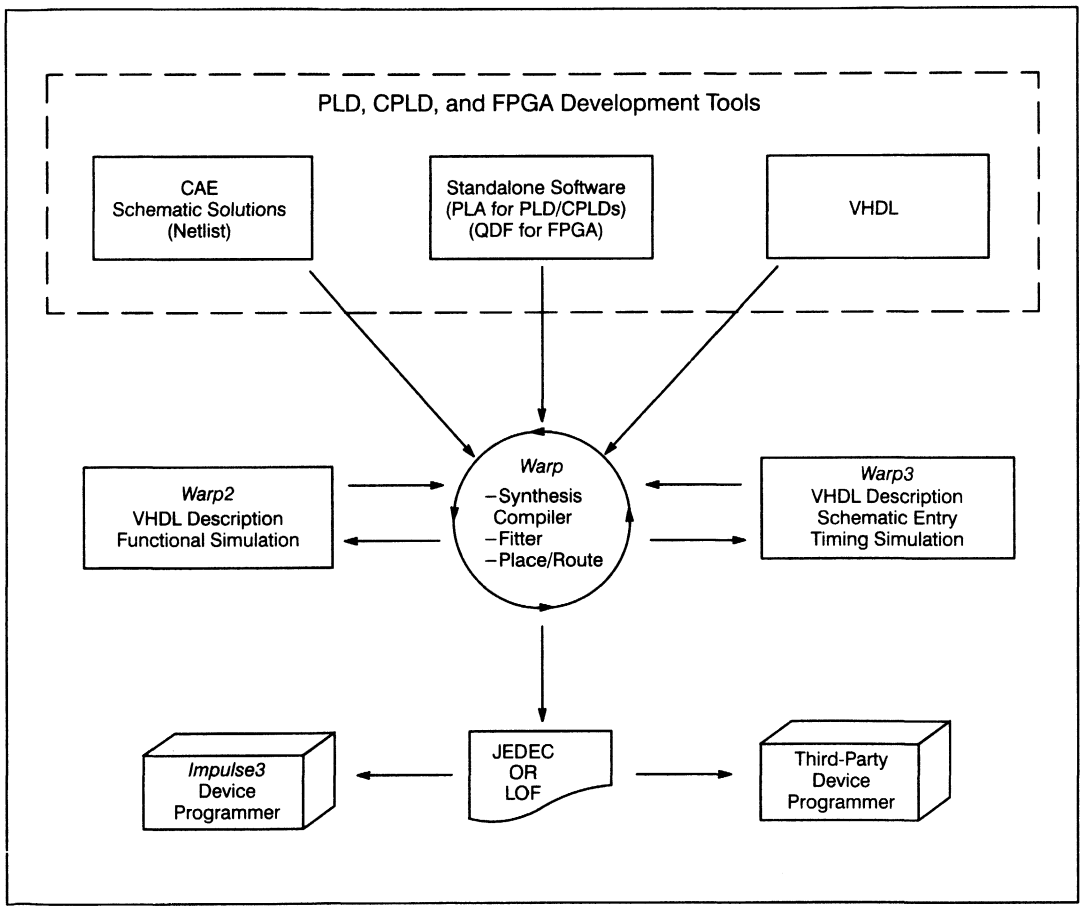
Software **Page Number**

PLD, CPLD, and FPGA Development Tools Overview

A large number of development tools are available for use when designing with Cypress Semiconductor's PLDs, CPLDs, and FPGAs. Many of these tools are available from Cypress, while additional design flow options are available from numerous third-party tool vendors. (For a complete listing of third-party tool vendors, see the Third-Party Tools datasheet.)

Development software is available that provides design entry, synthesis, optimization, fitting, place and route, and simulation. As shown below, this software produces a programming file for use with a device programmer. *Warp2*™ provides VHDL design description and functional simulation. *Warp3*™ includes *Warp2* functionality plus schematic entry and timing simulation. In addition, many third-party tools are available and provide various levels of support.

Device programmers use the programming file created by the development tool and program the PLD, CPLD, or FPGA. The *Impulse3*™ can program any Cypress device and can be upgraded to program other manufacturers' devices. Many third-party programmers are available that can be used to program a wide array of devices including those from Cypress.



Document #: 38–00370

Warp2™ CY3120/CY3125

VHDL Compiler for PLDs, CPLDs, and FPGAs

Features

- **VHDL (IEEE 1076) high-level language compiler**
  - **— VHDL facilitates device independent design**
  - **— VHDL designs are portable across multiple devices and/or CAD platforms**
  - **— VHDL facilitates the use of industry-standard simulation and synthesis tools for board and system-level design**
  - **— VHDL supports functions and libraries facilitating modular design activity**
- ***Warp2* provides synthesis for a powerful subset of IEEE standard VHDL including:**
  - **— enumerated types**
  - **— opeartor overloading**
  - **— for . . . generate statements**
  - **— integers**
- **State-of-the-art optimizations and reduction algorithms**
  - **— Optimization for flip-flop type (D type/T type)**
  - **— Automatic selection of optimal flip-flop type (D type/T type)**
  - **— Automatic pin assignment**
  - **— Automatic state assignment (grey code, one-hot, binary)**
- **Several design entry methods support multiple levels of abstraction:**
  - **— VHDL Behavioral (IF...THEN...ELSE; CASE...)**
  - **— State tables**
  - **— Boolean**
  - **— VHDL Standard (RTL)**
- **Designs can intermix multipleVHDL entry methods in a single design**
- **Supports all Cypress PLDs and PROMs, including MAX5000 and the state machine PROMs (CY7C258/9)**
- **Functional simulation provided with Cypress NOVA simulator:**
  - **— Graphical waveform simulator**
  - **— Entry and modification of on-screen waveforms**
  - **— Ability to probe internal nodes**
  - **— Display of inputs, outputs, and High Z signals in different colors**
  - **— Automatic clock and pulse creation**
  - **— Waveform to JEDEC test vector conversion utility**
  - **— JEDEC to symbolic disassembly**
  - **— Support for buses**
- **Hosted on IBM PC-AT**
- **Windows 3.1 on PCs**
- **OpenLook or Motif on Sun workstations**

Functional Description

Warp2™ is a state-of-the-art VHDL compiler for designing with Cypress PLDs and PROMs. *Warp2* utilizes a proper subset of IEEE 1076 VHDL as its Hardware Description Language (HDL) for design entry. VHDL provides a number of significant benefits for the design engineer. *Warp2* accepts VHDL input, synthesizes and optimizes the entered design, and outputs a JEDEC map or POF file for the desired device (see *Figure 1*). For simulation, *Warp2* provides the graphical waveform simulator from the NOVA.

VHDL Compiler

VHDL (VHSIC Hardware Description Language) is an open, powerful, non-proprietary language that is a standard for behavioral design entry and simulation. It is already mandated for use by the Department of Defense and supported by every major vendor of CAE tools. VHDL allows designers to learn a single language that is useful for all facets of the design process.

VHDL offers designers the ability to describe designs at different levels of abstraction. At the highest level, designs can be entered as a description of their behavior. This behavioral description is not tied to any specific target device. As a result, simulation can be done very early in the design to verify correct functionality, which significantly speeds the design process.

Warp2's VHDL syntax also includes support for intermediate level entry modes such as state table and boolean entry. At the lowest level, designs can be described using gate-level RTL (Register Transfer Language). *Warp2* gives the designer the flexibility to intermix all of these entry modes.

In addition, VHDL allows you to design hierarchically, building up entities in terms of other entities. This allows you to work either "top-down" (designing the highest levels of the system and its interfaces first, then progressing to greater and greater detail) or "bottom-up" (designing elementary building blocks of the system, then combining these to build larger and larger parts) with equal ease.

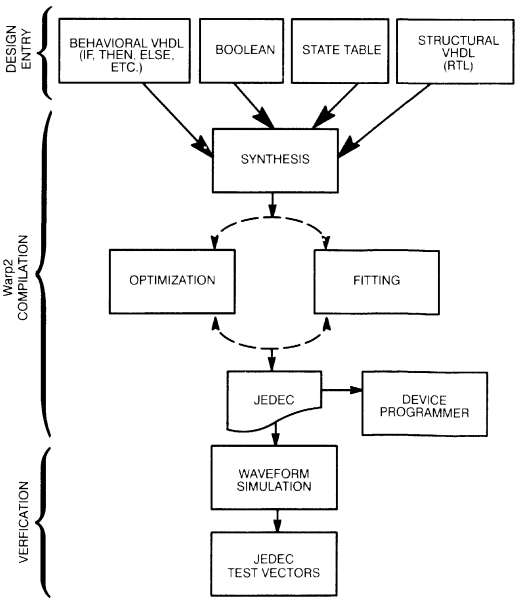


Figure 1. *Warp2* Design Flow

Because VHDL is an IEEE standard, multiple vendors offer tools for design entry, simulation at both high and low levels, and synthesis of designs to different silicon targets. The use of device independent behavioral design entry gives users the freedom to retarget designs to different devices. The wide availability of VHDL tools provides complete vendor independence as well. Designers can begin their project using *Warp2* for Cypress PLDs and convert to high volume gate arrays using the same VHDL behavioral description with industry-standard synthesis tools.

While design portability and device independence are significant benefits, VHDL has other advantages. The VHDL language allows users to define their own functions. User-defined functions allow users to extend the capabilities of the language and build reusable libraries of tested routines. As a result the user can produce complex designs faster than with ordinary "flat" languages. VHDL also provides control over the timing of events or processes. VHDL has constructs that identify processes as either sequential, concurrent, or a combination of both. This is essential when describing the interaction of complex state machines.

Cypress chose to offer tools that use the VHDL language because of the languages' universal acceptance, the ability to do both device and vendor independent design, simulation capabilities at both the chip and system level that improve design efficiency, the wide availability of industry-standard tools with VHDL support for both simulation and synthesis, and the inherent power of the languages' syntax.

VHDL is a rich programming language. Its flexibility reflects the nature of modern digital systems and allows designers to create accurate models of digital designs. Because of its depth and completeness, it is easier to describe a complex hardware system accurately in VHDL than in any other hardware description language. In addition, models created in VHDL can readily be transported to other CAD systems. *Warp2* supports a rich subset of VHDL including loops, for...generate statements, full hierarchical designs with packages, as well as synthesis for enumerated types and integers.

Designing with *Warp2*

Design Entry

Warp2 descriptions specify

1. The behavior or structure of a design, and
2. The mapping of signals in a design to the pins of a PLD (optional)

The part of a *Warp2* description that specifies the mapping of signals from the design to the pins of a PLD is called a binding architecture. It takes signal names from the design and matches them up with pin names from the PLD's entry in a library.

The part of a *Warp2* description that specifies the behavior or structure of the design is called an entity/architecture pair. Entity/architecture pairs, as their name implies, can be divided into two parts: an entity declaration, which declares the design's interface signals (i.e., tells the world what external signals the design has, and what their directions and types are), and a design architecture, which describes the design's behavior or structure.

Some users prefer to put the binding architecture for a design in one file, and the entity/architecture pair containing the design's behavioral or structural description in a different file. This allows you to isolate the device-dependent pin mapping in one file (the one containing the binding architecture), while leaving the device-independent behavioral or structural description in another (the one containing the entity/architecture pair). *Warp2* makes it easy to do this, offering separate analysis of files and easy reference to previously analyzed files by means of the USE clause.

Design Entity

If the entity/architecture pair is kept in a separate file, that file is usually referred to as the design entity file. The entity portion of a design entity file is a declaration of what a design presents to the outside world (the interface). For each external signal, the entity declaration specifies a signal name, a direction and a data type. In addition, the entity declaration specifies a name by which the entity can be referenced in a design architecture. In this section are code segments from four sample design entity files. The top portion of each example features the entity declaration.

Behavioral Description

The architecture portion of a design entity file specifies the function of the design. As shown in *Figure 1*, multiple design-entry methods are supported in *Warp2*. A behavioral description in VHDL often includes well known constructs such as If...Then...Else, and Case statements. Here is a code segment from a simple state machine design (soda vending machine) that uses behavioral VHDL to implement the design:

```
ENTITY drink IS
  PORT (nickel,dime,quarter,clock:in bit;
    returnDime,returnNickel,giveDrink:out bit);
END drink;


ARCHITECTURE fsm OF drink IS

TYPE drinkState IS (zero,five,ten,fif-
teen,twenty,twentyfive,owedime);
SIGNAL drinkstatus:drinkState;
ATTRIBUTE FSM_synthesis OF drinkStatus:signal
is sequential;


BEGIN

PROCESS BEGIN

 WAIT UNTIL clock = '1';

  giveDrink <= '0';
  returnDime <= '0';
  returnNickel <= '0';

  CASE drinkStatus IS

  WHEN zero =>
    IF (nickel = '1') THEN
      drinkStatus <= drinkStatus'SUCC(drink-
      Status);
        -- goto Five
    ELSIF (dime = '1') THEN
      drinkStatus <= Ten;
    ELSIF (quarter = '1') THEN
      drinkStatus <= TwentyFive;
    ENDIF;
  WHEN Five =>
    IF (nickel = '1') THEN
      drinkStatus <= Ten;
    ELSIF (dime = '1') THEN
      drinkStatus <= Fifteen;
    ELSIF (quarter = '1') THEN
```

5

```
      giveDrink <= '1';
      drinkStatus <= drinkStatus'PRED(drink-
Status);
        -- goto Zero
    ENDIF;

  WHEN oweDime =>
    returnDime <= '1';
    drinkStatus <= zero;

  when others =>
  -- This ELSE makes sure that the state
  -- machine resets itself if
  -- it somehow gets into an undefined state.
    drinkStatus <= zero;
  END CASE;
  END PROCESS;

END FSM;
```

VHDL is a highly typed language. It comes with several predefined operators, such as + and /= (add, not-equal-to). VHDL offers the capability of defining multiple meanings for operators (such as +), which results in simplification of the code written. For example, the following code segment shows that "count = count +1" can be written such that count is a bit vector, and 1 is an integer.

```
ENTITY sequence IS
  port (clk: in bit;
    s: inout bit);
end sequence;

ARCHITECTURE fsm OF sequence IS

SIGNAL count: INTEGER RANGE 0 TO 7;

BEGIN

PROCESS BEGIN

  WAIT UNTIL clk = '1';

    CASE count IS

    WHEN 0 | 1 | 2 | 3 =>
      s <= '1';
      count <= count + 1;
    WHEN 4 =>
      s <= '0';
      count <= count + 1;
    WHEN 5 =>
      s <= '1';
      count <= '0';
    WHEN others =>
      s <= '0';
      count <= '0';
    END CASE;

END PROCESS;

END FSM;
```

In this example, the + operator is overloaded to accept both integer and bit arguments. *Warp2* supports overloading of operators.

Functions

A major advantage of VHDL is the ability to implement functions. The support of functions allows designs to be reused by simply specifying a function and passing the appropriate parameters. *Warp2* features some built-in functions such as ttf (truth-table function). The ttf function is particularly useful for state machine or look-up table designs. The following code describes a seven-segment display decoder implemented with the ttf function:

```
ENTITY SEG7 IS
  PORT(
    inputs: IN BIT_VECTOR (0 to 3);
    outputs: OUT BIT_VECTOR (0 to 6)
  );
END SEG7;

ARCHITECTURE mixed OF SEG7 IS

CONSTANT truthTable:
  x01_table (0 to 11, 0 to 10) := (
-- input   &      output
-- ----------------------
  "0000"   &   "0111111",
  "0001"   &   "0000110",
  "0010"   &   "1011011",
  "0011"   &   "1001111",
  "0100"   &   "1100110",
  "0101"   &   "1101101",
  "0110"   &   "1111101",
  "0111"   &   "0000111",
  "1000"   &   "1111111",
  "1001"   &   "1101111",
  "101x"   &   "1111100", --creates E pattern
  "111x"   &   "1111100"
  );

BEGIN

    outputs <= ttf(truthTable,inputs);

END mixed;
```

Boolean Equations

A third design-entry method available to *Warp2* users is Boolean equations. *Figure 2* displays a schematic of a simple one-bit half adder. The following code describes how this one-bit half adder can be implemented in *Warp2* with Boolean equations:

```
--entity declaration
ENTITY half_adder IS
  PORT (x, y : IN BIT;
    sum, carry : OUT BIT);
END half_adder;
--architecture body
ARCHITECTURE behave OF half_adder IS
BEGIN
```

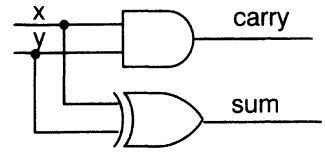


Figure 2. One-Bit Half Adder

```
  sum <= x XOR y;
  carry <= x AND y;
END behave;
```

Structural VHDL (RTL)

While all of the design methodologies described thus far are high-level entry methods, structural VHDL provides a method for designing at a very low level. In structural descriptions (also called RTL), the designer simply lists the components that make up the design and specifies how the components are wired together. *Figure 3* displays the schematic of a simple 3-bit shift register and the following code shows how this design can be described in *Warp2* using structural VHDL:

```
ENTITY shifter3 IS port (
    clk : IN BIT;
    x : IN BIT;
    q0 : OUT BIT;
    q1 : OUT BIT;
    q2 : OUT BIT);
  END shifter3;

ARCHITECTURE struct OF shifter3 IS
  SIGNAL q0_temp, q1_temp, q2_temp : BIT;
  BEGIN
    d1 : DFF PORT MAP(x,clk,q0_temp);
    d2 : DFF PORT MAP(q0_temp,clk,q1_temp);
    d3 : DFF PORT MAP(q1_temp,clk,q2_temp);
    q0 <= q0_temp;
    q1 <= q1_temp;
    q2 <= q2_temp;
  END struct;
```

All of the design-entry methods described can be mixed as desired. The ability to combine both high- and low-level entry methods in a single file is unique to VHDL. The flexibility and power of VHDL allows users of *Warp2* to describe designs using whatever method is appropriate for their particular design.

Binding Architecture

The purpose of a binding architecture is to map external signals of a design to the pins of a physical device. The binding architecture can be in a separate file or appended to the end of the design file.

Here is a binding architecture file for the 3-bit shift register described in the last example:

```
USE work.rtlpkg.all;
USE work.shift3pkg.all;
```

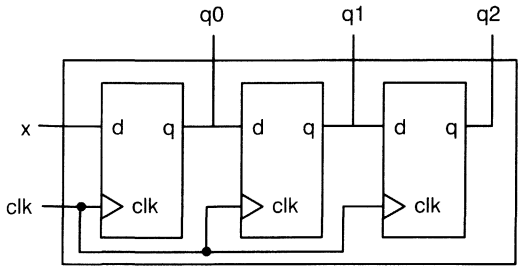


Figure 3. Three-Bit Shift Register Circuit Design

```
ARCHITECTURE shift3 OF c22v10 IS
  BEGIN
    SH1:shifter3 PORT MAP(
      clk     => pin1,
      x       => pin2,
      fbx(q0) => pin14,
      fbx(q1) => pin15,
      fbx(q2) => pin16);
  END shift3;
```

As indicated in the architecture statement, this design targets the Cypress 22V10 for implementing the specified function. By simply changing the architecture statement and appropriately modifying the pin assignments, a binding architecture file targeting other Cypress PLDs can easily be generated.

Compilation

Once a design entity and binding architecture have been completed, a design is compiled using *Warp2*. Although implementation is with a single command, compilation is actually a multistep process (as shown in *Figure 1*). The first step is synthesizing the input VHDL into a logical representation of the design. *Warp2* synthesis is unique in that the input language (VHDL) supports a very high level of abstraction. Competing PLD compilers require very specific and device-dependent information in the design input file.

The second step of compilation is an iterative process of optimizing the design and fitting the logic into the targeted PLD. Logical optimization in *Warp2* is accomplished with the Espresso algorithms. The optimized design is fed to the *Warp2* fitter, which applies the design to the specified target PLD. The *Warp2* fitter supports manual or automatic pin assignments as well as automatic selection of D or T flip-flops. After the optimization and fitting step is complete, *Warp2* automatically creates a JEDEC file for the specified PLD.

Simulation

Warp2 is delivered with Cypress's NOVA Simulator. NOVA features a graphical waveform simulator that can be used to simulate designs generated in *Warp2*. The NOVA simulator provides functional simulation and features interactive waveform editing and viewing. The simulator also provides the ability to probe internal nodes, automatically generate clocks and pulses, and to generate JEDEC test vectors from simulator waveforms.

Programming

The result of *Warp2* compilation is a JEDEC file that implements the input design in the targeted PLD. Using the JEDEC file, Cypress PLDs can be programmed on Cypress's *Impulse3*™ programmer or on any qualified third-party programmer.

System Requirements

For PCs

IBM PC-AT or equivalent (386 or higher recommended)

PC-DOS™ version 3.3 or higher

2 Mbytes of RAM (4 Mbytes recommended)

EGA, VGA, or Hercules™ monochrome display

20-Mbyte hard disk drive

1.2-Mbyte 5¼-inch or 1.44-Mbyte floppy disk drive

Two or three-button mouse

Windows® Version 3.1 or higher

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For Sun Workstations

SPARC CPU
Sun OS™ 4.1.1 or later
16 Mbytes of RAM
1.44-Mbyte 3½-inch disk drive

Ordering Information

CY3120 *Warp2* for Windows PLD Compiler includes:
- 3½-inch, 1.4-Mbyte floppy disks
- *Warp2* User's Guide
- *Warp2* Workbook
- *Warp2* Reference Manual
- Registration Card

CY3125 *Warp2* for Sun PLD Compiler includes:
- 3½-inch, 1.4-Mbyte floppy disks
- *Warp2* User's Guide
- *Warp2* Workbook
- *Warp2* Reference Manual
- Registration Card

Document #: 38-00218-A

Warp3 VHDL Development System for PLDs and FPGAs

Features

- **Sophisticated PLD/FPGA design and verification system based on VHDL**
- ***Warp3*™ is based on Viewlogic's Powerview™ (Sun) and Workview Plus™ (PC) design environments**
  - **Advanced graphical user interface for Windows and Sun Workstations**
  - **Schematic capture (Viewdraw™)**
  - **Interactive timing simulator (Viewsim™)**
  - **Waveform stimulus and viewing (Viewtrace™)**
  - **Textual design entry using VHDL**
  - **Mixed-mode design entry support**
- **The core of *Warp3* is an IEEE 1076 standard VHDL compiler**
  - **VHDL is an open, powerful design language**
  - **VHDL (IEEE standard 1076) facilitates design portability across devices and/or CAD platforms**
  - **VHDL facilitates the use of industry-standard simulation and synthesis tools for board and system-level design**
  - **VHDL facilitates hierarchical design with support for functions and libraries**
- **Support for ALL Cypress PLDs/FPGAs and PROMs, including:**
  - **Industry-standard 20- and 24-pin devices like the 22V10**
  - **Cypress 7C33X family of 28-pin PLDs**
  - **CY7C34X (MAX5000™ Series)**
  - **FLASH370™**
  - **pASIC38X**

Introduction

As the capacity and complexity of programmable logic increased dramatically over the last couple of years, users began to demand software tools that would allow them to manage this growing complexity. They also began to demand design-entry standards that would allow them to spend more time designing with PLDs rather than learning a vendor's proprietary software package. Thus, Hardware Description Languages (HDLs) in general, and VHDL (Very high speed integrated-circuit Hardware Description Language) in particular, have emerged as the standard methodology for integrated-circuit and system design.

While the design community debated whether VHDL could become the standard for PLDs, Cypress took an industry leading position by introducing the first native VHDL compiler for PLDs—our *Warp* tools.

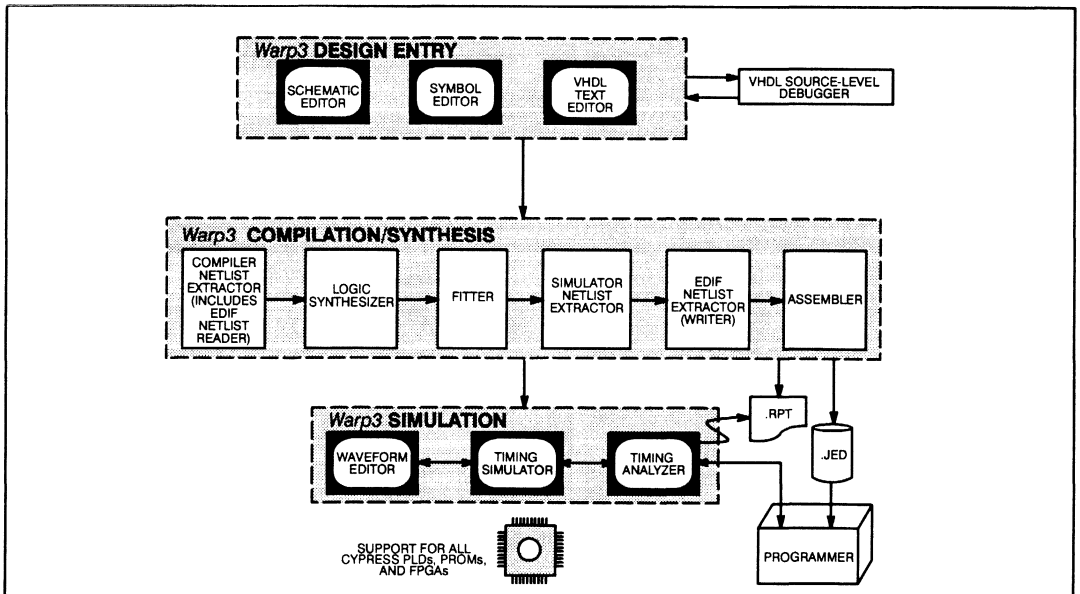


Figure 1. *Warp3* Design Flow

Functional Description

Warp3 is an integration of Cypress's advanced VHDL synthesis and fitting technology with Viewlogic's sophisticated CAE design environment. On the PC platform, *Warp3* includes Cypress' VHDL compiler and Viewlogic's Workview Plus V5.1 software for Microsoft Windows®. On the Sun platform, *Warp3* includes Cypress' VHDL compiler and Viewlogic's Powerview V5.1 software for OpenWindows™.

Design Flow

Figure 1 displays a block diagram of the typical design flow in *Warp3*. Designs can be entered in VHDL text, schematic capture or via an imported EDIF netlist. In fact, *Warp3* supports mixing these approaches on individual designs. Designs are then functionally verified using the *Warp3* functional simulator. The third step is to compile the design and target a PLD, PROM or FPGA. Post-synthesis, the waveform timing simulator is used to verify design timing as programmed in the chosen device. If the simulation results are satisfactory the JEDEC, HEX or netlist file is used to program the targeted device. A detailed description of each step follows.

Specifically, the *Warp3* Design Flow includes the following:

Viewlogic GUI
IEEE 1076 VHDL Synthesis
Schematic Capture (Viewdraw)
Hierarchy Navigator
Mix-mode Design Entry
Waveform Editor (Viewtrace)
VHDL Timing Simulator (VHDLsim™)
Device fitters for all Cypress PLD/CPLDs/PROMs
Automatic Place&Route for all Cypress FPGAs

The Cockpit

The Viewlogic graphical user interface (GUI) is built around a file/tool manager called "the cockpit". The cockpit is used to select the project and current toolset in use. The cockpit allows users to select from a variety of design environments called toolboxes. For UNIX workstations the GUI is under the PowerView cockpit and for PC/Windows the GUI is under the WorkView Plus cockpit (see *Figure 2*).

Design Entry

Text Editor

Text entry is done with industry standard VHDL. *Warp3* can synthesize a rich set of the VHDL language in conformance with IEEE standard 1076. This includes support for Behavioral, Boolean, State Table and Structural VHDL entry.

Text entry is ideal for describing complex logic functions such as state machines or truth tables. With VHDL, the behavior of a state machine can be described in concise, easily-readable code. Further, the hierarchical nature of VHDL allows very complex functions to be described in a modular, top-down fashion. For more information on VHDL see the *Warp2* (CY3120) datasheet.

Schematic Capture

Warp3 users can also to enter designs graphically with a sophisticated schematic capture system (Viewdraw). With schematic entry, designers can quickly describe a variety of common logic functions from simple gates to complex multipliers (see *Figure 3*).

Within *Warp3*, users have access to an extensive symbol library of standard components and macro functions. These include:

- adders/multipliers
- counters
- gates (AND, OR, NAND, NOR, XOR, XNOR, INV, & BUF)
- io (singles, buses, three-states, clk-pads, hd-pad, gnd, & vcc)
- macrocells
- memory (assorted flip-flops and latches)
- mux (decoders and multiplexers)
- registers, shift registers and universal registers
- 7400-ttl (commonly used parts)

In addition, the designer may create custom functions that can be used in any *Warp3* design.

Symbol Editor

The *Warp3* schematic capture tools also provide methods to create symbols for schematics. Using the VHDL2SYM utility, symbols are automatically generated from VHDL text files. Using the Viewgen™ utility, symbols are automatically generated from low-

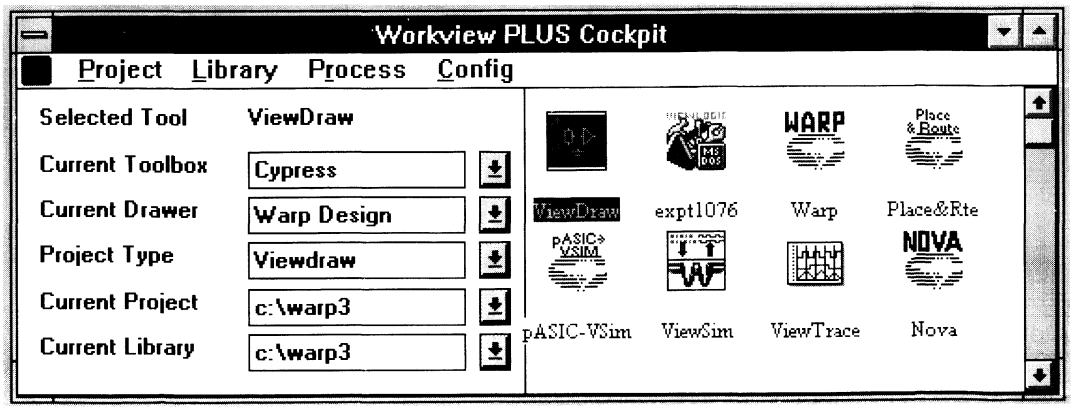


Figure 2. WorkView PLUS Cockpit for PC Workstations

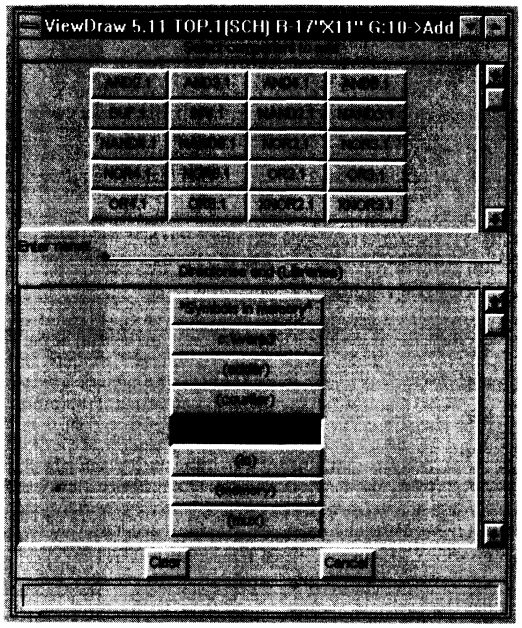


Figure 3. Typical Symbol Library

er-level schematic data. Symbols are useful for creating a design hierarchy to easily describe complex designs.

EDIF Input

Warp3 includes an EDIF netlist converter that provides a convenient way for designers to import designs from other CAE schematic capture and simulation tools. The EDIF-in tool supports EDIF version 2 0 0.

Mix-mode Entry

Perhaps the most powerful design entry methodology in *Warp3* is the combination of the above methods. In most designs, some portions of the circuit are most easily described in schematics while others are best described in text. Typically, standard logic components such as counters, adders and registers are best implemented by retrieving components from the *Warp3* schematic symbol library.

Meanwhile, text entry is usually preferred for describing sections of the circuit design that implement control logic. In particular, state machines are often much easier to describe with behavioral VHDL as opposed to schematic gates. Combining these methods in a single design simplifies the input process and shortens the design cycle time.

As mentioned above, *Warp3* can automatically generate symbols for text and schematic designs. This capability facilitates hierarchical design entry by allowing users to represent complex functions by a symbol. The top level of the design may be represented by the connection of a small number of symbols representing the main functional blocks. To move to lower levels in the design the user can push into selected symbols. If the underlying design is described in VHDL, a text window will be launched with the design file. If the underlying design is a schematic, a Viewdraw window will be opened with the design. There is no limit to the number of levels of hierarchy used or the number of symbols in a particular design.

Design Verification

Functional Simulation

Verifying functionality early in the design process can greatly reduce the number of design iterations necessary to complete a particular design. Using Viewsim the functionality of the design can be verified with textual stimulus from the keyboard or from a file. Viewtrace can be used in conjunction with Viewsim to simulate the design functionality graphically. The simulation process is described in detail below.

VHDL Source-level Debugger (Release 2)

A unique and powerful feature of *Warp3* is the source-level VHDL debugger. The VHDL debugger works in concert with the *Warp3* simulator and waveform editor. The debugger allows users to graphically step through VHDL code and monitor the results textually or in waveforms. After each single step the debugger highlights the VHDL text representing the current state of the simulation. Simultaneously waveform and text windows can display the inputs and outputs of the design.

Note that a design does not have to be entered in VHDL text to use the VHDL debugger. Since *Warp3* converts all facets of a design (schematic, EDIF-in etc.) to VHDL before compilation, this VHDL representation can be single stepped to verify design functionality.

Hierarchy Navigator

Another powerful debugging tool within *Warp3* is the hierarchy navigator (Viewnav). The navigator allows users to select a net or node at one level of the design and automatically trace that net through all levels of the hierarchy. This is very useful for tracing signal paths when looking for design errors.

Compilation

VHDL Synthesis

- **For synthesis *Warp3* supports a rich subset of VHDL including**
  - **— Enumerated types**
  - **— Integers**
  - **— For . . . generate loops**
  - **— Operator overloading**

Once design entry is complete and functionality has been verified, the entire design is converted to VHDL using the "Export 1076" utility on schematic modules. At this point in the design there is a VHDL description of the entire design. This VHDL description is fed to the Cypress VHDL compiler for translation to a device programming file. Although compilation is a multistep process, it appears as a single step to the user (as shown in *Figure 1*).

The first step in compilation is synthesizing the input VHDL into a logical representation of the design in terms of components found in the target device (AND gates, OR gates, flip-flops etc.). *Warp3* synthesis is unique in that the input language (VHDL) supports a very high level of abstraction. Competing PLD compilers require very specific and device-dependent information in the design file.

5

Device Fitting

- **State-of-the-art optimization and reduction algorithms**
  - **— Optimization for flip-flop type (D type/T type)**
  - **— Automatic pin assignment**
  - **— Automatic state assignment (Gray code, binary, one-hot)**

For PLDs and FPGAs, the second phase of the compilation is an iterative process of optimizing the design and fitting the logic into the targeted device (see *Figure 4*). Logical optimization in *Warp3* is accomplished with Espresso algorithms. Once optimized, the design is fed to the device-specific fitter which applies the design to the selected device (see *Figure 5*). *Warp3* fitters support manual or automatic pin assignments as well as automatic selection of D-type or T-type flip-flops. After optimization and fitting are complete, *Warp3* will create a JEDEC file (PLDs) or a LOF file (FPGAs) implementing the users design.

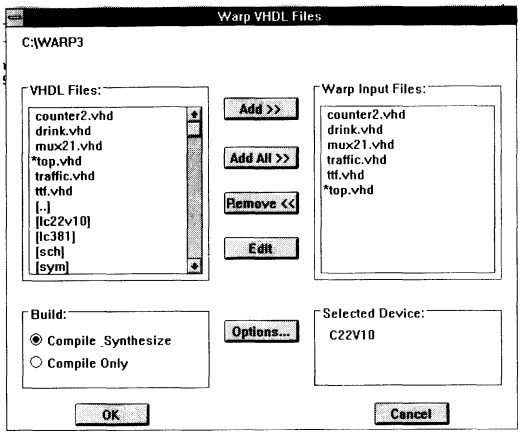


Figure 4. Compile/Synthesize Dialog Box

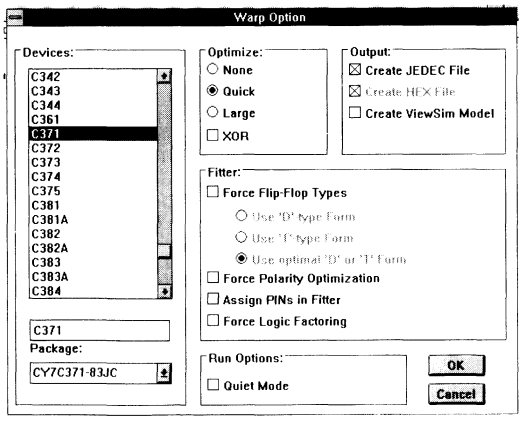


Figure 5. Device Fitting/Routing Dialog Box

Automatic Place&Route

- **Completely automatic place and route**
  - **— Includes timing back annotation into Viewsim**

For Cypress FPGAs, the second phase of the design process is called place&route. The place&route tools in *Warp3* take the logical design description from synthesis and apply it to the cells of the targeted FPGA. Once placed, the programmable interconnect channels are programmed to connect logic blocks as required by the design. With Cypress FPGAs and *Warp3*, the place&route process is 100% automatic. No tedious manual intervention or hand tweaking is necessary. Once place&route is finished, *Warp3* generates a netlist that is used to program the FPGA.

Automatic Error Locating

Of course, the compilation process may not always go as planned. VHDL syntax errors should be identified and corrected in the pre-synthesis functional simulation stage. During the compilation phase *Warp3* will detect errors that occur in the fitting/place&route process. *Warp3* features automatic error location that allows problems to be diagnosed and corrected in seconds. Errors from compilation are displayed immediately in a pop-up window. If the user highlights a particular error, *Warp3* will automatically highlight the offending line in the entered design. If the device fitting or place&route process includes errors, a pop-up window will again describe them. Further, a detailed report file is generated indicating the resources required to fit the input design and any problems that occurred in the process.

Simulation

The last step in the design process before programming is verifying the timing of your design. For this, *Warp3* includes the Viewsim VHDL timing simulator. During compilation, delays that result from fitting the input design are "written" into an internal file for use by the *Warp3* simulator. This information represents worst-case path delays for the design as fit in the selected device. Delays are based on the type of device and speed grade selected.

One of the ways to simulate is with the command-line interface to Viewsim. From the command line, the designer can specify the state of inputs (high, low, X, etc.) and watch how outputs behave over a specified time frame. In this way users can easily step through test cases and view the output results. Stimulus can be entered from the command line or from a file.

Waveform Editor

A graphical method of simulation uses the Viewlogic waveform editor, Viewtrace, in conjunction with Viewsim. With Viewtrace users can input stimulus from a file or graphically via digital waveforms. Outputs are viewed as digital waveforms that reflect the timing delays of the device as programmed. Viewtrace is interactive, allowing modifications of the stimulus and re-simulation of the results without re-running synthesis tools.

If user inputs violate device specifications the *Warp3* simulator will detect the violation and warn the user. For example, if an input changes immediately before a CLK rise (violating the device set-up time) *Warp3* will issue a warning and highlight the offending signal. The same occurs for all other timing violations.

Programming

After the design is compiled and verified, the targeted device is ready for programming. The program file generated in *Warp3* (a JEDEC file or LOF file) is used as input to a device programmer. Cypress offers the *Impulse3* programmer, based on Data I/O's ChipLab™, that programs all Cypress PLDs and FPGAs. Alternatively, customers can use any one of several qualified 3rd party pro-

grammers from corporations like Data I/O, SMS and Logical Devices.

System Requirements

PC Platform

80486-based IBM PC
MicroSoft Windows V3.1 or higher
16 Mbytes of RAM
60-Mbyte Disk Space
1.44 Mbyte 3.5 inch floppy disk drive

Sun Platform

SPARC CPU
Sun OS 4.1.1 or later
Motif or OpenLook GUI
16 Mbytes of RAM
130 Mbytes of Disk Space
Cartridge Tape

Ordering Information

CY3130 *Warp3* PLD Development System on the PC includes:
- 3 1/2-inch 1.44-Mbyte floppy disks
- *Warp3* Viewlogic hardware key
- *Warp3* User's Guide
- *Warp3* Reference Manual
- Registration Card

Document #: 38-00242-C

CY3131[1] *Warp3* PLD Development System on the PC (for current Viewlogic Users of Workview Plus) includes:
- 3 1/2-inch 1.44-Mbyte floppy disks
- *Warp3* User's Guide
- *Warp3* Reference Manual
- Registration Card

CY3135 *Warp3* PLD Development System on a UNIX/SUN Workstation includes:
- Three Cartridge Tapes
  1) Viewlogic Software
  2) *Warp3* Software
  3) Viewlogic On-line Documentation
- *Warp3* User's Guide
- *Warp3* Reference Manual
- Registration Card

CY3136[2] *Warp3* PLD Development System on a UNIX/SUN Workstation (for current Viewlogic Users of Powerview) includes:
- One Cartridge Tapes of *Warp3* Software
- *Warp3* User's Guide
- *Warp3* Reference Manual
- Registration Card

Notes:

1. This is a "Bolt-in" Solution and requires the customer to be a current User of Viewlogic's Workview Plus S/W
2. This is a "Bolt-in" Solution and requires the customer to be a current User of Viewlogic's Powerview S/W.

5

CYPRESS

Impulse3™

Device Programer

Features

- **OEM version of Data I/O ChipLab™**
- **Programs all Cypress PROMs, EPROMs, PLDs, CPLDs, and FPGAs**
- **Modular for easy device-specific support**
- **Easy to use DOS-based, PC interface**
- **New device support available with floppy disk software change**
- **DIP adapter included with base unit**
- **Mouse-driven user interface**
- **On-line documentation and device support list**
- **One-year warranty**
- **Dimensions of *Impulse3* are 25 x 25 x 7.6 cm or 9.75 x 9.75 x 3 in and the weight is 1.02 kg or 2.25 lbs.**

Functional Description

Impulse3 is Cypress's OEM version of the Data I/O ChipLab. It provides programming support for all of Cypress' programmable devices. The programmer uses a DOS-based PC interface to provide an easily accessible programming environment. The PC's parallel port is used to communicate with the programmer, and device-specific adapters and drivers to ensure that you get the specific device support you need for your programming application.

Impulse3 uses industry standard JEDEC, HEX (for PROMs), and LOF (for pASIC380) data format for programming and can be upgraded by Data I/O to support products from other vendors.

System Requirements

The *Impulse3* works with your IBM compatible PC computer. The minimum system requirements are:

- **One free parallel port**
- **Minimum 2-MB extended memory**
- **Intel® 286 (not recommended), 386, 486 or Pentium™ processor**
- **DOS version 3.3 or higher**
- **5 MB of free hard disk space for the programmer drivers and programs**
- **High Density floppy disk drive (3.5- or 5.25-inch)**
- **Microsoft®-compatible mouse**

Device Support

Impulse3 supports all Cypress Programmable products. The base unit (CY3500) supports DIP devices up to 44 pins. For other device/package combinations, an adapter is required. In addition, devices over 44 pins require a high pin-count adapter (CY3501). The *Impulse3* products are sold modularly so that you can adapt them to your specific device support needs.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Input Voltage	90 to 264 Vac, 48 to 63 Hz
Programmer Voltage	24V (AC or DC) ±10%
Programmer Current	AC = 1.67 Å, DC = 1.25 Å
Operating Temperature	0°C to 40°C
Storage Temperature	−40°C to 55°C
Relative Humidity (Operating)	20% to 80%
Relative Humidity (Storage)	10% to 90%
Operating Altitude	to 5,000 Meters
Storage Altitude	to 15,000 Meters

Ordering Information

Part Number	Description
CY3500	*Impulse3* base unit and DIP adapter for all DIP packaged devices.
CY3501	Adapter for high pin count devices including pASIC380 and FLASH370 Family
CY3509	28-pin PLCC for CY7C34x
CY3511	44-pin PLCC PPI for the CY7C34x
CY3512	44-pin PLCC PPI for the CY7C37x
CY3513	44-pin PLCC PPI for CY7C38x
CY3514	68-pin PLCC PPI for CY7C34x
CY3515	68-pin PLCC PPI for CY7C38x
CY3516	84-pin PLCC PPI for CY7C34x
CY3517	84-pin PLCC PPI for CY7C37x
CY3518	84-pin PLCC PPI for CY7C38x
CY3521	144-pin TQFP PPI for pASIC380 family
CY3522	100-pin TQFP PPI for CY7C37x
CY3523	100-pin TQFP PPI for pASIC380 family
CY3524	176-pin PGA PPI for CY7C34x, CY7C37x
CY3525	145-pin PGA PPI CY7C38x
CY3526	85-pin PGA PPI for CY7C34x
CY3527	85-pin PGA PPI for CY7C37x
CY3528	85-pin PGA PPI for CY7C38x
CY3529	69-pin PGA PPI for CY7C34x
CY3530	69-pin PGA PPI for CY7C38x
CY3535	100-pin PQFP PPI for CY7C34x
CY3536	84-pin PLCC for CY7C34x
CY3538	160-pin CQFP for CY7C37x, CY7C38x
CY3004A	28-pin LCC adapter for PAL22V10
CY3005	20-pin LCC adapter for PAL20, PALC20 families
CY3006A	28-pin PLCC adapter for PAL22V10
CY3007	20-pin PLCC adapter for PAL20, PALC20 families
CY3008	28-pin LCC adapter for 265, 269, 330, 331, 332, 335
CY3009	28-pin PLCC adapter for 265, 269, 330, 331, 332, 335
CY3010	28-pin LCC adapter for 20G10, 20RA10
CY3011	28-pin PLCC adapter for 20G10, 20RA10
CY3014	24-pin SOIC adapter for CY7C251
CY3017	32-pin PLCC adapter for CY7C251
CY3019	24-pin CerPack adapter for 245, 261, 263, 291
CY3020	28-pin CerPack adapter for 251, 330, 331, 332, 271, 265
CY3021	20-pin CerPack adapter for PAL20, PALC20, families
CY3024	32-pin LCC adapter for 256, 266, 271, 274, 277, 279, 286
CY3027	32-pin LCC adapter for CY7C287
CY3043	32-pin PLCC adapter for CY7C201
CY3044	32-pin PLCC adapter for 256, 271, 266, 274, 277, 279, 286
CY3045	32-pin PLCC adapter for CY7C287

Document #: 38–00374

Third-Party Tools

Cypress Semiconductor provides a complete solution for PLD, CPLD, and FPGA development and programming with its *Warp2*™ and *Warp3*™ development software and *Impulse3*™ device programmer. Additionally, a wide array of third-party tool vendors also provide support for Cypress devices. These third-party tools are available directly from the third-party tool vendor.

The following vendors provide support for some of Cypress's devices. Please contact the vendor directly for the most up-to-date information on specific features and device support.

Programming Support

BP Microsystems
1000 N Post Oak Road
Houston, TX 77055–7237
(713) 688–4600

Data I/O Corporation
10525 Willows Rd., N.E.
P.O. Box 97046
Redmond, WA 98073–9746
(206) 881–6444

Digelec Corporation
1602 Lawrence Ave.
Suite 113
Ocean, NJ 07712
(201) 493–2420

P.O. Box 380
Herzliya, Israel
(97) 252–559615

Logical Devices Inc.
692 S. Military Trail
Deerfield Beach, FL 33442
(305) 428–6868

SMS Mikrocomputersysteme GmbH
Im Morgental 13, D–8994 Hergatz
Germany 5018
(49) 7522–5018 (phone)
(49) 7522–8929 (fax)

17411 NE Union Hill Rd. #100
Redmond, WA 98052
(206) 883–8447

Stag Microsystems
1600 Wyatt Dr.
Santa Clara, CA 95054
(408) 988–1118
STAG ZL32 Rev. 30A03

Third-Party Development Software

Data I/O Corporation (ABEL™, Synario™)
10525 Willows Rd. N.E.
P.O. Box 97046
Redmond, WA 98073–9764
(206) 881–6444

Exemplar Logic, Inc (CORE™)
2550 Ninth Street, Suite 102
Berkeley, CA 94710
(510) 849–0937

ISDATA GmbH (LOG/iC™)
Haid-und-Neu-Strasse 7
D–7500 Karlsruhe 1
Germany
(0721) 69 30 92

P.O. Box 19278
Oakland, CA 94619
(510) 531–8553

Logic Modeling Corporation
(SmartModels™)
19500 NW Gibbs Dr.
PO Box 310
Beaverton, OR 97075
(503) 690–6900

Logical Devices Inc. (CUPL™)
692 S. Military Trail
Deerfield Beach, FL 33442
(305) 428–6868

Minc Incorporated (PLDesigner™)
6755 Earl Rd.
Colorado Springs, CO 80918
(719) 590–1155

OrCAD (OrCAD™)
3175 NW Aloclek Dr.
Hillsboro, OR 97124
(503) 690–9881

Synopsys (FPGA Compiler™,
Design Compiler™)
700 E. Middlefield Rd.
Mountain View, CA 94043–4033
(415) 962–5000

ViewLogic Systems (Workview Plus™,
Powerview™, Proseries™)
293 Boston Post Rd. West
Marlboro, MA 01752
(508) 480–0881

Test and Prototype Sockets

Yamaichi Electronics, Inc
(408) 452–0797

Nepenthe
(800) NEPENTHE

CTI Technologies, Inc
(602) 998–1484

Test Sockets:

Package	Yamaichi Part	Nepenthe Part
44 Pin PLCC	IC51–0444–400	PC1–044050–002
84 Pin PLCC	IC51–0844–401	PC1–084050–003
100 Pin TQFP	IC51–1004–809	QP1–100050–048
160 Pin TQFP	IC51–1604–1350	QP1–160065–010

Prototype Sockets:

Package	Yamaichi Part
44 Pin PLCC	TPL–044–T–S–100
84 Pin PLCC	TPL–084–T–S–100
100 Pin TQFP	IC149–100–025–S5

Document #: 38–00371

Quality and Reliability 6

Section Contents

Quality and Reliability

PLD Programming Information

Introduction

PLDs, or programmable logic devices, provide an attractive alternative to logic implemented with discrete devices. Cypress Semiconductor is in the enviable position of being able to offer PLDs in several different process technologies, thus assuring our customers of a wide range of options for leading-edge speed as well as very low power consumption. Cypress optimizes the mix of technology and device architecture to insure that the programmable logic requirements of today's highest-performance electronics systems can be fully supported by a single PLD vendor.

Cypress offers a wide variety of PLDs based on our leading-edge CMOS EPROM process technology. This technology facilitates the lowest power consumption and the highest logic density of any nonvolatile PLD technology on the market today, at speeds that are as fast as state-of-the-art bipolar technology would provide. Furthermore, these devices offer the user the option of device erasure and reprogrammability in windowed packages. Cypress also offers a number of PLDs based on our state-of-the-art BiCMOS and bipolar technologies. These PLDs are targeted at applications where power consumption and density are not as critical as leading-edge speed. Cypress offers PLDs based on CMOS Flash technology. The ViaLink™ Technology provides OTP FPGAs with high-speed and routability. Thus Cypress offers solutions for state-of-the-art systems regardless of what the optimal balance is between speed, power, and density for any particular system.

Programmable Technology

EPROM Process Technology

EPROM technology employs a floating or isolated gate between the normal control gate and the source/drain region of a transistor. This gate may be charged with electrons during the programming operation, permanently turning off the transistor. The state of the floating gate, charged or uncharged, is permanent because the gate is isolated in an extremely pure oxide. The charge may be removed if the device is irradiated with ultraviolet energy in the form of light. This ultraviolet light allows the electrons on the gate to recombine and discharge the gate. This process is repeatable and therefore can be used during the processing of the device, repeatedly if necessary, to assure programming function and performance.

Two Transistor Cells

Cypress uses a two-transistor EPROM cell. One transistor is optimized for reliable programming, and one transistor is optimized for high speed. The floating gates are connected such that charge injected on the floating gate of the programming transistor is conducted to the read transistor turning it off.

BiCMOS and Bipolar Process Technology

In addition to CMOS, Cypress offers BiCMOS TTL and bipolar ECL I/O-compatible PLDs. The BiCMOS devices offer the advantages of CMOS (high density and low power) and bipolar (high speed). Both the BiCMOS and bipolar devices are one-time fuse programmable. The fuses are Ti-W and are connected directly to first metal. First metal is a reliable composite of Ti-TiW-AlSi-Ti to ensure excellent electromigration resistance, eliminate contact spiking, and minimize hillocking.

Flash Process Technology

The Flash cell is programmed in the same manner as the EPROM cell, and is electrically erased via Fowler-Nordheim tunneling. This next-generation PLD technology will combine a number of key advantages for future Cypress PLDs. The principal advantages will be leading-edge speed, low CMOS power consumption, and electrical alterability for simplified inventory management. In addition, Flash technology offers two inherent advantages for PLDs over the commonly used full-features EE CMOS technology. One is its superior migratability to higher logic densities, due to the smaller Flash cell size. The second is superior reliability, due to the Flash cell's higher immunity to voltage transients and the accompanying risk of data corruption.

pASIC™ Process Technology

Programmable devices implement customer-defined logic functions by interconnecting user-configurable logic cells through a variety of semiconductor switching elements. The maximum speed of operation is determined by the effective impedance of the switch in both programmed, ON, and unprogrammed, OFF, states.

In pASIC380 devices, the switch is called a ViaLink element. The ViaLink element is an antifuse formed in a via between the two layers of metal of a standard CMOS process. The direct metal-to-metal link created as a result of programming achieves a connection with resistance values as low as 50 ohms. This is less than 5 percent of the resistance of an EPROM or SRAM switch and 10 percent of that of a dielectric antifuse. The capacitance of an unprogrammed ViaLink site is also lower than these alternative approaches. The resulting low RC time constant provides speeds two to three times faster than older generation technologies.

In a ViaLink programmable ASIC device, the two layers of metal are initially separated by an insulating semiconductor layer with resistance in excess of 1 gigaohm. A programming pulse of 10 to 12 volts applied across the via forms a bidirectional conductive link connecting the top and bottom metal layers.

Programming Algorithm—EPROM, BiCMOS and Flash Technology

Byte Addressing and Programming

Most Cypress programmable logic devices are addressed and programmed on a byte or extended byte basis where an extended byte is a filed that is as wide as the output path of the device. Each device, or family of devices, has a unique address map that is available in the product datasheet. Each byte, or extended byte, is written into the addressed location from the pins that serve as the output pins in normal operation. To program a cell, a 1, or HIGH, is placed on the input pin and a 0, or LOW, is placed on pins corresponding to cells that are not to be programmed. Data is also read from these pins in parallel for verification after programming. A 1, or HIGH, during program verify operation indicates an unprogrammed cell, while a 0, or LOW, indicates that the cell accessed has been programmed.

Blank Check

Before programming, all programmable logic devices may be checked in a conventional manner to determine that they have not been previously programmed. This is accomplished in a program verify mode of operation by reading the contents of the array. During this operation, a 1, or HIGH, output indicates that the ad-

dressed cell is unprogrammed, while a 0, or LOW, indicates a programmed cell.

Programming the Data Array

Programming is accomplished by applying a supervoltage to one pin of the device causing it to enter the programming mode of operation. This also provides the programming voltage for the cells to be programmed. In this mode of operation, the address lines of the device are used to address each location to be programmed, and the data is presented on the pins normally used for reading the contents of the device. Each device has a read/write pin in the programming mode. This signal causes a write operation when switched to a supervoltage and a read operation when switched to a logic 0 or LOW. In the logic HIGH or 1 state, the device is in a program inhibit condition and the output pins are in a high-impedance state. During a write operation, the data on the output pins is written into the addressed array location. In a read operation, the contents of the addressed location are present on the output pins and may be verified. Programming therefore is accomplished by placing data on the output pins and writing it into the addressed location. Verification of data is accomplished by examining the information on the output pins during a read operation.

The timing for actual programming is supplied in the unique programming specification for each device.

Phantom Operating Modes

All Cypress programmable logic devices on the EPROM and BiCMOS technology contain a Phantom array for post assembly testing. This array is accessed, programmed, and operated in a special Phantom mode of operation. In this mode, the normal array is disconnected from control of the logic, and in its place the Phantom array is connected. In normal operation the Phantom array is disconnected and control is only via the normal array. This special feature allows every device to be tested for both functionality and performance after packaging and, if desired, by the user before programming and use. The Phantom modes are entered through the use of supervoltages and are unique for each device or family of devices. See specific device datasheets for details.

Special Features

Cypress programmable logic devices, depending on the device, have several special features. For example, the security mechanism defeats the verify operation and therefore secures the contents of the device against unauthorized tampering or access. In advanced devices such as the PALC22V10, PLDC20G10, and CY7C330, the macrocells are programmable through the use of the architecture bits. This allows users to more effectively tailor the device architecture to their unique system requirements. Specific programming is detailed in the device datasheet.

Programming Algorithm—pASIC380 Family

The metal interconnections of pASIC devices can be considered as a vertical and horizontal grid of metal lines. Both ends of the metal line grids are connected to internal shift registers which control the connection of the end of the wire to the programming voltage, ground, or an open. Non-contiguous wires are connected for programming purposes by pass transistors, which are also controlled by the shift registers.

Individual ViaLink fuses can be "addressed" by turning on various pass transistors and (from the shift registers) driving the wires that connect to both sides of the fuse to be programmed. Applying a programming voltage (V_{PP}) to the device, the shift register contents directs the voltage to the ViaLink fuse, which becomes programmed.

Once a fuse is programmed, it has shorted two wires of the wire grid. This can cause other fuses to become "unaddressable." For this reason, fuses must be programmed in a specific order. This ordering is determined by the development tool. Programming is achieved by loading the internal shift registers with the required data and then applying the programming pulse for the fuse(s) to be programmed. The programming pulse is required to meet specific timing and current limit specifications.

Entering the programming mode is accomplished by applying supervoltages on specific pins. The shift registers are accessed in a variety of modes which permit rapid programming as well as specific internal test features. These test modes allow complete testing of devices during manufacture.

The unprogrammed device has all internal logic cell input gates in the unconnected state. Consequently, applying V_{CC} to an unprogrammed device will cause large currents to flow that can cause irreparable damage to the device. Under no circumstances should V_{CC} be applied to an unprogrammed pASIC.

After the device is programmed, the test modes can also be used to verify the device programming. The development tools provide automatic test vector generation (ATVG). These vectors can be used with appropriately equipped programmers to provide post program testing.

Document #: 38-00164-B

Reliability Report

Introduction

The Cypress pASIC380 family of very high speed FPGAs is built by integrating the ViaLink™ metal-to-metal antifuse programming element into a standard high-volume CMOS gate array process.

Reliability testing of pASIC™ devices is part of a continuous process to insure long-term reliability of the product. It consists of industry-established accelerated life tests for basic CMOS devices plus additional stress tests. The addition of two high-voltage life tests stresses the unprogrammed and programmed ViaLink elements beyond conventional CMOS reliability testing.

Results to date, from the evaluation of over 1700 pASIC devices from multiple wafer lots, indicate that the addition of the ViaLink element to a well-established CMOS process has no measurable effect on the reliability of the resulting product. There have been no failures in 31 million equivalent device hours of high-temperature operating life. The observed failure rate is 0 FITs, and the failure rate at a 60% confidence level is 29 FITs.

Process Description

The pASIC devices are fabricated using a standard, high-volume 1-μm CMOS gate array process with twin-well, single-poly, and double-layer metal interconnect. This technology has been qualified to meet MIL-STD-883C. Over 1.1×10^9 equivalent device hours of operating life test have been accumulated since volume production began in 1989.

The technology employs a high-integrity TiW-Al+Cu+TiW metal system that offers very low contact resistance through the use of pTSi contacts, high resistance to electromigration, and freedom from stress-induced opens.[1]

The basic CMOS technology[2] features LDD-type transistors with a gate oxide thickness of 200Å. BPSG applied over the polysilicon lines is reflowed after contact formation giving a sloped entry for metal one. The interlevel dielectric is planarized with spin-on-glass. Vias are wet/dry etched, giving sloped walls for good metal two-step coverage. Interconnect metal lines contain layers of TiW on both sides of standard Al+Cu alloy.

The ViaLink element is located in an intermetal oxide via between the first and second layers of metal. It is created by depositing a very high resistance silicon film in a standard size metal one to metal two via. The silicon deposition is done at low temperature and causes no change to the properties of the CMOS transistors. When deposited at low temperatures, silicon forms an amorphous structure that can be electrically switched from a high-resistance state ($\cong 1$ GΩ) to a low-resistance state ($\cong 50$ GΩ) for an off-to-on ratio of 2×10^7. QuickLogic takes advantage of this property to create the ViaLink metal-to-metal antifuse programming element (see *Figure 1*).

The programming voltage of the ViaLink element varies with amorphous silicon thickness. For a desired programming voltage between 10-12 volts, the thickness of the amorphous silicon film is approximately 1000Å. This is ideal for good process control and minimizes the capacitive coupling effect of an unprogrammed element located between the two layers of metal.

Amorphous silicon is deposited with standard semiconductor manufacturing equipment and processing techniques. In addition to antifuse elements, it is used in the high-volume fabrication of image sensors, decode, and drive circuits for flat panel displays, and high-efficiency solar cells.

Failure Mechanisms in the pASIC Device

A variety of failure mechanisms exists in CMOS integrated circuits. Since the overall failure rate is composed of various failure mechanisms, each having different temperature dependence and thus varying time-temperature relationships, it is important to understand the characteristics of each contributing failure mechanism. *Table 1* lists nine key failure mechanisms that have been characterized for standard CMOS devices, plus the two mechanisms for the programmed and unprogrammed ViaLink elements.

Various accelerated life tests are used to detect the possible contribution of each mechanism to the overall failure rate of the device. Failure rate data taken at elevated temperature can be translated to a lower temperature through the Arrhenius equation. This equation, in the form of an acceleration factor, A_f, can be written as

$$A_f = \exp[-E_a/k(1/T_s - 1/T_o)] \qquad \text{Eq. 1}$$

where T_s is the stress temperature, T_o is the operating temperature of the device, E_a is the activation energy for that mechanism, and k is the Boltzmann constant.

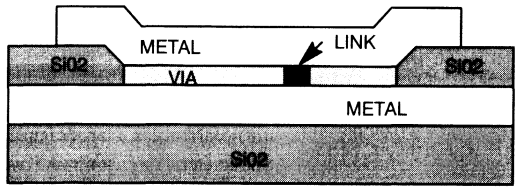


Figure 1. Cross Section of a ViaLink Antifuse

Table 1. Failure Mechanisms That May Be Operative in pASIC Devices

Failure Mechanism	t_{50} Dependence	Activation Energy (E_a)	Detection Tests
Insulator breakdown (leakage, opens)	exp(−β/E) value of β depends on the dielectric and may be temperature dependent.	Approx. 0.3 eV for SiO_2 and dependent on E	High-voltage operating life test (HTOL)
Parameter shifts due to contamination (such as Na)	exp(E_a/kT) (Arrhenius)	1.0 eV	High-temperature bias
Silicon defects (leakage, etc.)	Arrhenius	0.5 eV	High-voltage and guard-banded tests
Metal line opens from electromigration	$\frac{Wt}{J^2}$ exp(E_a/kT)	Approx. 0.7 eV for Al+Cu alloys	HTOL
Masking and assembly defects	Arrhenius	0.5 eV	High-temperature storage and HTOL
Shorts channel charge trapping (V_T and g_m shifts)	$g_m \cong$ exp(−AE)	Approx. −0.06 eV	Low-temperature, high-voltage operating life test
Stress-induced open metal (operative only on non-clad metal systems)	$W^m t^p$ exp (E_a/kT) (m and p range from 1.3 to 4.7)	0.6 to 1.4 eV (E_a difficult to reproduce)	Temperature cycling
Open metal from electrolytic corrosion	$(\%RH)^{-4.5}$ exp(E_a/kT)	0.3 to 0.6	High-temperature/ high-humidity/bias test
Wire bond failure from excessive gold-aluminum interdiffusion	$1/(Dt)^{1/2}$ where D = D_0exp(E_a/kT)	0.7 eV	HTOL
Unprogrammed ViaLink	exp(−BE)	0 eV	High V_{CC} static life test
Programmed ViaLink	exp(−PJ)	Approx. 0 eV	High V_{CC} operating life test

In *Table 1*, t_{50} is the mean time to failure, E is the electric field, E_a is the activation energy, k is the Boltzmann constant (8.62×10^{-5} eV/°K), W is the metal width, t is the metal thickness, J is current density, g_m is transconductance, V_T is the threshold voltage, A is a constant, m and p are constants, T is the absolute temperature, RH is the relative humidity, and D is the diffusion constant.

Accelerated Life Tests on 7C382

The purpose of a life test is to predict the reliability and failure rate of a device. However, a device operating under normal operating conditions would require years of testing to determine its long-term reliability. Methods of accelerating failures developed in the industry allow accurate prediction of a device life time and failure rate in a much shorter time duration. Accelerated stress tests are run at high temperature, high voltages, or a combination of both. *Table NO TAG* contains the results of the tests performed on a programmed 7C382, where approximately 3500 ViaLink elements were programmed and about 75,000 ViaLink elements were left unprogrammed. These numbers are typical for a fully utilized device.

A failure is defined as any change in the DC characteristic beyond the datasheet limits and any measurable change in the AC performance.

The overall reliability of the 7C382 devices as indicated by the results of the tests shown in *Table NO TAG* is 29 FITs with a 60% confidence.

Details of each of the tests of *Table 2* are given in the following sections. The failure mechanisms specific to the ViaLink antifuse element are described in detail. All tested devices were in the 68-lead plastic leaded chip carrier (PLCC) package.

Standard CMOS Tests and Results

HTOL is the life test that operates the device at a high V_{CC} and high temperature. This test is used to determine the long-term reliability and failure rate of the device in the customer environment. The specific condition of this test is defined by the MIL-STD-883C Quality Conformance Test. The devices are operated at 5.5V and 125°C for 1000 hours. The acceleration due to temperature can be calculated by using *Equation 1*, assuming an average activation energy of 0.7 eV and an operating temperature of 55°C. The observed failure rate in FITs is

$$\text{Failure Rate} = (\text{failures}) \times (10^9 \text{ device-hrs})/(\text{total equivalent device-hrs}) \qquad \text{Eq. 2}$$

The generally reported failure rate is a 60% confidence level of the observed FITs. The failure rate at this confidence level is calculated using Poisson statistics since the distribution is valid for a low failure occurrence in a large sample.

The acceleration factor from *Equation 1*, for 55°C and $E_a = 0.7$ eV is 78. Therefore, from the results shown in *Table 3*, the 7C382 has been operating for more than 31 million equivalent device hours without a failure. The observed failure rate is 0 FITs and the failure rate at a 60% confidence levels is 29 FITs.

Table 2. Results of Accelerated Life Tests on the 7C382

Test	Process Qual. Acceptance Requirements	Test Results
HTOL, 1,000 hrs, 125°C, V_{CC} = 5.5V, MIL-STD-883C, Method 1005	≤100 FITs @ 55°C, E_a = 0.7 eV, 60% confidence	0 observed FITs, 29 FITs at a 60% confidence, 40 units from 4 lots
High-temperature storage, 1,000 hrs., 150°C, unbiased	≤1% cumulative failures per test	0%, 105 units from 3 lots
THB, 1,000 hrs., alternately biased, 85% R.H., 85°C, JEDEC STD 22-B, Method A101	≤1% cumulative failures per test	0%, 300 units from 3 lots
Temperature cycle, 1,000 cycles, −65°C to 150°C, MIL-STD-883C, Method 1010	≤1% cumulative failures per test	0%, 110 units from 4 lots
Thermal shock, 100 cycles, −65°C to 150°C, 883C, Method 1011	≤1% cumulative failures per test	0%, 105 units from 3 lots
Pressure Pot, 168 hrs., 121°C, 2.0 atm., no bias	≤1% cumulative failures per test	0%, 105 units from 3 lots
High V_{CC} static life, 1,000 hrs., 25°C, V_{CC} = 7.0V static	<20 FITs due to unprogrammed ViaLink element, A_f = 130	0 observed FITs, 363 units from 5 lots
High V_{CC} dynamic life, 1,000 hrs., 25°C, V_{CC} = 6.0V, 15 MHz	<20 FITs due to programmed ViaLink element, A_f = 380	0 observed FITs, 300 units from 3 lots, 1 failure not related to ViaLink element

Table 3. Results of High-Temperature Operating Life Test
(V_{CC} = 5.5V, Temp. = 125°C, f = 1 MHz, 68-Lead PLCC)

Fab Lot	Quantity	Failures @ Hours		
		168	500	1,000
18362	100	0	0	0
19194	100	0	0	0
19618	100	0	0	0
20454	100	0	0	0

High-Temperature Storage

High-temperature storage test is a 150°C, 1,000-hour, unbiased bake. This test accelerates failures due to mobile charge, such as sodium. The results in *Table 4* demonstrate the stability of the programmed and unprogrammed ViaLink element and the long-term shelf life of the 7C382.

Table 4. Results of High-Temperature Operating Life Test
(V_{CC} = 5.5V, Temp. = 125°C, f = 1 MHz, 68-Lead PLCC)

Fab Lot	Quantity	Failures @ Hours		
		168	500	1,000
18362	35	0	0	0
19194	35	0	0	0
19390	35	0	0	0

Temperature, Humidity, and Bias (85/85)

The temperature, humidity, and bias test is performed under severe environmental conditions. The device is exposed to a temperature of 85°C and a relative humidity of 85% for 1,000 hours, which the pins are alternately biased between 0 and 5.5 volts (JEDEC STD 22-B). This test is effective at detecting corrosion problems, while also stressing the package and bonding wires. *Table 5* shows that the 7C382 had no failures.

Table 5. Results of Temperature, Humidity, and Bias Test
(85% R.H., Temp. = 85°C, pins alternately biased at 5.5V, 68-Lead PLCC)

Fab Lot	Quantity	Failures @ Hours		
		168	500	1,000
19194	100	0	0	0
19618	100	0	0	0
19454	100	0	0	0

Temperature Cycle Tests

The temperature cycle test stresses the packaged part from −65°C to 150°C for 1,000 cycles. The air-to-air cycling follows the MIL-STD-883C Quality Conformance Test. This test checks for any problems due to the thermal expansion stresses. The plastic package, lead frame, silicon die, and die materials expand and contract at different rates. This mismatch can lead to cracking, peeling, or delamination of the high-stress layers. The results in *Table 6* show that the 7C382 had no failures.

Table 6. Results of Temperature Cycle Test
(85% R.H., Temp. = 85°C, pins alternately biased at 5.5V, 68-Lead PLCC)

Fab Lot	Quantity	Failures @ Hours		
		250	500	1,000
16921	5	0	0	0
18362	35	0	0	0
19194	35	0	0	0
19618	35	0	0	0

Thermal Shock Tests

The thermal shock test cycles the packaged part through the same temperatures as the temperature cycle test except that the cycling is done from liquid to liquid. The temperature change is nearly instantaneous in this case. The rapid temperature change can result in higher stresses in the package and lead frame. The results in *Table 7* show that the 7C382 had no failures.

Table 7. Results of Thermal Shock Test
(Liquid to Liquid, −65°C to 150°C, 68-Lead PLCC)

Fab Lot	Quantity	Failures @ Cycle
		100
18362	35	0
19194	35	0
19618	35	0

Pressure Pot Tests

The pressure pot test is performed at 121°C at 2.0 atmospheres of saturated steam with devices in an unbiased state. This test forces moisture into the plastic package and tests for corrosion in the bonding pads and wires that are not protected by passivation. Corrosion can also occur in passivated areas where there are micro cracks or poor step coverage 7C382 had no failures, as shown in *Table 8*.

Table 8. Results of Pressure Pot Test
(Pressure = 2.0 atm., Temp. = 121°C, no bias, 68-Lead PLCC)

Fab Lot	Quantity	Failures @ Hours		
		48	96	168
18362	35	0	0	0
19194	35	0	0	0
19618	35	0	0	0

ViaLink Element Reliability Tests and Results

The ViaLink antifuse is a one-time programmable device. In the unprogrammed state it has a resistance of greater than one gigaohm and capacitance of less than one femtofarad.

The application of a programming voltage across the antifuse structure, above a critical level causes the device to undergo a switching transition through a negative resistance region into a low-resistance state. The magnitude of the current allowed to flow in the low-resistance state, the programming current, is predetermined by design. A link of tungsten, titanium, and silicon alloy is formed between metal one and metal two during the programming process.

The link has a metallic-like resistivity of the order of 500 microohms-cm and is responsible for the low 50-ohm resistance that is a unique characteristic of the ViaLink antifuse.

The link forms a permanent, bidirectional connection between two metal lines. The size of the link, and hence the resistance, depends on the magnitude of the programming current. *Figure 6* shows the relationship between programming current and programmed link resistance. *Figure 3* shows the distribution of link resistance for a fixed programming current.

Unprogrammed ViaLink Element Reliability

Reliability studies on an antifuse that can exist in two stable resistance states, must focus on the ability of an unprogrammed and a programmed device under stress to remain in the desired state. In the context of standard IC testing, the antifuse should be stressed under conditions similar to those for a dielectric (in the unprogrammed state) and for a conductor (in the programmed state).

For ViaLink elements in the unprogrammed state, the tests must determine their ability to withstand applied voltages over the range of operating conditions without changing resistance or becoming programmed. Amorphous materials might be expected to show gradual changes in resistance as a result of relaxation or annealing. Reliability studies have been designed to explore these effects.

When a ViaLink element is stressed at high electric fields, its resistance can decrease from the initial 1 GΩ value. The reliability testing program examined the time for the resistance to reach 50 MΩ at different stress fields. *Figures 4* and *5* illustrate that because of time constraints (≅ 500 years), it is impossible to detect this effect at normal operating fields in systems.

The pASIC device is designed to operate with resistance of the unprogrammed ViaLink element from 50 MΩ, the pASIC product would remain within the guaranteed speed and standby I_{CC} specifications.

Figure 4 shows the time required for a ViaLink element to reach 50 MΩ under various applied electric fields at different temperatures. The time required for the change is not accelerated by temperature over the studied range of electric fields. The activation energy, E_a, for this process is zero.

Figure 5 shows the time required for a ViaLink element to reach 50 MΩ under various electric field stresses. A range of amorphous silicon thicknesses have been included in this chart. The data can be modeled using the equation

$$t_{50M\Omega} = t_0 \exp(-BE) \qquad \text{Eq. 3}$$

where the time to 50 MΩ decreases exponentially with increasing applied electric field. The constant t_0 is $3x10^{15}$ seconds and the field acceleration factor, B, is 20 cm/MV. The model is valid for electric fields, E, below 1.6 MV/cm. Above this field, programming occurs. The electric field for 5.0 volt V_{CC} operation with a typical amorphous silicon thickness is 0.61 MV/cm, which extrapolates $t_{50M\Omega}$ to $1.5x10_{10}$ seconds, or 500 years. The time to 50 MΩ for the worst-case amorphous silicon thickness and operating at worst-case V_{CC} is in excess of 30 years.

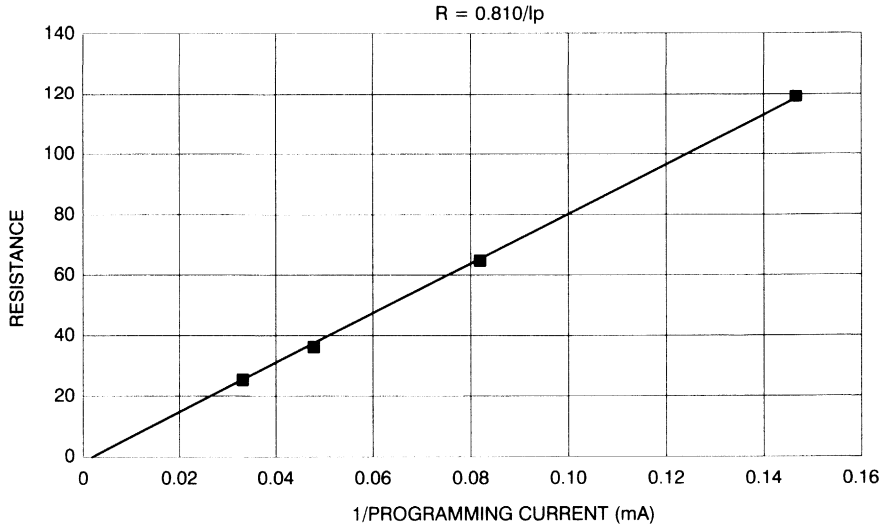


Figure 2. Resistance Versus 1/Programming Current

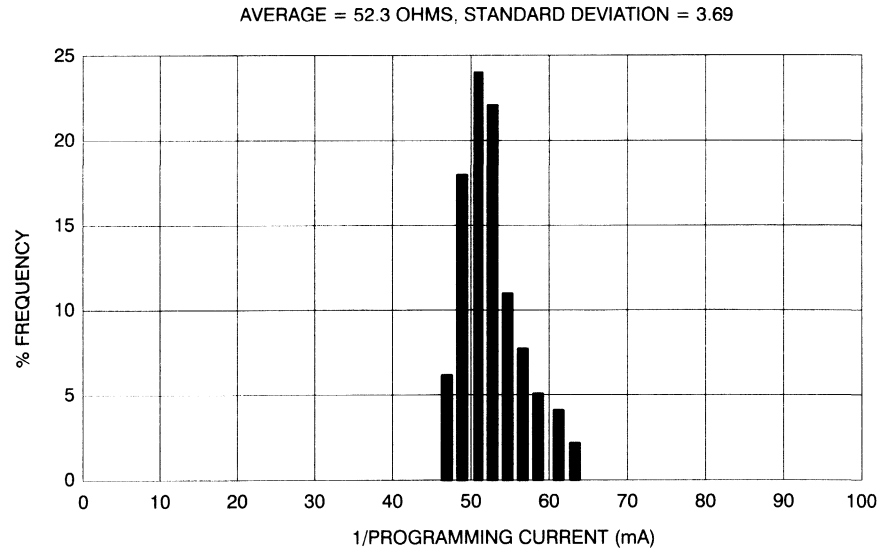


Figure 3. Distribution of ViaLink Resistance at Ip = 15 mA

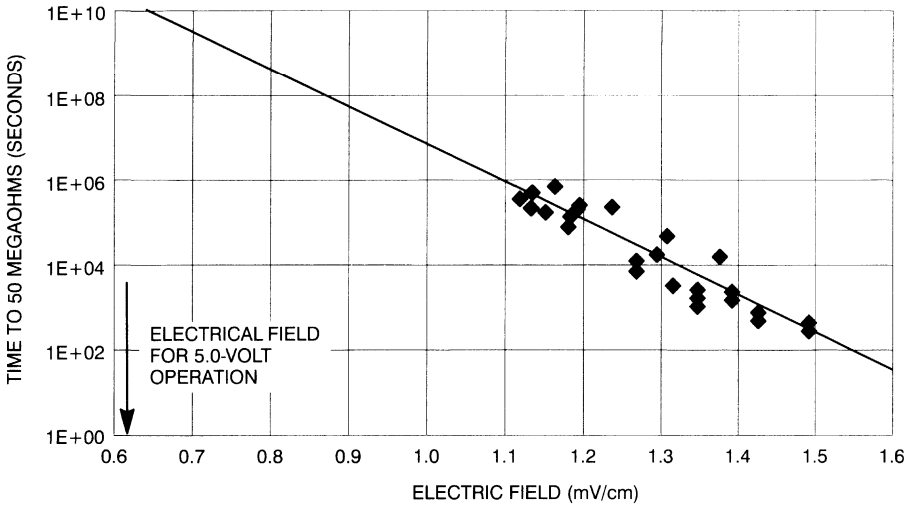


Figure 4. Electric Field Acceleration of Unprogrammed ViaLink Element

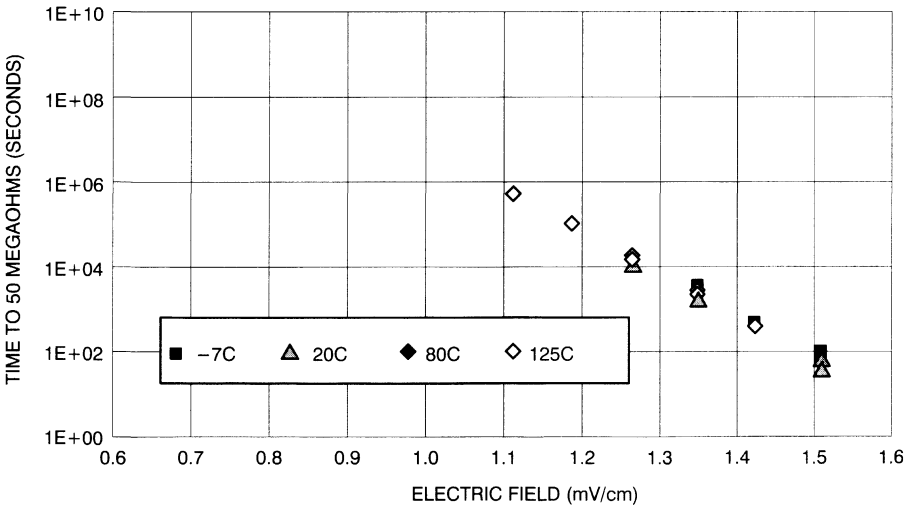


Figure 5. Temperature Dependence of Time to 50 Megaohms (Lot 617, Wafer 8)

The high field effect is both predicable and reproducible. This effect is inherent to the amorphous silicon in the ViaLink element[3]. The pASIC device has been designed to operate where the effect is minimized and has no impact on the reliability of the pASIC device.

Accelerated Stress Tests for Unprogrammed ViaLink Elements

The high field effect is created in the packaged 7C382 device through a high V_{CC} static life test. This test stresses the unprogrammed ViaLink element with a V_{CC} = 7.0 volts for 1000 hours. Over 360 7C382 devices from four lots have been tested. This condition stresses over 20,000 unprogrammed ViaLink elements in each 7C382. The failure criteria for the pASIC device for this test is the same as that of the previous tests, with emphasis placed on the standby I_{CC}, which increases as the resistance of the unprogrammed ViaLink element decreases. The acceleration factor for this stress is calculated by using *Equation 3* to find the ratio of the t_{50M} for E = 0.61 MV/cm at 5 volts and E = 0.85 MV/cm at 7 volts. This test has an acceleration factor = 130 for the unprogrammed ViaLink element. The test results in *Table 9* show that no device has failed this stress in more than 73 million equivalent device hours. Life tests continue to run; two lots have reached 1,500 hours, and one lot has exceeded 3,500 hours.

Table 9. Results of High V_{CC} Static Life Test
(V_{CC} = 7.0V Static, Temp. = 25°C, 68-Lead PLCC)

Fab Lot	Quantity	Failures	Total Hours
16558	14	0	3,650
18362	39	0	1,907
19194	110	0	1,756
19618	101	0	1,456
20454	100	0	1,000

Programmed ViaLink Element Reliability

The reliability tests on the programmed ViaLink element must demonstrate the stability of the link resistance in the programmed state. While an increase in resistance of the programmed device may not be catastrophic, a higher resistance can affect the device operating speed. Because the programmed ViaLink element has become part of the on-chip interconnect, reliability tests should be similar to those that are normally used to validate the integrity of metal interconnects.

In operation, the programmed ViaLink elements are subjected to capacitive switching current of the interconnect network. They do not experience any DC current or voltage (see *Figure 6*). Each switching pulse forces a capacitive charging current to flow through programmed ViaLink elements into the network on the rising edge, and an opposite, or discharging current, to flow on the falling edge. Each cycle is analogous to a read pulse for a memory device. A 10% change in resistance was set as the read disturb criteria for the ViaLink element. The typical impedance of a network is about 500Ω with the programmed ViaLink element contributing 50Ω. A 10% increase in the ViaLink resistance will increase the network impedance by approximately 5Ω or 1%. This increase in resistance will increase a network delay in the pASIC device by about the same proportion.

Programmed ViaLink elements were stressed under severe capacitive currents. AC stresses rather than DC stresses were used to accelerate the failures for closer correlation with actual operation. The mean number of read cycles to disturb, N_{50}, for

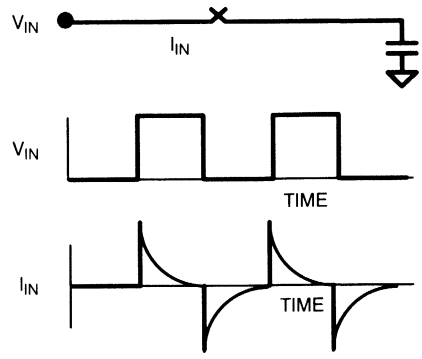


Figure 6. Switching of Programmed ViaLink Antifuse

various temperatures were found to be identical. The absence of temperature dependence indicates an $E_a \cong 0$. *Figure 7* shows the acceleration of the read disturb at high AC current densities through the programmed ViaLink element. Thus, the number of cycles to disturb can be modeled as

$$N_{50} = N_0 \exp(-PJ) \qquad \text{Eq. 4}$$

where $N_0 = 7x10_{41}$ cycles is a constant, P = 1.2 cm^2/mA is the current density acceleration factor, and J is the peak AC current density through the link.

The 7C382 is designed to operate at worst-case AC current density of $40x10^6$ A/cm^2. The N_{50} for this condition is $1x10^{21}$ cycles. The failure rate can be calculated using the cumulative density F(t),

$$F(t) = \phi \ln [N/N_{50}/\sigma] \qquad \text{Eq. 5}$$

The failure distribution can be determined by plotting the data on a log normal probability scale versus the log of the number of cycles to failure (see *Figure 8*). The shape parameter, σ, is $\ln(N_{50}/N_{16}) = 2.5$.

High AC current density occurs at low frequencies where there is sufficient time for the network to be fully charged or discharged. At frequencies above 50 MHz, AC current through a ViaLink element decreases due to incomplete charging and discharging cycle. The worst-case pattern in a programmed pASIC has less than 150 ViaLink elements operating at $40x10^6$ A/cm^2. Most of the programmed ViaLink elements operate at much lower current densities. Using *Equation 5*, the cumulative failure rate for the ViaLink element operating at $40x10^6$ A/cm^2 for $1.6x10^{16}$ read cycles (equivalent to continuous operation at 50 MHz for 10 years) is 0.6 parts per million. This failure rate for the pASIC device is 90 parts per million operating under worst-case condition for 10 years. The failure rate of the programmed ViaLink element would contribute 1 FIT to the overall failure rate of the pASIC device.

Accelerate Stress Tests for Programmed ViaLink Elements

The high V_{CC} dynamic life test stresses the 7C382 with V_{CC} = 6.0 volts at 15 MHz for 1,000 hours. This test stresses the programmed ViaLink elements at $45x10^6$ A/cm^2 for $5.4x10^{13}$ cycles. The acceleration factor, calculated from *Equation 4*, is 380. This test is equivalent to $2.0x10^{16}$ switching cycles, or continuous operation under worst-case condition at 50 MHz for 12 years. Three hundred 7C382 devices from 3 lots have been stressed. The failure criteria is the same as previously described, with emphasis placed on careful monitoring of AC performance. Test results in *Table 10* show that there have been no failures of the programmed ViaLink elements in over 34 million equivalent device hours.

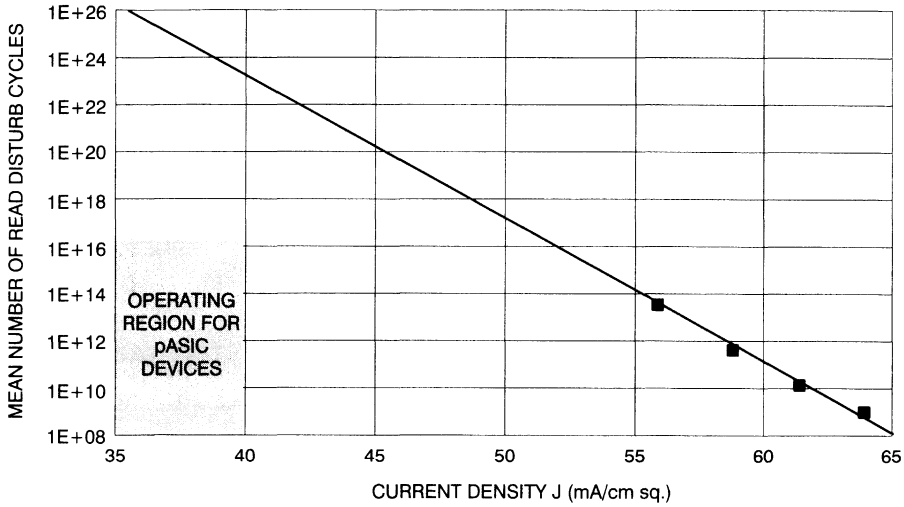


Figure 7. Acceleration of Read Disturb for Programmed ViaLink Element

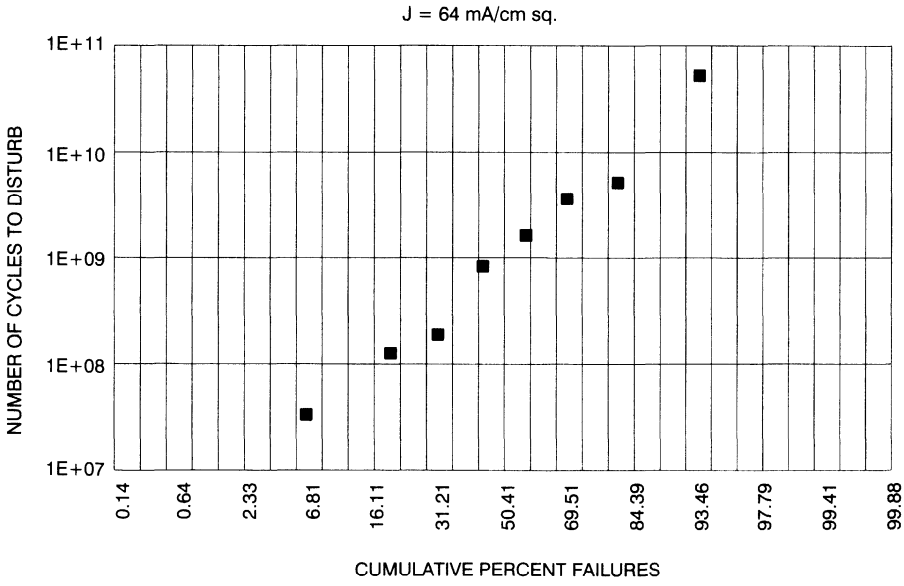


Figure 8. Distribution of Read Disturb on Programmed ViaLink Elements

Table 10. Results of High V_{CC} Dynamic Life Test
(V_{CC} = 6.0V, Temp. = 25°C, 15 MHz, 68-Lead PLCC)

Fab Lot	Quantity	Failures @ Hours		
		168	500	1,000
19194	100	0	0	0
19618	100	1[1]	0	0
20454	100	0	0	0

Note:
1. I_{CC} failure. Not a ViaLink element related failure. Failure analysis revealed a particle under M2 causing a short.

One failure, which was not associated with the ViaLink element, was observed during this test. Failure analysis on this part revealed a particle under the second metal that caused a short. This failure was due to an oxide defect and is highly accelerated by voltage stress. This device, which failed at the 6.0-volt stress, may not have failed had it been subjected to the standard 5.5-volt HTOL stress.

Conclusion on Life Tests

The testing reported here establishes the reliability of the 7C382. No failures have been observed in 31 million equivalent device hours of high-temperature operating life. The observed failure rate is 0 FITs and the failure rate with a 60% confidence is 29 FITs. The acceleration factors that can lead to the degradation of the programmed and unprogrammed ViaLink elements were studied. The pASIC devices are designed to operate at voltages and currents where the failure rate of the ViaLink element does not measurably increase the failure rate of the pASIC device above that of normal CMOS products.

Document #: 38–00375

References

1. Jim Nulty, et al, *A High Reliability Metallization System for a Double Metal 1.5 µm CMOS Process*, Proc. Fifth IEEE VMIS, 1988, PP. 453–459.

2. Dipankar Pramanik, et al, *A High Reliability Triple Metal Process for High-Performance Application-Specific Circuits*, Proc. Eighth IEEE VMIS, 1991, pp. 27–33

3. F. Yonezawa, *Fundamental Physics of Amorphous Semiconductors*, Proc. of the Kyoto Summer Inst., 1981.

Power Characteristics of Cypress Programmable Logic Products

This application note presents and analyzes the power dissipation characteristics of Cypress programmable logic products. The knowledge and tools presented here will help you manage power when using Cypress CMOS products.

Design Philosophy

The design philosophy for all Cypress products is to achieve superior performance at reasonable power dissipation levels. The CMOS technology, circuit design techniques, architecture, and topology are carefully combined to optimize the speed/power ratio.

Power Dissipation Sources

Power is dissipated both inside and outside ICs. The internal and external power have a quiescent (or DC) component and a frequency-dependent component. The relative magnitudes of each depend upon the circuit design objectives.

In circuits designed to minimize power dissipation at low to moderate performance, the frequency-dependent component is significantly greater than the DC component. In the high-performance circuits designed and manufactured by Cypress, the frequency-dependent power component is much lower than the DC component. This is because a large percentage of the internal power is dissipated in linear circuits such as sense amplifiers, bias generators, and voltage/current references, which are required for high performance.

Frequency-Dependent Power

CMOS circuits inherently dissipate significantly less power than either bipolar or NMOS circuits. The ideal CMOS circuit has no direct current path between V_{CC} and V_{SS}. In circuits using other technologies, such paths exist, and DC power is dissipated while the device is in a static state.

The principal component of power dissipation in a power-optimized CMOS circuit is the transient power required to charge and discharge the capacitances associated with the inputs, outputs, and internal nodes. This component is commonly called CV^2 power and is directly proportional to the operating frequency, f.

The charge, Q, stored in a capacitor, C, that is charged to a voltage, V, is given by the equation:

$$Q = CV \qquad \text{Eq. 1}$$

Dividing both sides of *Equation 1* by the time required to charge and discharge the capacitor (one period, or T) yields:

$$\frac{Q}{T} = \frac{CV}{T} \qquad \text{Eq. 2}$$

By definition, current (I) is the charge per unit time and

$$f = \frac{1}{T}$$

Therefore,

$$I = CVf \qquad \text{Eq. 3}$$

The power (P = VI) required to charge and discharge the capacitor is obtained by multiplying both sides of *Equation 3* by V:

$$P = VI = CV^2f \qquad \text{Eq. 4}$$

It is standard practice to assume that the capacitor is charged to the supply voltage (V_{CC}), so that

$$P = V_{CC}\, I = CV_{CC}^{\ 2} f \qquad \text{Eq. 5}$$

The total power consumption for CMOS systems depends upon the operating frequency, the number of inputs and outputs, the total load capacitance, the internal equivalent (device) capacitance, and the static (quiescent) or standby power consumption. In equation form:

$$P_d = [C_{INT}F_{INT} + C_{load}F_{load}]V_{CC}^{\ 2} + I_{quiescent}V_{CC} = I_{CC}V_{CC} \qquad \text{Eq. 6}$$

The first four quantities are frequency dependent, the last is not. This same equation can be used to describe the power dissipation of every IC in the system. The total power dissipation is then the algebraic sum of the individual components.

The relative magnitudes of the various terms in the equation are device dependent. Note that *Equation 6* must be modified if all of the internal nodes or all of the outputs are not switching at the same frequency.

Transient Power

Cypress devices incorporate N-well CMOS inverters that can affect the devices' transient power consumption. In an ideal N-well CMOS inverter, the P-channel pull-up transistor and the N-channel pull-down transistor (which are in series with each other between V_{CC} and V_{SS}) are never on at the same time. Thus, there is no direct current path between V_{CC} and ground, and the quiescent power is very nearly zero.

In the real world, when the input signal makes the transition through the linear region (i.e., between logic levels), both the N-channel and P-channel transistors are partially turned on. This creates a low-impedance path between V_{CC} and V_{SS} whose resistance equals the sum of the N- and P-channel resistances.

Calculating Power for the pASIC380

Since the pASIC380 family of devices is programmable, determining active power is difficult in that it is dependent on the functions implemented in the pASIC and the frequency of the internal nodes. To obtain a reasonably accurate estimate of the power consumption for a particular pASIC ™ design, a calculation must be made that sums the power for each contributor in the device. This section presents the details of how this is accomplished.

Static Power

The pASIC family of devices does not have sense amplifiers, but they do have an internal bias generator, which typically uses about 2 mA for the 5-volt versions. This current is less for the 3-volt versions. The worst case static current is 10 mA for all pASIC380 devices.

Active Power

Active power arises from the energy required to move charge in and out of the load capacitances on the CMOS gates. A simple model of this is shown in *Figure 1*. The capacitance is composed of the intrinsic capacitance of the gate, the interconnect wire capacitance to ground, and the input capacitance of the gates to which the driving gate is connected. For the purpose of the model, the capacitance is lumped into the one capacitor in *Figure 1*.

The calculation can be a consuming task. Each logic cell contains multiple gates each toggling at different average frequencies. Each logic cell can be connected to the inputs of other logic cells through various types and lengths of interconnect wires. With several thousand gates in the device, a power calculation based on the simple model is not a useful approach. A simplification is obtained by attributing an average capacitance to elements easily identifiable by the user.

These elements are:

- logic cell
- input buffer
- output buffer (unloaded externally)
- loads on high drive input buffers

- express interconnect wire
- clock input buffer
- clock distribution (internal column) buffer
- clock load

These elements are identified in *Figure 2,* which is an architectural representation of the pASIC family devices. Three of the elements in this list are explicitly identified load capacitances: loads on high drive input buffers, express interconnect wires, and clock loads. The average capacitances for each of these elements may not be directly due to a named element but will include interconnect wire capacitance and loads the element is connected to (given some average fanout). The capacitances for these elements will be referred to as an equivalent capacitance to reflect this averaging and the fact that the capacitance includes loads not necessarily in that particular element.

The equivalent capacitances are derived from empirical data to insure accuracy. Moreover, the measurements verify the averaging process and they verify the way the capacitances are attributed to the various elements. The equivalent capacitances for all the elements are given in *Table 1* for various average frequencies from 10 to 100 MHz. The equivalent capacitances are also plotted vs frequency in *Figure 3*. Given this data, the user only needs to know how many of each of these elements are used and their average frequency in order to estimate the power consumption. Not all elements are included in all members of the family. The individual datasheets should be consulted for further details.

With the capacitance in pF, the frequency in MHz, and the resulting power in mW, the power equation can be expressed as

$$P_{mW} = C_{EQ} V_{CC}^2 f 10^{-3}$$

This equation is in a form for practical use. The equivalent capacitance values, C_{EQ}, are obtained form the table or curves for the frequency of interest.

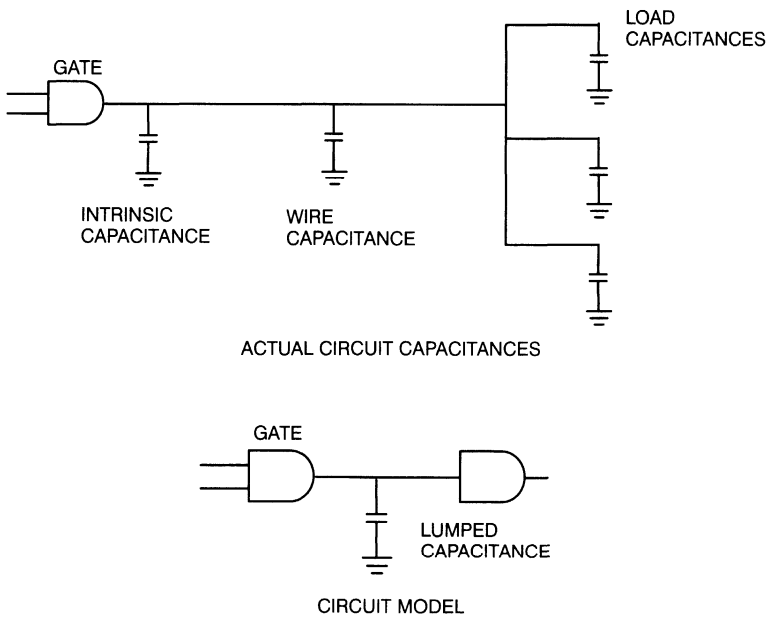


Figure 1. Capacitances in CMOS Circuits

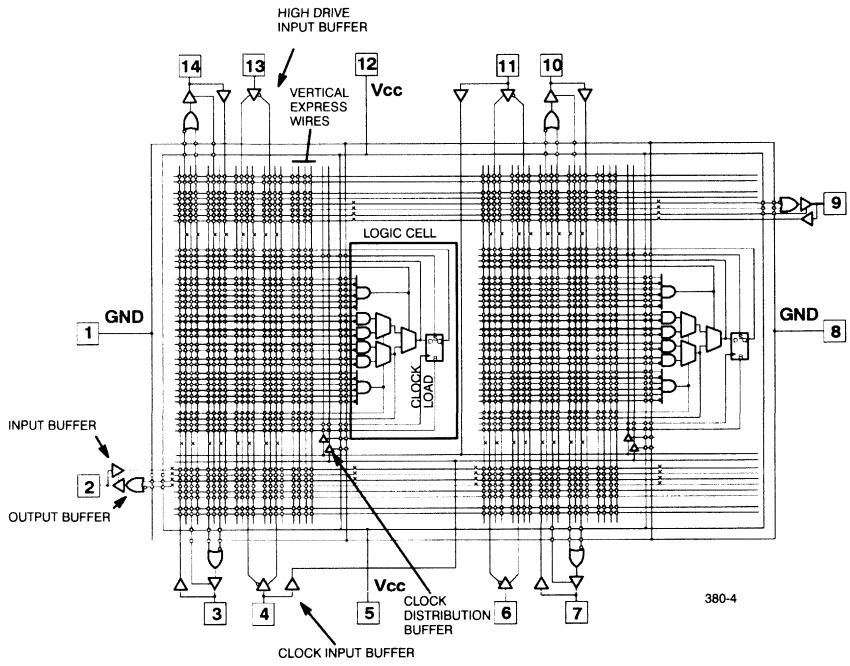


Figure 2. pASIC Internal Architecture

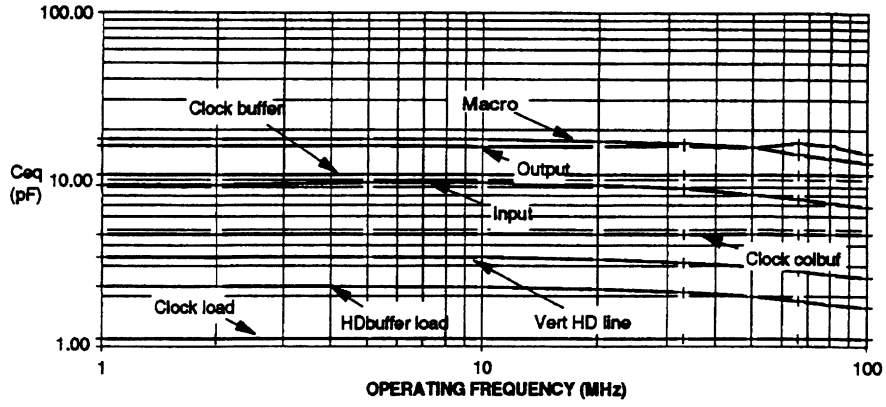


Figure 3. pASIC380 C_{EQ} vs. Operating Frequency

Table 1. pASIC380 Equivalent Capacitance (C_{EQ})

	10 MHz	20 MHz	33 MHz	50 MHz	66 MHz	80 MHz	100 MHz
Input	9.60	9.30	8.89	8.13	7.62	7.23	6.83
Output	15.73	15.83	16.04	15.55	16.60	16.04	14.39
Macro	17.47	17.02	16.57	15.78	14.15	13.42	12.69
HDbuffer Load	2.25	2.19	2.10	1.98	1.87	1.77	1.71
Vert HD Line	3.38	3.29	3.16	2.97	2.80	2.66	2.57
Clock Buffer	10.75	10.75	10.75	10.75	10.75	10.75	10.75
Clock Colbuf	4.67	4.67	4.67	4.67	4.67	4.67	4.67
Clock Load	1.11	1.11	1.11	1.11	1.11	1.11	1.11

Power Estimation Example

As an example of a power estimate, consider a 16-bit synchronous counter operating at 33 MHz. This example is for illustrative purposes only and the results should not be used for any other purposes. The counter clock is placed on a high-drive input-only pad (not one of the specialized clock input buffers) and is routed to the counter flip-flops through vertical express wires. When laid out, the counter occupies four columns in the array. All of the counter outputs are sent to output pins. Equivalent capacitance numbers are obtained from *Table 1* under the 33 MHz column.

First examine the 16 bit counter and the logic cells used to implement it. An analysis of this gives a simple result that can be used for the logic and output cell power calculation. The first flip-flop toggles at f/2, the next flip-flop toggles at f/4, the third at f/8, etc. The average per flip-flop toggle rate is

$(f/16)*(1/2 + 1/4 + 1/8 ... + 1/65536)$

or approximately f/16. The counter and the outputs can be considered as 16 logic cells and 16 outputs each toggling at f/16.

The power for all the elements can now be easily calculated.

Logic Cells (each cell)

$C_{EQ} = 16.57$ pF

f = 33/16 MHz

$P = 16.57\ (33/16) * 5^2 * 10^{-3} = 0.83$ mW

and for all 16

$P = 16 * 0.83 = 13.28$ mW

Input Buffer

This is a high drive input buffer for the clock.

The input buffer itself

$C_{EQ} = 8.89$ pF

f = 33 MHz

$P = 8.89\ (33) * 5^2 * 10^{-3} = 7.33$ mW

The vertical express wires (4)

$C_{EQ} = 3.16$ pF

f = 33 MHz

$P = 4 * 3.16\ (33) * 5^2 * 10^{-3} = 10.43$ mW

The high drive buffer loads (clocks on 16 flip–flops)

$C_{EQ} = 2.10$ pF

f = 33 MHz

$P = 16 * 2.10\ (33) * 5^2 * 10^{-3} = 27.72$ mW

The output buffers (total for all 16)

$C_{EQ} = 16.04$ pF

f = 33/16 MHz

$P = 16 * 16.04\ (33/16) * 5^2 * 10^{-3} = 13.23$ mW

Adding all of the contributors to the power, the total dynamic power for the counter is 72.51 mW. To this must be added the maximum quiescent power of 50

mW (10 mA max. specification) giving a total of 123 mW. This power calculation does not include the power resulting from external loads on the device pins.

Obtaining Values for the Calculations

The difficult part of the calculations is obtaining values for the number of logic cells used, the number of clock buffers used, and the average toggle frequency. There is no prescription for determining these numbers. However, there are aids to this process. These aids will be discussed in this section.

Consider a 16-bit counter different from the one in the previous example. This new counter will use the internal clock distribution tree. The task of obtaining the number of logic cells and clock buffers used is aided by the Physical View in the *Warp3™* tool. *Figure 4* shows the physical view for a 16-bit synchronous counter using the internal clock distribution tree. The number of logic cells used in the counter can be easily counted; there are 27. With the physical view displayed in SpDE, the user can obtain a summary of the cell utilization. This is done by selecting Cell Utilization under Info. There are 16 output buffers and one clock input buffer, as expected. The upper/lower column division is between row 5 and row 6. Therefore, the clock is distributed to both the upper and lower half of columns A and B, whereas only the lower half of columns C, D, E, and H receive clocks. Columns A and B will use two clock internal buffers each (one for the lower half column and one for the upper half column) and there will be one each for columns C, D, E, and H. The results for clock distribution are:

clock input buffer (clock buffer)	1
clock internal buffers (clock colbuf)	8
clock loads	16

All of the components of the active power have been identified. From the previous example, the average frequency for the flip-flop logic cells, the output buffers, and the clock related buffers and loads is known. Eleven of the logic cells are combinatorial and need to be examined more closely. These logic cells must be part of the excitation logic for the counter flip-flops. There are several approaches. The most direct approach is to examine the physical view and, for each cell in question, examine the origin of the inputs and the destination of the output and determine heuristically the approximate logic function being implemented in the cell. Knowing this, the average toggle rate can be estimated. This approach can be time consuming and difficult if there is a large amount of circuitry in the design. An alternative is to use approximations to an advantage. An approach used earlier was to attribute an average toggle frequency to each flip-flop of the counter. A simple extension of this approximation suggests that each of these combinatorial cells be estimated as having an average toggle frequency of f/16.

Using the above data, the power for this 16-bit counter is determined as follows:

Logic Cells (each cell)

C_{EQ} = 16.57 pF

f = 33/16 MHz

$P = 16.57\ (33/16) * 5^2 * 10^{-3} = 0.85$ mW

and for all 27

$P = 27 * 0.85 = 22.95$ mW

Clock Input Buffer and Distribution Tree

The input buffer itself

C_{EQ} = 10.75 pF

f = 33 MHz

$P = 10.75\ (33) * 5^2 * 10^{-3} = 8.87$ mW

The clock column buffers (8)

C_{EQ} = 4.67 pF

f = 33 MHz

$P = 8 * 4.67\ (33) * 5^2 * 10^{-3} = 30.82$ mW

The loads (16)

C_{EQ} = 1.11 pF

f = 33 MHz

$P = 16 * 1.11\ (33) * 5^2 * 10^{-3} = 14.65$ mW

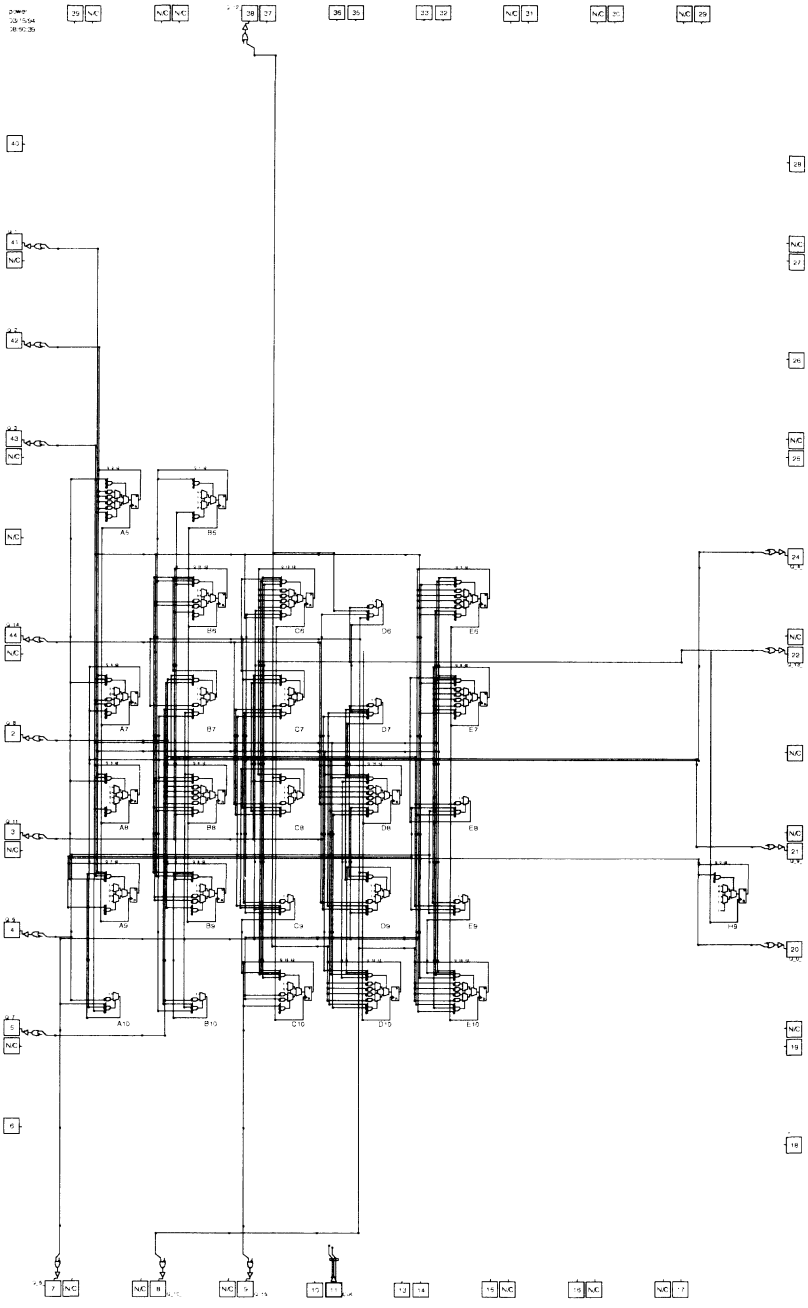


Figure 4. 16-Bit Counter Physical View

The output buffers (total for all 16)

C_{EQ} = 16.04 pF

f = 33/16 MHz

$P = 16 * 16.04 (33/16) * 5^2 * 10^{-3} = 13.23$ mW

The total dynamic power for the counter is 90.52 mW. Adding, as before, the maximum quiescent power of 50 mw, the total power becomes 140 mW. This power calculation does not include the power resulting from external loads on the device pins.

Conclusion

This application note provides algorithms and reference data for calculating power consumption in Cypress programmable logic devices. All calculations for active power are based on *Equation 4*. The accuracy of the results is related to the determination of the capacitance and the frequency. In many cases, significant power dissipation is a result of driving external loads. Users should make certain that the device power calculations include the power associated with the external loads.

Quality, Reliability, and Process Flows

Corporate Views on Quality and Reliability

Cypress believes in product excellence. Excellence can only be defined by how the users perceive both our product quality and reliability. If you, the user, are not satisfied with every device that is shipped, then product excellence has not been achieved.

Product excellence does not occur by following the industry norms. It begins by being better than one's competitors, with better designs, processes, controls and materials. Therefore, product quality and reliability are built into every Cypress product from the start.

Some of the techniques used to insure product excellence are the following:

- Product Reliability is built into every product design, starting from the initial design conception.
- Product Quality is built into every step of the manufacturing process through stringent inspections of incoming materials and conformance checks after critical process steps.
- Stringent inspections and reliability conformance checks are done on finished product to insure the finished product quality requirements are met.
- Field data test results are encouraged and tracked so that accelerated testing can be correlated to actual use experiences.

Product Assurance Documents

Cypress Semiconductor uses MIL-STD-883D and MIL-I-38535B as baseline documents to determine our Test Methods, Procedures and General Specifications for semiconductors.

Customers using our commercial and industrial grade product receive the benefit of a military patterned process flow at no additional charge.

Product Testing Categories

Five different testing categories are offered by Cypress:

1. Commercial operating range product: 0°C to +70°C.
2. Industrial operating range product: − 40°C to +85°C.
3. Military Grade product processed to MIL-STD-883D; Military operating range: − 55°C to +125°C.
4. SMD (Standardized Military Drawing) approved product: Military operating range: − 55°C to +125°C, electrically tested per the applicable Military Drawing.
5. JAN qualified product; Military operating range: − 55°C to +125°C, electrically tested per JAN slash sheet requirements.

Categories 1, 2, and 3 are available on all products offered by Cypress Semiconductor. Categories 4 and 5 are offered on a more limited basis, dependent upon the specific part type in question.

Commercial Product Assurance Categories

Commercial grade devices are offered with two different classes of product assurance. Every device shipped, as a minimum, meets the processing and screening requirements of level 1.

Level 1: For commercial or industrial systems where the demand for quality and reliability is high, but where field service and device replacement can be reasonably accomplished.

Level 2: For enhanced reliability applications and commercial or industrial systems where maintenance is difficult and/or expensive and reliability is paramount.

Devices are upgraded from Level 1 to Level 2 by additional testing and a burn-in of 12 hours at 150°C.

Tables 1 and *2* list the 100% screening and quality conformance testing performed by Cypress Semiconductor in order to meet requirements of these programs.

Military Product Assurance Categories

Cypress's Military Grade components and SMD products are processed per MIL-STD-883D using methods 5004 and 5005 to define our screening and quality conformance procedures. The processing performed by Cypress results in a product that meets the class B screening requirements as called out by these methods. Every device shipped, as a minimum, meets these requirements.

JAN, SMD, and Military Grade devices supplied by Cypress are processed for applications where maintenance is difficult or expensive and reliability is paramount. *Tables 3* through *7* list the screening and quality conformance testing that is performed in order to meet the processing requirements required by MIL-STD-883D and MIL-I-38535B.

Table 1. Cypress Commercial and Industrial Product Screening Flows—Components

Screen	MIL-STD-883D Method	Product Temperature Ranges			
		Commercial 0°C to +70°C; Industrial −40°C to +85°C			
		Level 1		Level 2	
		Plastic	Hermetic	Plastic	Hermetic
Visual/Mechanical					
• Internal Visual	2010	0.4% AQL	100%	0.4% AQL	100%
• Hermeticity					
– Fine Leak	1014, Cond A or B (sample)	Does Not Apply	LTPD = 5	Does Not Apply	LTPD = 5
– Gross Leak	1014, Cond C	Does Not Apply	100%	Does Not Apply	100%
Burn-in					
• Pre-Burn-in Electrical	Per Device Specification	Does Not Apply	Does Not Apply	100%	100%
• Burn-in	Per Cypress Specification	Does Not Apply	Does Not Apply	100%[1]	100%[1]
• Post-Burn-in Electrical	Per Device Specification	Does Not Apply	Does Not Apply	100%	100%
• Percent Defective Allowable (PDA)		Does Not Apply	Does Not Apply	5% (max)[2]	5% (max)[2]
Final Electrical	Per Device Specification				
• Static (DC), Functional, and Switching (AC) Tests	1. At 25°C and Power Supplies Extremes	Not Performed	Not Performed	100%[1]	100%[1]
	2. At Hot Temperature and Power Supply Extremes	100%	100%	100%	100%
Cypress Quality Lot Acceptance					
• External Visual	2009	Note 3	Note 3	Note 3	Note 3
• Final Electrical Conformance	Cypress Method 17-00064	Note 3	Note 3	Note 3	Note 3

Table 2. Cypress Commercial and Industrial Product Screening Flows—Modules

Screen	MIL-STD-883D Method	Product Temperature Ranges	
		Commercial 0°C to +70°C; Industrial −40°C to +85°C	
		Level 1	Level 2
Burn-in			
• Pre-Burn-in Electrical	Per Device Specification	Does Not Apply	100%
• Burn-in	1015	Does Not Apply	100%
• Post-Burn-in Electrical	Per Device Specification	Does Not Apply	100%
• Percent Defective Allowable (PDA)		Does Not Apply	15%
Final Electrical	Per Device Specification		
• Static (DC), Functional, and Switching (AC) Tests	1. At 25°C and Power Supply Extremes	Not Performed	100%
	2. At Hot Temperature and Power Supply Extremes	100%	100%
Cypress Quality Lot Acceptance			
• External Visual	2009	Per Cypress Module Specification	Per Cypress Module Specification
• Final Electrical Conformance	Cypress Method 17-00064	Note 3	Note 3

Notes:
1. Burn-in is performed as a standard for 12 hours at 150°C.
2. Electrical Test is performed after burn-in. Results of this are used to determine PDA percentage.
3. Lot acceptance testing is performed on every lot to guarantee 200 PPM average outgoing quality.

6

Table 3. Cypress JAN/SMD/Military Grade Product Screening Flows for Class B

Screen	Screening Per Method 5004 of MIL-STD-883D	Product Temperature Ranges −55°C to +125°C		
		JAN	SMD/Military Grade Product	Military Grade Module
Visual/Mechanical				
• Internal Visual	Method 2010, Cond B	100%	100%	N/A
• Temperature Cycling	Method 1010, Cond C, (10 cycles)	100%	100%	Optional
• Constant Acceleration	Method 2001, Cond E (Min.), Y1 Orientation Only	100%	100%	N/A
• Hermeticity:				
— Fine Leak	Method 1014, Cond A or B	100%	100%	N/A
— Gross Leak	Method 1014, Cond C	100%	100%	N/A
Burn-in				
• Pre-Burn-in Electrical Parameters	Per Applicable Device Specification	100%	100%	100%
• Burn-in Test	Method 1015, Cond D, 160 Hrs at 125°C Min. or 80 Hrs at 150°C	100%	100%	100% (48 Hours at 125°C)
• Post-Burn-in Electrical Parameters	Per Applicable Device Specification	100%	100%	100%
• Percent Defective Allowable (PDA)	Maximum PDA, for All Lots	5%	5%	10%
Final Electrical Tests				
• Static Tests	Method 5005 Subgroups 1, 2, and 3	100% Test to Slash Sheet	100% Test to Applicable Device Specification	100% Test to Applicable Specification
• Functional Tests	Method 5005 Subgroups 7, 8A, and 8B	100% Test to Slash Sheet	100% Test to Applicable Device Specification	100% Test to Applicable Specification
• Switching	Method 5005 Subgroups 9, 10, and 11	100% Test to Slash Sheet	100% Test to Applicable Device Specification	100% Test to Applicable Specification
Quality Conformance Tests				
• Group A[4]	Method 5005, see Tables 4 – 7 for details	Sample	Sample	Sample
• Group B		Sample	Sample	Sample
• Group C[5]		Sample	Sample	Sample
• Group D[5]		Sample	Sample	Sample
External Visual	Method 2009	100%	100%	100%

Notes:

4. Group A subgroups tested for SMD/Military Grade products are 1, 2, 3, 7, 8A, 8B, 9, 10, 11, or per JAN Slash Sheet.
5. Group C and D end-point electrical tests for SMD/Military Grade products are performed to Group A subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11, or per JAN Slash Sheet.

Table 4. Group A Test Descriptions

Sub-group	Description	Sample Size/Accept No.	
		Components	Modules[6]
1	Static Tests at 25°C	116/0	116/0
2	Static Tests at Maximum Rated Operating Temperature	116/0	116/0
3	Static Tests at Minimum Rated Operating Temperature	116/0	116/0
4	Dynamic Tests at 25°C	116/0	116/0
5	Dynamic Tests at Maximum Rated Operating Temperature	116/0	116/0
6	Dynamic Tests at Minimum Rated Operating Temperature	116/0	116/0
7	Functional Tests at 25°C	116/0	116/0
8A	Functional Tests at Maximum Temperature	116/0	116/0
8B	Functional Tests at Minimum Temperature	116/0	116/0
9	Switching Tests at 25°C	116/0	116/0
10	Switching Tests at Maximum Temperature	116/0	116/0
11	Switching Tests at Minimum Temperature	116/0	116/0

Cypress uses an LTPD sampling plan that was developed by the Military to assure product quality. Testing is performed to the subgroups found to be appropriate for the particular device type. All Military Grade component products have a Group A sample test performed on each inspection lot per MIL-STD-883D and the applicable device specification.

Table 5. Group B Quality Tests

Sub-group	Description	Quantity/Accept # or LTPD	
		Components	Modules[6]
2	Resistance to Solvents, Method 2015	3/0	3/0
3	Solderability, Method 2003	10	10
5	Bond Strength, Method 2011	15	NA

Group B testing is performed for each inspection lot. An inspection lot is defined as a group of material of the same device type, package type and lead finish built within a six week seal period and submitted to Group B testing at the same time.

Note:
6. Military Grade Modules are processed to proposed JEDEC standard flows for MIL-STD-883D compliant modules.

Table 6. Group C Quality Tests

Sub-group	Description	LTPD	
		Components	Modules[6]
1	Steady State Life Test, End-Point Electricals, Method 1005, Cond D	5	15/0

Group C tests for JAN product are performed on one device type from one inspection for lot representing each technology. Sample tests are performed per MIL-I-38535B from each three month production of devices, which is based upon the die fabrication date code.

Group C tests for SMD and Military Grade products are performed on one device type from one inspection lot representing each technology. Sample tests are performed per MIL-STD-883D from each four calendar quarters production of devices, which is based upon the die fabrication date code.

End-point electrical tests and parameters are performed per the applicable device specification.

Table 7. Group D Quality Tests (Package Related)

Sub-group	Description	Quantity/Accept # or LTPD	
		Components	Modules[7]
1	Physical Dimensions, Method 2016	15	15/0
2	Lead Integrity, Seal: Fine and Gross Leak, Method 2004 and 1014	5	15/0
3	Thermal Shock, Temp Cycling, Moisture Resistance, Seal: Fine and Gross Leak, Visual Examination, End-Point, Electricals, Methods 1011, 1010, 1004 and 1014	15	15/0
4	Mechanical Shock, Vibration - Variable Frequency, Constant Acceleration, Seal: Fine and Gross Leak, Visual Examination, End-Point Electricals, Methods 2002, 2007, 2001 and 1014	15	15/0

Table 7. Group D Quality Tests (Package Related) (continued)

Sub-group	Description	Quantity/Accept # or LTPD	
		Components	Modules[7]
5	Salt Atmosphere, Seal: Fine & Gross Leak, Visual Examination, Methods 1009 & 1014	15 (0)	15/0
6	Internal Water-Vapor Content; 5000 ppm maximum @ 100°C. Method 1018	3(0) or 5(1)	N/A
7	Adhesion of Lead Finish,[8] Method 2025	15(0)	15/0
8	Lid Torque, Method 2024[9]	5(0)	N/A

Notes:
7. Does not apply to leadless chip carriers.
8. Based on the number of leads.
9. Applies only to packages with glass seals.

Group D tests for JAN product are performed per MIL-I-38535B on each package type from each six months of production, based on the lot inspection identification (or date) codes.

Group D tests for SMD and Military Grade products are performed per MIL-STD-883D on each package type from each six months of production, based on the lot inspection identification (or date) codes.

End-point electrical tests and parameters are performed per the applicable device specification.

Product Screening Summary

Commercial and Industrial Product

- Screened to either Level 1 or Level 2 product assurance flows
- Hermetic and molded packages available
- Incoming mechanical and electrical performance guaranteed:
  - 0.02% AQL Electrical Sample test performed on every lot prior to shipment
  - 0.65% AQL External Visual Sample inspection
- Electrically tested to Cypress data sheet

Ordering Information

Product Assurance Grade: Level 1

- Order Standard Cypress part number
- Parts marked the same as ordered part number
  Ex: CY7C122-15PC, PALC22V10-25PI

Product Assurance Grade: Level 2

- Burn-in performed on all devices to Cypress detailed circuit specification
- Add 'B' Suffix to Cypress standard part number when ordering to designate burn-in option
- Parts marked the same as ordered part number
  Ex: CY7C122-15PCB, PALC22V10-25PIB

Military Grade Product

- SMD and Military Grade components are manufactured in compliance with paragraph 1.2.1 of MIL-STD-883D. Compliant products are identified by an 'MB' suffix on the part number (CY7C122-25DMB) and the letter "C"
- JAN devices are manufactured in accordance with MIL-M-38510J
- Military grade devices electrically tested to:
  - Cypress data sheet specifications

    OR
  - SMD devices electrically tested to military drawing specifications

    OR
  - JAN devices electrically tested to slash sheet specifications
- All devices supplied in hermetic packages
- Quality conformance inspection: Method 5005, Groups A, B, C, and D performed as part of the standard process flow
- Burn-in performed on all devices
  - Cypress detailed circuit specification for non-Jan devices

    OR
  - Slash sheet requirements for JAN products
- Static functional and switching tests performed at 25°C as well as temperature and power supply extremes on 100% of the product in every lot
- JAN product manufactured in a DESC certified facility

Ordering Information

JAN Product:

- Order per military document
- Marked per military document
  Ex: JM38510/28901BVA

SMD Product:

- Order per military document
- Marked per military document
  Ex: 5962-8867001LA

Military Grade Product:

  - Order per Cypress standard military part number
  - Marked the same as ordered part number
    Ex: CY7C122-25DMB

Military Modules

- Military Temperature Grade Modules are designated with an 'M' suffix only. These modules are screened to standard combined flows and tested at both military temperature extremes.
- MIL-STD-883D Equivalent Modules are processed to proposed JEDEC standard flows for MIL-STD-883D compliant modules. All MIL-STD-883D equivalent modules are assembled with fully compliant MIL-STD-883D components.

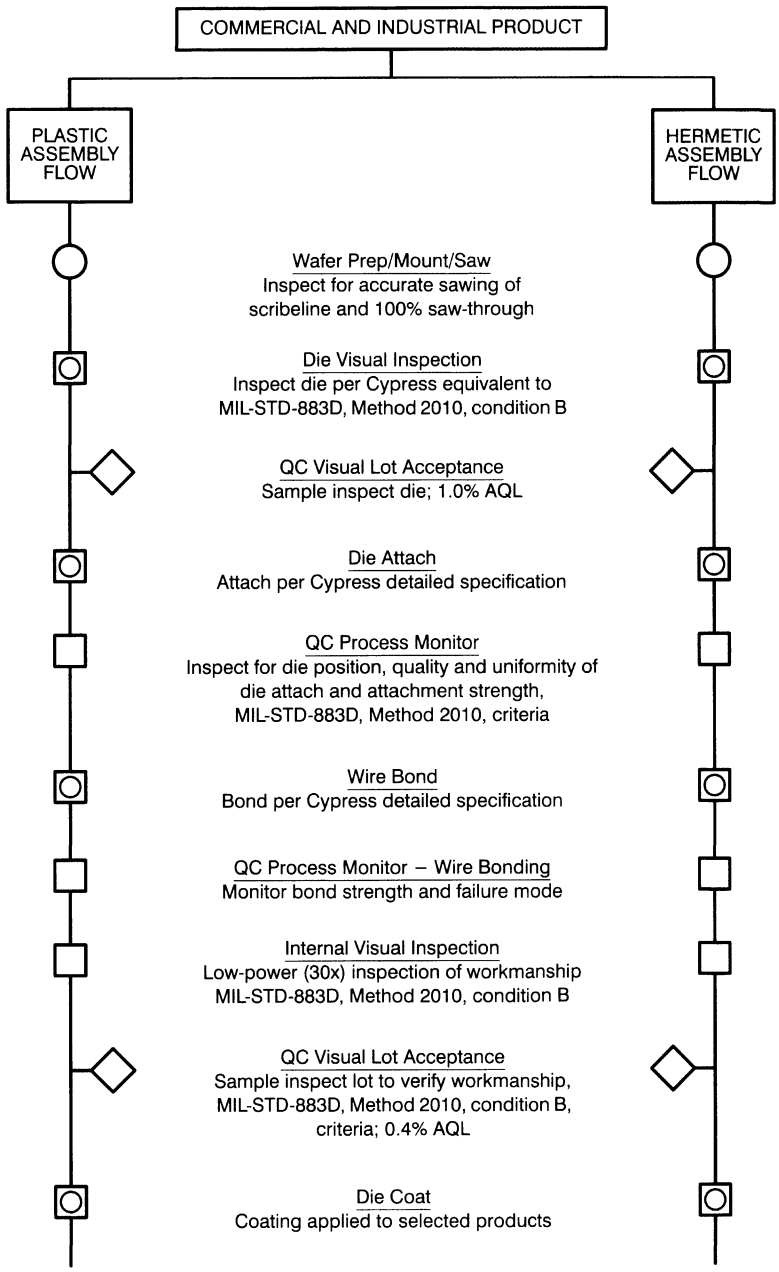
Product Quality Assurance Flow—Components

Area	PROCESS	Process Details
QC	INCOMING MATERIALS INSPECTION	All incoming materials are inspected to documented procedures covering the handling, inspection, storage, and release of raw materials used in the manufacture of Cypress products. Materials inspected are: wafers, masks, leadframes, ceramic packages and/or piece parts, molding compounds, gases, chemicals, etc.
FAB	DIFFUSION/ION IMPLANTATION	Sheet resistance, implant dose, species and CV characteristics are measured for all critical implants on every product run. Test wafers may be used to collect this data instead of actual production wafers. If this is done, they are processed with the standard product prior to collecting specific data. This insures accurate correlation between the actual product and the wafers used to monitor implantation.
FAB	OXIDATION	Sample wafers and sample sites are inspected on each run from various positions of the furnace load to inspect for oxide thickness. Automated equipment is used to monitor pinhole counts for various oxidations in the process. In addition, an appearance inspection is performed by the opeartor to further monitor the oxidation process.
FAB	PHOTOLITHOGRAPHY /ETCHING	Appearance of resist is checked by the operator after the spin operation. Also, after the film is developed, both dimensions and appearance are checked by the operator on a sample of wafers and locations upon each wafer. Final CDs and alignment are also sample inspected on several wafers and sites on each wafer on every product run.
FAB	METALIZATION	Film thickness is monitored on every run. Step coverage cross-sections are performed on a periodic basis to insure coverage.
FAB	PASSIVATION	An outgoing visual inspection is performed on 100% of the wafers in a lot to inspect for scratches, particles, bubbles, etc. Film thickness is verified on a sample of wafers and locations within each given wafer on each run. Pinholes are monitored on a sample basis weekly.
FAB	QC VISUAL OF WAFERS	
FAB	E-TEST	Electrical test is performed for final process electrical characteristics on every wafer.
FAB	QC MONITOR OF E-TEST DATA	Weekly review of all data trends; running averages, minimums, maximums, etc. are reviewed with the process control manager.
TEST	WAFER PROBE/SORT	Verify functionality, electrical characteristics, stress test devices.
TEST	QC CHECK PROBING AND ELECTRICAL TEST RESULTS	Pass/fail lot based on yield and correct probe placement.

TO ASSEMBLY AND TEST

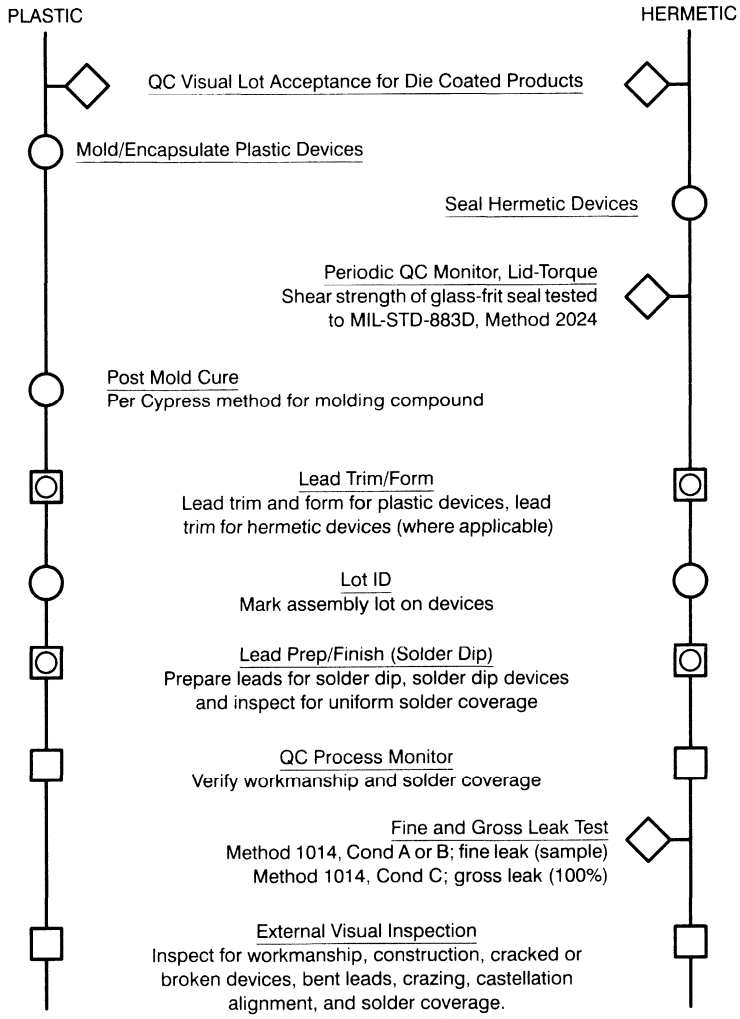
(continued)

Product Quality Assurance Flow—Components (continued)
Commercial and Industrial Product



(continued)

Product Quality Assurance Flow—Components (continued)
Commercial and Industrial Product



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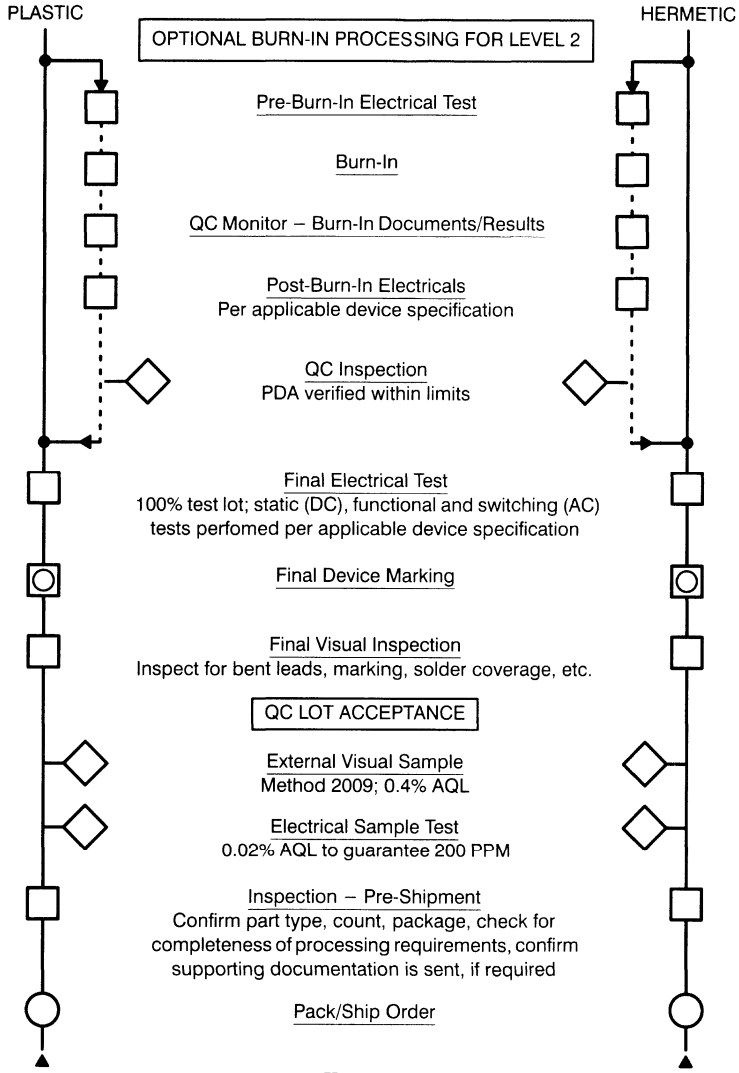
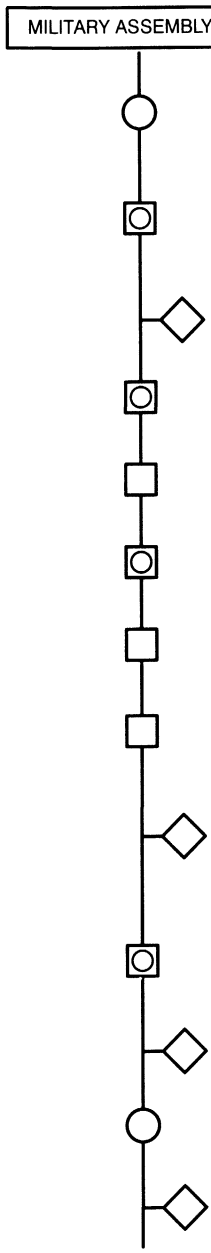
Product Quality Assurance Flow—Components (continued)
Commercial and Industrial Product



Key

- Production Process
- Test/Inspection
- Production Process and Test Inspection
- QC Sample Gate and Inspection

Product Quality Assurance Flow—Components
Military Components



Wafer Prep/Mount/Saw
Inspect for accurate sawing of scribeline and 100% saw-through

Die Visual Inspection
Inspect die per MIL-STD-883D, Method 2010, condition B

QC Visual Lot Acceptance
Sample inspect die; 1.0% AQL

Die Attach
Attach per Cypress detailed specification

Die Adherence Monitor
MIL-STD-883D, Method 2019 or Method 2027

Wire Bond
Bond per Cypress detailed specification

Bond Pull Monitor
MIL-STD-883D, Method 2011

Internal Visual Inspection
Low-power and high-power inspection per MIL-STD-883D, Method 2010, condition B

QC Visual Lot Acceptance
Sample inspect lot per MIL-STD-883D, Method 2010, condition B, 0.4% AQL

Die Coat
Coating applied to selected products

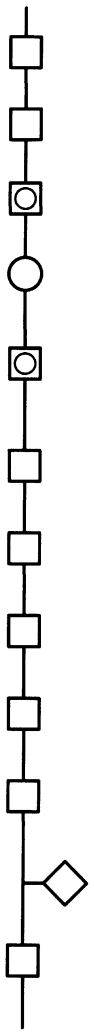
QC Visual Lot Acceptance for Die Coated Products

Seal

Periodic QC Monitor, Lid-Torque
Shear strength of glass

(continued)

Product Quality Assurance Flow—Components (continued)
Military Components



Temperature Cycle
Method 1010, Cond C, 10 cycles

Constant Acceleration
Method 2001, Cond E, Y1 Orientation

Lead Trim
Lead trim when applicable

Lot ID
Mark assembly lot on devices

Lead Finish
Solder dip or matte tin plate applicable devices and inspect

QC Process Monitor
Verify workmanship and lead finish coverage

External Visual Inspection
Method 2009

Pre-Burn-In Electrical Test
Method 5004, per applicable device specification

Burn-In
Method 1015, condition D

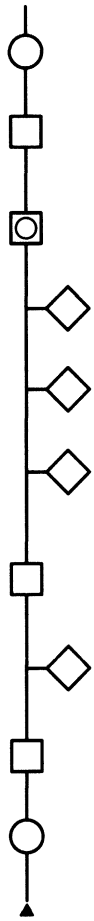
Post-Burn-In Electricals
Method 5004, per applicable device specification

PDA Calculation
Method 5004, 5%

Final Electrical Test
Method 5004; Static, functional and switching tests per applicable device specification

(continued)

Product Quality Assurance Flow—Components (continued)
Military Components



Lead Finish – Solder Dip
Solder dip applicable devices

Fine and Gross Leak Test
Method 1014, condition A or B, fine leak; condition C, gross leak

Final Device Marking
MIL-STD-883D or applicable device specification

Group B
Method 5005

Group A
Method 5005, per applicable device specification

Group C and D
Method 5005, in accordance with
1.2.1 of MIL-STD-883D; JAN devices
in accordance with MIL-M-38510J

External Visual
Method 2009, 100% inspection

External Visual Sample
Method 2009, 0.4% AQL

Plant Clearance

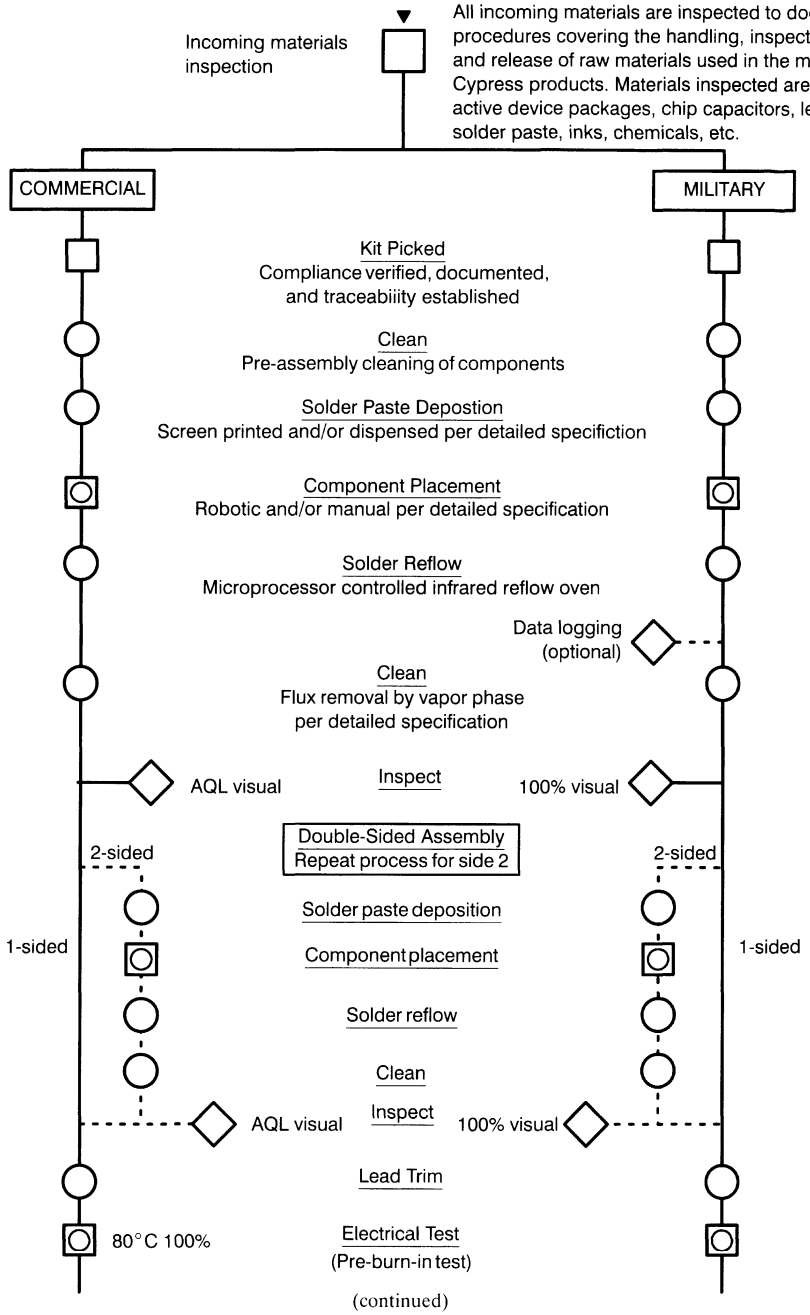
Pack/Ship Order

Key

- Production Process
- Test/Inspection
- Production Process and Test Inspection
- QC Sample Gate and Inspection

6

Product Quality Assurance Flow—Modules



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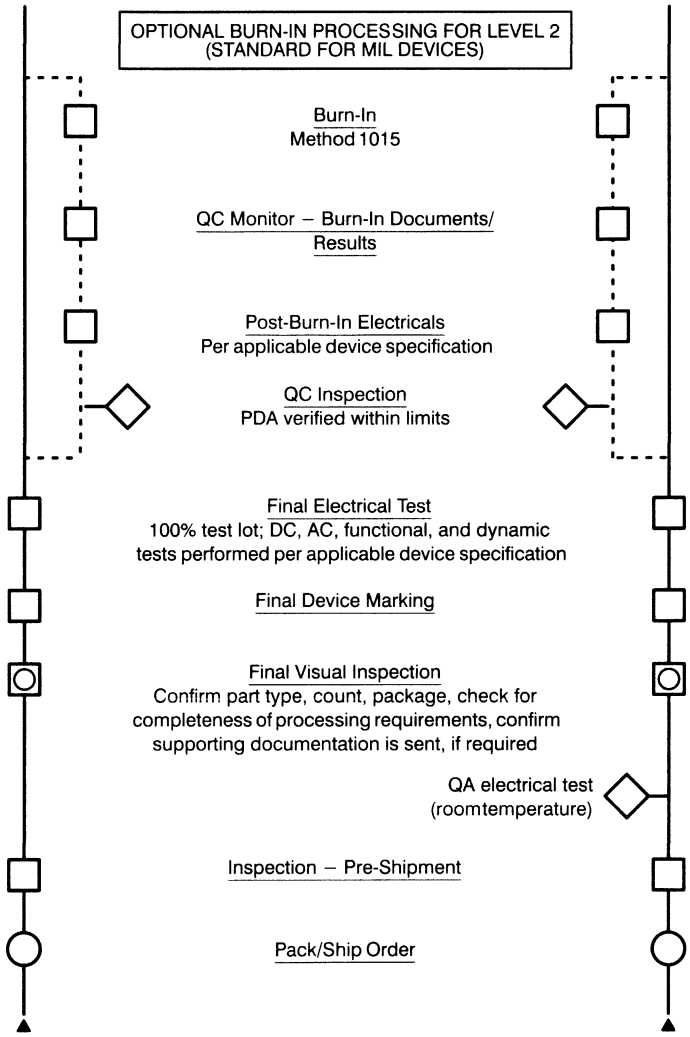
Product Quality Assurance Flow—Modules (continued)



Key

- Production Process
- Test/Inspection
- Production Process and Test Inspection
- QC Sample gate and inspection

6

Reliability Monitor Program

The Reliability Monitor Program is a documented Cypress procedure that is described in Cypress specification #25-00008, which is available to Cypress customers upon request. This specification describes a procedure that provides for periodic reliability monitors to insure that all Cypress products comply with established goals for reliability improvement and to minimize reliability risks for Cypress customers. The Reliability Monitor Program monitors our most advanced technologies and packages. Every technology produced at a given fabrication site (Tech. – Fab.) and all assembly houses are monitored at least quarterly. If failures occur, detailed failure analyses are performed and corrective actions are implemented. A summary of the Reliability Monitor Program test and sampling plan is shown below.

Quarterly Reliability Monitor Test Matrix

Stress	Devices Tested	# per Quarter
HTOL	Tech. – Fab.	6
	All High Volume	2
HAST	Tech. – Fab.	6
	All High Volume	2
PCT	Plastic Packages	4
TC	Tech. – Fab.	6
	Plastic Packages	3
	Ceramic Packages	5
	All High Volume	2
DRET	FAMOS – San Jose and Texas	2
HTSSL	All Technologies	4
TEV	All Technologies	4
Total		46

Reliability Monitor Test Conditions

Test	Abbrev.	Temp. (°C)	R.H. (%)	Bias	Sample Size	LTPD	Read Points (hrs.)
High-Temperature Operating Life	HTOL	+150	N/A	5.75V Dynamic	116	2	48, 168, 500, 1000
High-Temperature Steady-State Life	HTSSL	+150	N/A	5.75V Static	116	2	48, 168, 500, 1000
Data Retention for Plastic Packages	DRET	+165	N/A	N/A	76	3	168, 1000
Data Retention for Ceramic Packages	DRET2	+250	N/A	N/A	76	3	168, 1000
Pressure Cooker	PCT	+121	100	N/A	76	3	96, 168
Highly Accelerated Stress Test	HAST	+140	85	5.5V Static	76	3	128
Temperature Cycling for Plastic Packages	TC	−40 to +125°C	N/A	N/A	76	3	500, 1000 Cycles
Temperature Cycling for Ceramic Packages	TC2	−65 to +150°C	N/A	N/A	45	5	500, 1000 Cycles
Temperature Extreme Verification	TEV	Commercial Hot & Cold 0 to +70°C	N/A	N/A	116	2	N/A

Tape and Reel Specifications

Description

Surface-mounted devices are packaged in embossed tape and wound onto reels for shipment in compliance with Electronics Industries Association Standard EIA–481 Rev. A.

Specifications

Cover Tape

- The cover tape may not extend past the edge of the carrier tapes
- The cover tape shall not cover any part of any sprocket hole.
- The seal of the cover tape to the carrier tape is uniform, with the seal extending over 100% of the length of each pocket, on each side.
- The force to peel back the cover tape from the carrier tape shall be: 20 gms minimal, 70 gms nominal, 100 gms maximal, at a pull-back speed of 300 ± 10 mm/min.

Loading the Reel

Empty pockets between the first and last filled pockets on the tape are permitted within the following requirements:

- No two consecutive pockets may be left empty
- No more than a total of ten (10) empty pockets may be on a reel

The surface-mount devices are placed in the carrier tape with the leads down, as shown in *Figure 1*.

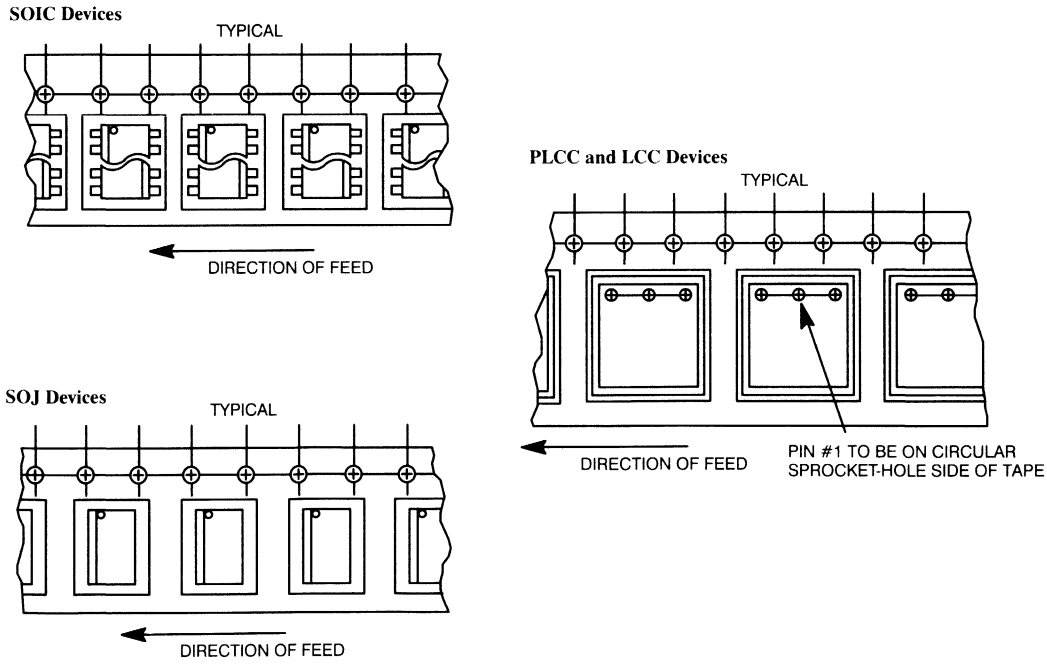


Figure 1. Part Orientation in Carrier Tape

Leaders and Trailers

The carrier tape and the cover tape may not be spliced. Both tapes must be one single uninterrupted piece from end to end.

Both ends of the tape must have empty pockets meeting the following minimum requirements:

- Trailer end (inside hub of reel) is 300 mm minimum
- Leader end (outside of reel) is 500 mm min., 560 mm max.
- Unfilled leader and trailer pockets are sealed
- Leaders and trailers are taped to tape and hub respectively using masking tape

Packaging

- Full reels contain a standard number of units (refer to *Table 1*)
- Reels may contain up to 3 inspection lots.
- Each reel is packed in an anti-static bag and then in its own individual box.
- Labels are placed on each reel as shown in *Figure 2*. The information on the label consists of a minimum of the following information, which complies with EIA 556, "Shipping and Receiving Transaction Bar Code Label Standard":
  - Barcoded Information:
    Customer PO number
    Quantity
    Date code
  - Human Readable Only:
    Package count (number of reels per order)
    Description
    "Cypress–San Jose"
    Cypress p/n
    Cypress CS number (if applicable)
    Customer p/n
- Each box will contain an identical label plus an ESD warning label.

Ordering Information

CY7Cxxx–yyzzz

xxx = part type

yy = speed

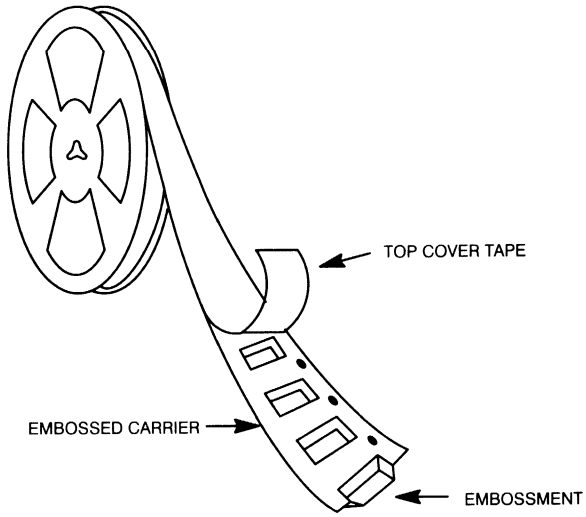
zzz = package, temperature, and options

SCT = soic, commercial temperature range
SIT = soic, inductrial temperature range
SCR = soic, commercial temperature plus burn-in
SIR = soic, industrial temperature plus burn-in
VCT = soj, commercial temperature range
VIT = soj, industrial temperature range
VCR = soj, commercial temperature plus burn-in
VIR = soj, industrial temperature plus burn-in
JCT = plcc, commercial temperature range
JIT = plcc, industrial temperature range
JCR = plcc, commercial temperature range plus burn-in
JIR = plcc, industrial temperature range plus burn-in

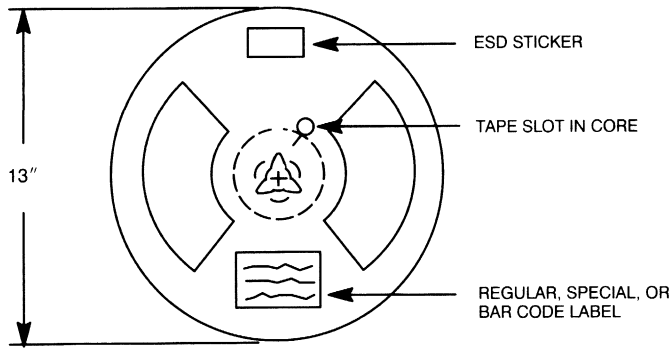
Notes:
1. The T or R suffix will not be marked on the device. Units will be marked the same as parts in a tube.
2. Order releases must be in full-reel multiples as listed in *Table 1*.

Table 1. Parts Per Reel and Tape Specifications

Package Type	Terminals	Carrier Width (mm)	Pocket Pitch	Parts Per Meter	Parts Per Full Reel
PLCC	18	24	3	83.3	750
	20	16	3	83.3	750
	28(S)	24	4	62.5	500
	32	24	4	62.5	500
	44	32	6	41.6	400
	52	32	6	41.6	400
	68	44	8	31.2	250
	84	44	8	31.2	250
SOIC	20	24	3	83.3	1,000
	24	24	3	83.3	1,000
	28	24	3	83.3	1,000
SOJ	20	24	3	83.3	1,000
	24	24	3	83.3	1,000
	28	24	3	83.3	1,000
TSOP–1	32	24	3	62.5	1,500



Tape and Reel Shipping Medium



Label Placement

Figure 2. Shipping Medium and Label Placement

Package Diagrams 7

Section Contents

Packages **Page Number**

Sales Representatives and Distributors

Thermal Management and Component Reliability

One of the key variables determining the long-term reliability of an integrated circuit is the junction temperature of the device during operation. Long-term reliability of the semiconductor chip degrades proportionally with increasing temperatures following an exponential function described by the Arrhenius equation of the kinetics of chemical reactions. The slope of the logarithmic plots is given by the activation energy of the failure mechanisms causing thermally activated wear out of the device (see *Figure 1*).

Typical activation energies for commonly observed failure mechanisms in CMOS devices are shown in *Table 1*.

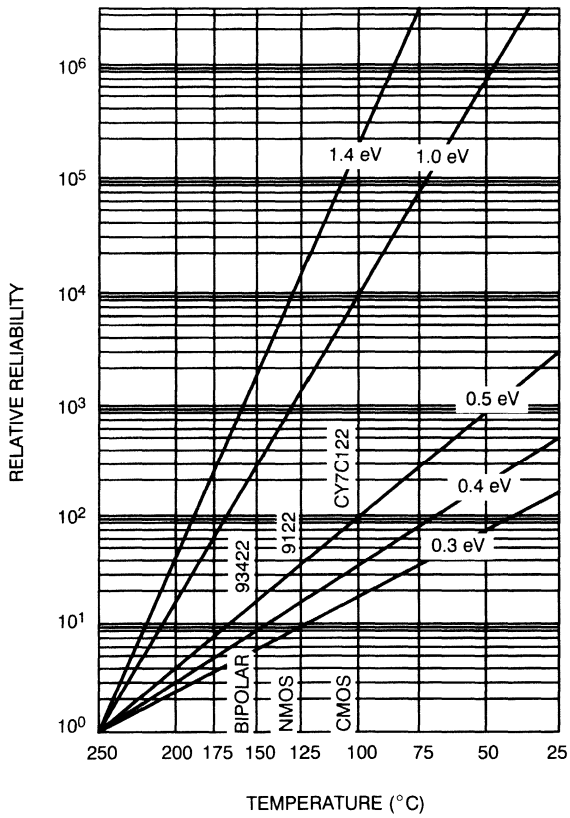


Figure 1. Arrhenius plot, which assumes a failure rate proportional to EXP ($-E_A/kT$) where E_A is the activation energy for the particular failure mechanism

Table 1. Failure Mechanisms and Activation Energies in CMOS Devices

Failure Mode	Approximate Activation Energy (Eq)
Oxide Defects	0.3 eV
Silicon Defects	0.3 eV
Electromigration	0.6 eV
Contact Metallurgy	0.9 eV
Surface Charge	0.5–1.0 eV
Slow Trapping	1.0 eV
Plastic Chemistry	1.0 eV
Polarization	1.0 eV
Microcracks	1.3 eV
Contamination	1.4 eV

To reduce thermally activated reliability failures, Cypress Semiconductor has optimized both their low-power-generating CMOS device fabrication process and their high-heat-dissipation packaging capabilities. *Table 2* demonstrates this optimized thermal performance by comparing bipolar, NMOS, and Cypress high-speed 1K SRAM CMOS devices in their respective plastic packaging environments under standard operating conditions.

Table 2. Thermal Performance of Fast 1K SRAMs in Plastic Packages

Technology	Bipolar	NMOS	Cypress CMOS
Device Number	93422	9122	7C122
Speed (ns)	30	25	25
I_{CC} (mA)	150	110	60
V_{CC} (V)	5.0	5.0	5.0
P_{MAX} (mW)	750	550	300
Package RTH (JA) (°C/W)	120	120	70
Junction Temperature (°C) at Datasheet P_{MAX}[1]	160	136	91

During its normal operation, the Cypress 7C122 device experiences a 91°C junction temperature, whereas competitive devices in their respective packaging environments see a 45°C and 69°C higher junction temperature. In terms of relative reliability life expectancy, assuming a 1.0-eV activation energy failure mechanism, this translates into an improvement in excess of two orders of magnitude (100x) over the bipolar 93422 device, and more than one order of magnitude (30x) over the NMOS 9122 device.

Thermal Performance Data of Cypress Component Packages

The thermal performance of a semiconductor device in its package is determined by many factors, including package design and construction, packaging materials, chip size, chip thickness, chip attachment process and materials, package size, etc.

Thermal Resistance (θ_{JA}, θ_{JC})

Thermal resistance is a measure of the ability of a package to transfer the heat generated by the device inside it to the ambient.

For a packaged semiconductor device, heat generated near the junction of the powered chip causes the junction temperature to rise above the ambient temperature. The total thermal resistance is defined as

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

and θ_{JA} physically represents the temperature differential between the die junction and the surrounding ambient at a power dissipation of 1 watt.

The junction temperature is given by the equation

$$T_J = T_A + P[\theta_{JA}] = T_A + P[\theta_{JC} + \theta_{CA}]$$

where

$$\theta_{JC} = \frac{T_J - T_C}{P} \quad \text{and} \quad \theta_{CA} = \frac{T_C - T_A}{P}$$

T_A = Ambient temperature at which the device is operated; Most common standard temperature of operation is room temperature to 70°C.

T_J = Junction temperature of the IC chip.

T_C = Temperature of the case (package).

P = Power at which the device operates.

θ_{JC} = Junction-to-case thermal resistance. This is mainly a function of the thermal properties of the materials constituting the package.

θ_{JA} = Junction-to-ambient thermal resistance. The junction-to-ambient environment is a still-air environment.

θ_{CA} = Case-to-ambient thermal resistance. This is mainly dependent on the surface area available for convection and radiation and the ambient conditions among other factors. This can be controlled at the user end by using heat sinks providing greater surface area and better conduction path or by air or liquid cooling.

Thermal Resistance: Finite Element Model

θ_{JC} and θ_{JA} values given in the following figures and listed in the following tables have been obtained by simulation using the Finite element software ANSYS[2]. SDRC-IDEAS Pre and Post processor software[3] was used to create the finite element model of the packages and the ANSYS input data required for analysis.

SEMI Standard (Semiconductor Equipment and Materials International) method SEMI G30-88[4] states "heat sink" mounting technique to be the "reference" method for θ_{JC} estimation of ceramic packages. Accordingly, θ_{JC} of packages has been obtained by applying the boundary conditions that correspond to the heat sink mounted on the packages in the simulation.

For θ_{JA} evaluation, SEMI standard specification SEMI G38-87 suggests using a package-mounting arrangement that approximates the application environment. So, in evaluating the θ_{JA}, package on-board configuration is assumed.

Notes:
1. $T_{ambient}$ = 70°C
2. *ANSYS Finite Element Software User Guides*
3. *SDRC-IDEAS Pre and Post Processor User Guide*
4. *SEMI International Standards*, Vol. 4, Packaging Handbook, 1989.

Model Description

- One quarter of the package is mounted on a FR-4 PC board.
- Leads have been modeled as a continuous metallic plane, and equivalent thermal properties have been used to account for the plastic (or the glass in the case of ceramic packages) that fills the space between the leads.
- 1W power dissipation over the entire chip is assumed.
- 70°C ambient condition is considered.

Comparison of Simulation Data with Measured Data

In the case of ceramic packages, it is not unusual to see significant differences in θ_{JC} values when a heat sink is used in the place of fluid bath.[5] However, SEMI G30-88 test method recommends the heat sink configuration for θ_{JC} evaluation.

θ_{JA} values from simulation compare within 12 percent of the measured values. θ_{JA} values obtained from simulation seem to be *conservative* with an accuracy of about +12 percent.

Measured values given in *Table 3* used the Temperature Sensitive Parameter method described in MIL STD 883C, method 1012.1. The junction-to-ambient measurement was made in a still-air environment where the device was inserted into a low-cost standard-device socket and mounted on a standard 0.062" G10 PC board.

Table 3. 24-Lead Ceramic and Plastic DIPs

Package	Cavity/PAD Size (mils)	θ_{JA} (°C/W)		
		Measured	Simulation	% Diff.
24LCDIP[6]	170 x 270	64	67	5
24LPDIP[7]	160 x 210	72	82	12

Thermal Resistance of Packages with Forced Convection Air Flow

One of the methods adopted to cool the packages on PC boards at the system level is to used forced air (fans) specified in linear feet per minute or LFM. This helps reduce the device operating temperature by lowering the case to ambient thermal resistance. Available surface area of the package and the orientation of the package with respect to the air flow affect the reduction of thermal resistance that can be achieved. A general rule of thumb is:

- For plastic packages:
  - 200 LFM air flow can reduce θ_{JA} by 20 to 25%
  - 500 LFM air flow can reduce θ_{JA} by 30 to 40%
- For ceramic packages:
  - 200 LFM air flow can reduce θ_{JA} by 25 to 30%
  - 500 LFM air flow can reduce θ_{JA} by 35 to 45%

If θ_{JA} for a package in still air (no air flow) is known, approximate values of thermal resistance at 200 LFM and 500 LFM can be estimated. For estimation, the factors given in *Table 4* can be used as a guideline.

Table 4. Factors for Estimating Thermal Resistance

Package Type	Air Flow Rate (LFM)	Multiplication Factor
Plastic	200	0.77
Plastic	500	0.66
Ceramic	200	0.72
Ceramic	500	0.60

Example:

θ_{JA} for a plastic package in still air is given to be 80°C/W. Using the multiplication factor from *Table 4*:

- θ_{JA} at 200 LFM is (80 x 0.77) = 61.6°C/W
- θ_{JA} at 500 LFM is (80 x 0.66) = 52.8°C/W

θ_{JA} for a ceramic package in still air is given to be 70°C/W. Using *Table 4*:

- θ_{JA} at 200 LFM is (70 x 0.72) = 50.4°C/W
- θ_{JA} at 500 LFM is (70x0.60) = 42.0°C/W

Presentation of Data

The following figures and tables present the data taken using the aforementioned procedures. The thermal resistance values of Cypress standard packages are graphically illustrated in *Figures 2* through *6*. Each envelope represents a spread of typical Cypress integrated circuit chip sizes (upper boundary=5000 mils^2, lower boundary = 100,000 mils^2) in their thermally optimized packaging environments. These graphs should be used in conjunction with *Table 10*, which lists the die sizes of Cypress devices.

Tables 5 through *9* give the thermal resistance values for other package types not included in the graphs. The letter in the header (*D, P, J*, etc.) of these tables refer to the package designators as detailed in the Package Diagrams section of this catalog. The numeric values given in the table (e.g., 20.3) refer to the lead count (20) and package width in inches (.3). If no decimal appears, the reader must refer to the package diagrams.

Packaging Materials

Cypress plastic packages incorporate

- High thermal conductivity copper lead frame
- Molding compound with high thermal conductivity
- Gold bond wires

Cypress cerDIP packages incorporate

- High conductivity alumina substrates
- Silver-filled glass as die attach material
- Alloy 42–lead frame
- Aluminum bond wires
- Silver-filled conductive epoxy as dic attach material

7

Notes:
5. "Thermal resistance measurements and finite calculations for ceramic hermetic packages." James N. Sweet et. al., *SEMI-Therm*, 1990.
6. 24LCDIP = 24-lead cerDIP
7. 24LPDIP = 24-lead plastic DIP

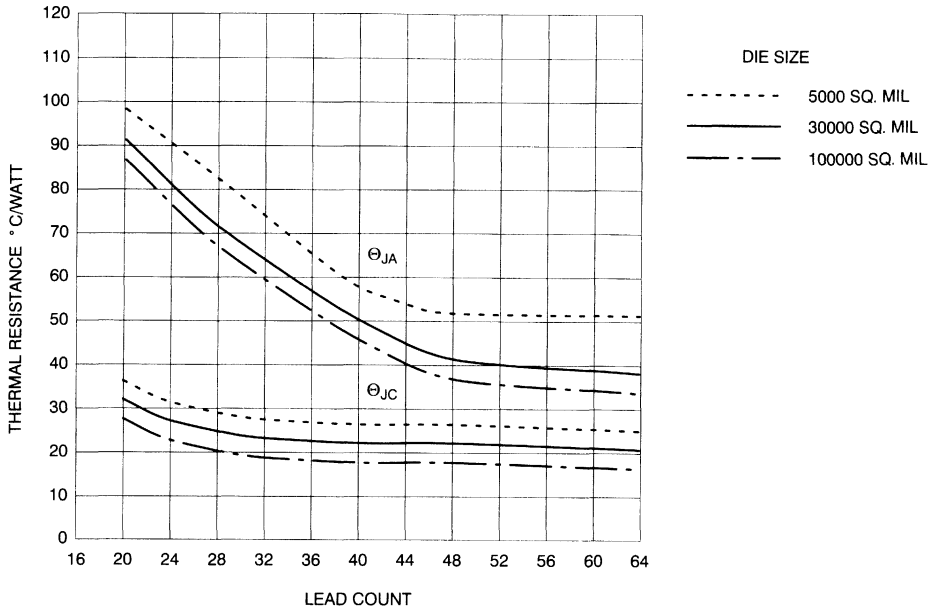


Figure 2. Thermal Resistance of Cypress Plastic DIPs (Package type "P")

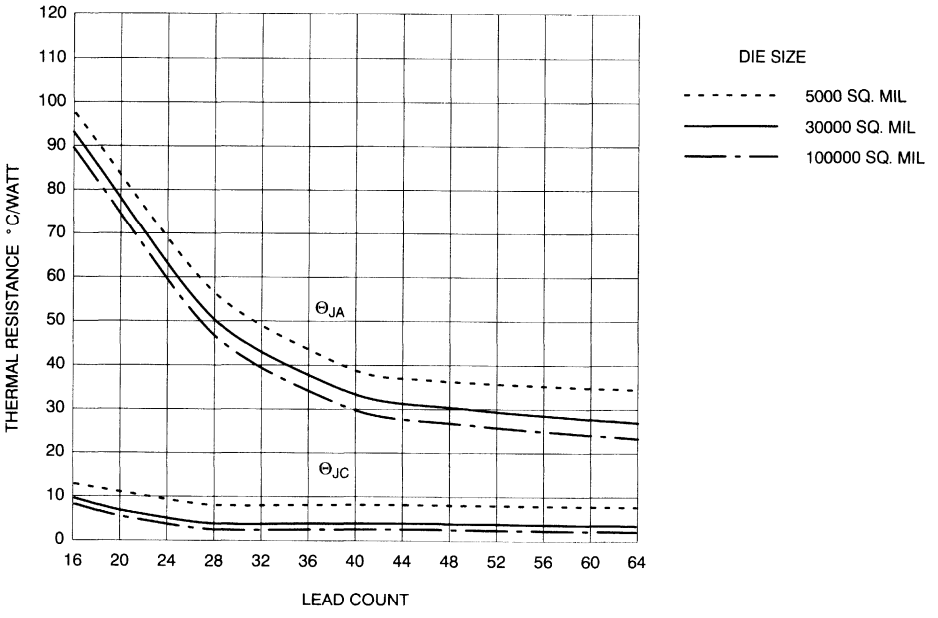


Figure 3. Thermal Resistance of Cypress Ceramic DIPs (Package type "D" and "W")

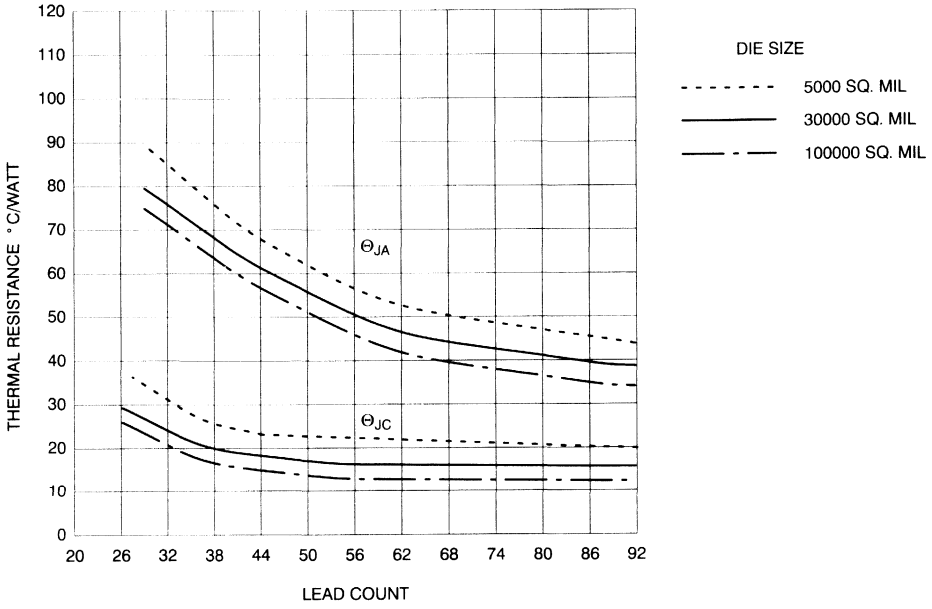


Figure 4. Thermal Resistance of Cypress PLCCs (Package type "J")

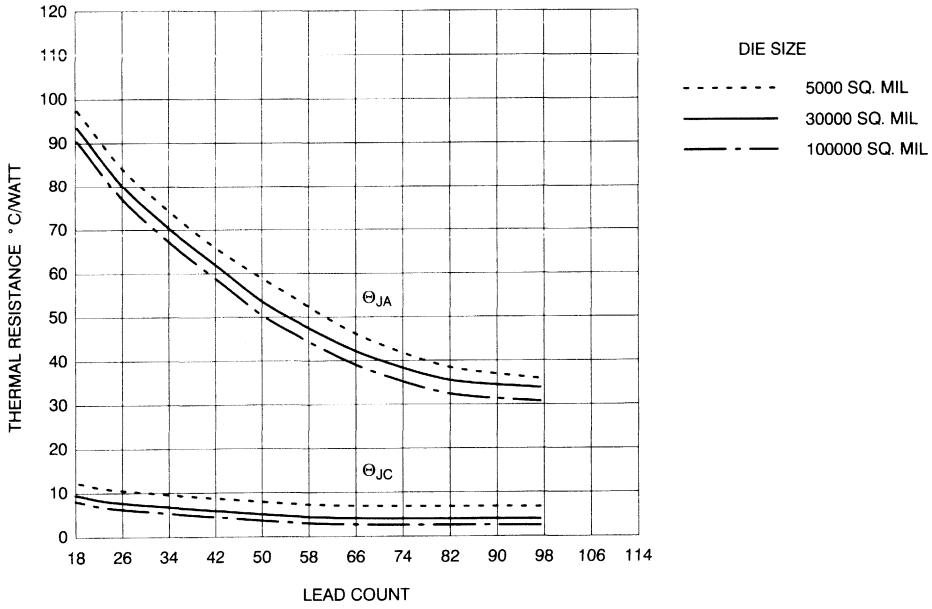


Figure 5. Thermal Resistance of Cypress LCCs (Package type "L" and "Q")

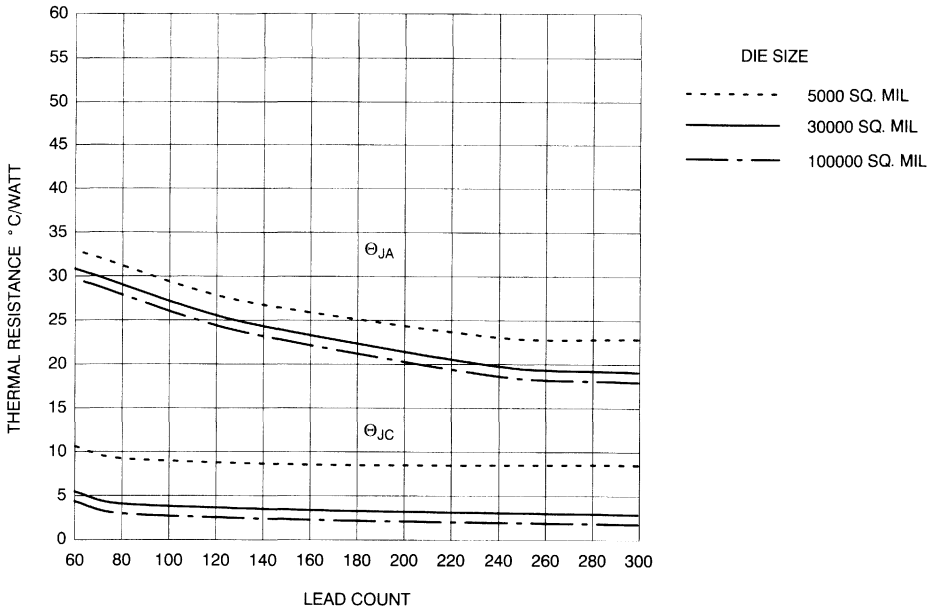


Figure 6. Thermal Resistance of Cypress Ceramic PGAs

Table 5. Plastic Surface Mount SOIC, SOJ[8,9]

Package Type "S" and "V"	Paddle Size (mil)	LF Material	Die Size (mil)	Die Area (sq. mil)	θ_{JC} (°C/W)	θ_{JA} (°C/W still air)
16	140 x 170	Copper	98 x 84	8,232	19.0	120
18	140 x 170	Copper	98 x 84	8,232	18.0	116
20	180 x 250	Copper	145 x 213	30,885	17.0	105
24	180 x 250	Copper	145 x 213	30,885	15.4	88
24	170 x 500	Copper	141 x 459	64,719	14.9	85
28	170 x 500	Copper	145 x 213	30,885	16.7	84
28	170 x 500	Copper	141 x 459	64,719	14.4	80

Table 6. Plastic Quad Flatpacks

Package Type "N"	LF Material	Paddle Size (mil)	Die Size (mil)	θ_{JC} (°C/W)	θ_{JA} (°C/W still air)
100	Copper	310 x 310	235 x 235	17	51
144	Copper	310 x 310	235 x 235	18	41
160	Copper	310 x 310	230 x 230	18	40
184	Copper	460 x 460	322 x 311	15	38.5
208	Copper	400 x 400	290 x 320	16	39

Notes:
8. The data in *Table 6* was simulated for SOIC packaging.
9. SOICs and SOJs have very similar thermal resistance characteristics. The thermal resistance values given above apply to SOJ packages also.

Table 7. Ceramic Quad Flatpacks

Package Type "H" and "Y"	Cavity Size (mil)	LF Material	Die Size (mil)	Die Area (sq. mil)	θ_{JC} (°C/W)	θ_{JA} (°C/W still air)
28	250 x 250	Alloy 42	123 x 162	19,926	9.2	96
28	250 x 250	Alloy 42	150 x 180	27,000	8.9	93
32	316 x 317	Alloy 42	198 x 240	47,520	7.5	72
44	400 x 400	Alloy 42	310 x 250	77,500	5.9	55
52	400 x 400	Alloy 42	250 x 310	77,500	5.9	55
68	400 x 400	Alloy 42	310 x 250	77,500	5.4	33
84	450 x 450	Alloy 42	310 x 250	77,500	5.4	29

Table 8. Cerpacks

Package Type "K" and "T"	Cavity Size (mil)	Leadframe Material	Die Size (mil)	Die Area (sq. mil)	θ_{JC} (°C/W)	θ_{JA} (°C/W still air)
16	140 x 200	Alloy 42	100 x 118	11,800	10	107
18	140 x 200	Alloy 42	100 x 118	11,800	10	104
20	180 x 265	Alloy 42	128 x 170	21,760	9	102
24	170 x 270	Alloy 42	128 x 170	21,760	10	102
28	210 x 210	Alloy 42	150 x 180	27,000	9	98
32	210 x 550	Alloy 42	141 x 459	64,719	7	81

Table 9. Miscellaneous Packaging

Package Type	Cavity Size (mil)	Leadframe Material	Die Size (mil)	Die Area (sq. mil)	θ_{JC} (°C/W)	θ_{JA} (°C/W still air)
24 VDIP[10]	500 x 275	Alloy 42	145 x 213	30,885	6	57
68 CPGA[11]	350 x 350	Kovar Pins	323 x 273	88,179	3	28

Notes:
10. VDIP = "PV" package.
11. CPGA = "G" package.

Table 10. Die Sizes of Cypress Devices

Part Number	Size (mil^2)
PLDs	
CY7C330	20088
CY7C331	16536
CY7C332	19116
CY7C335	23111
CY7C341	136320
CY7C342	83475
CY7C342B	49104
CY7C343	43953
CY7C344	21977
PAL16L8	13552
PAL16R4	13552
PAL16R6	13552
PAL16R8	13552

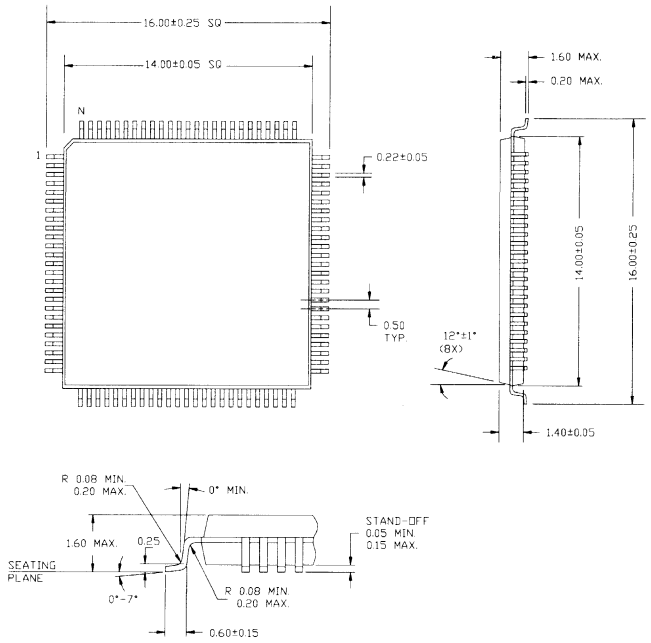
Part Number	Size (mil^2)
PAL22V10C	18834
PAL22VP10C	18834
PALC16L8	9700
PALC16R4	9700
PALC16R6	9700
PALC16R8	9700
PALC22V10	19926
PALC22V10B	13284
PALC22V10D	12954
PLD20G10C	18834
PLDC20G10	19926
PLDC20G10B	13284
PLDC20RA10	13284

Document #: 38–00190

Package Diagrams

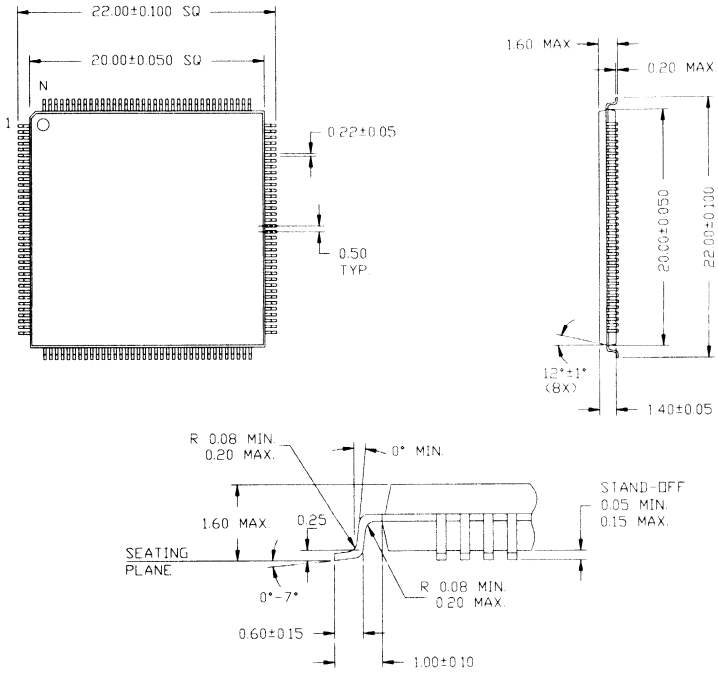
Thin Quad Flat Packs

100-Pin Thin Quad Flat Pack A100



Thin Quad Flat Packs (continued)

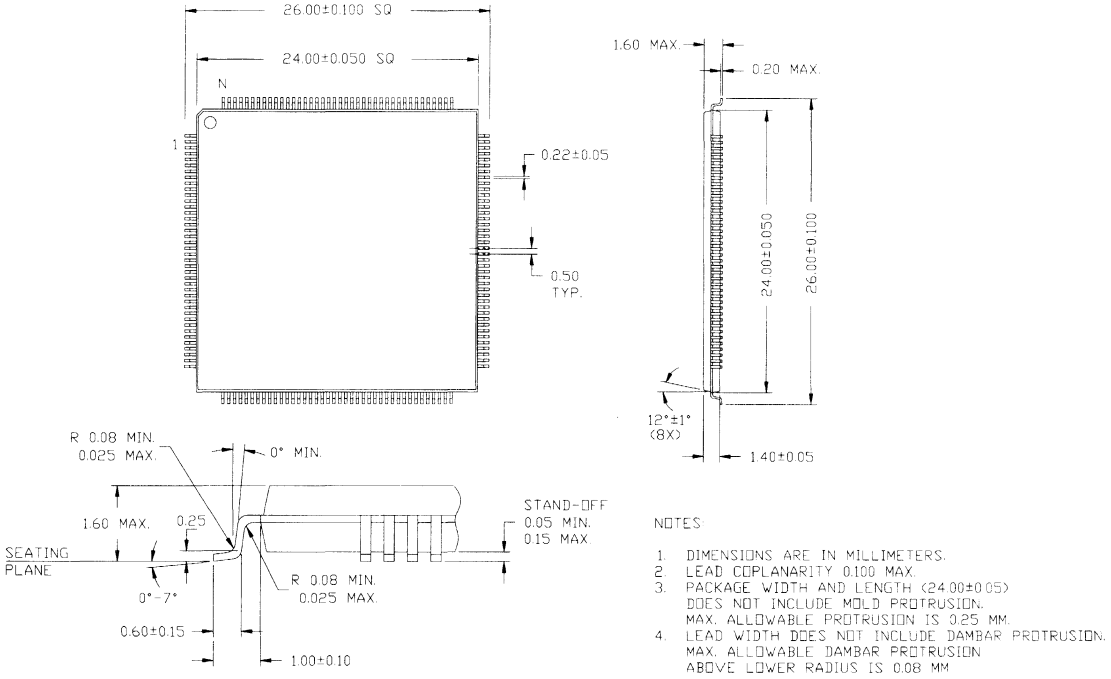
144-Pin Thin Quad Flat Pack A144



7

Thin Quad Flat Packs (continued)

160-Lead Thin Quad Flat Pack (TQFP) A160

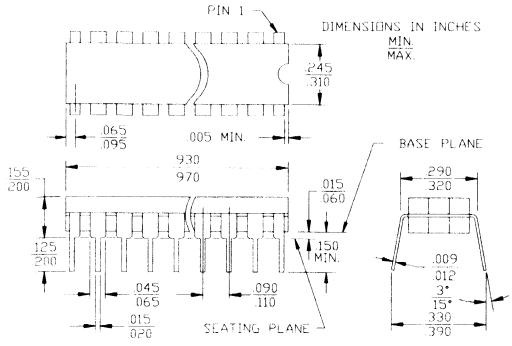


NOTES

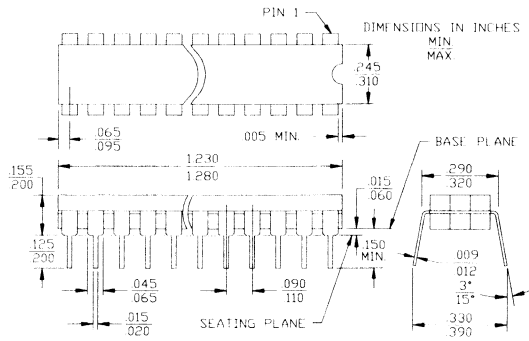
1. DIMENSIONS ARE IN MILLIMETERS.
2. LEAD COPLANARITY 0.100 MAX.
3. PACKAGE WIDTH AND LENGTH (24.00±0.05) DOES NOT INCLUDE MOLD PROTRUSION. MAX. ALLOWABLE PROTRUSION IS 0.25 MM.
4. LEAD WIDTH DOES NOT INCLUDE DAMBAR PROTRUSION. MAX. ALLOWABLE DAMBAR PROTRUSION ABOVE LOWER RADIUS IS 0.08 MM

Ceramic Dual-In-Line Packages

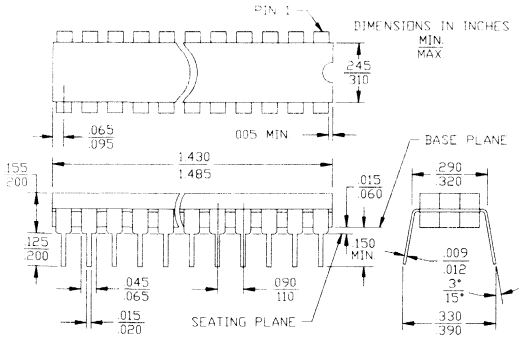
20-Lead (300-Mil) CerDIP D6
MIL–STD–1835 D–8 Config. A



24-Lead (300-Mil) CerDIP D14
MIL–STD–1835 D–9 Config. A



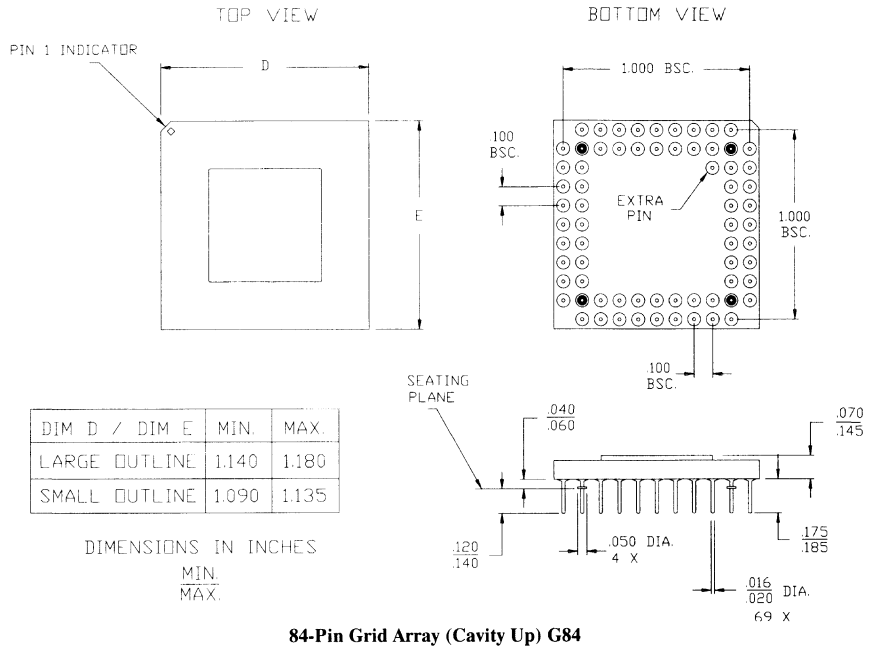
28-Lead (300-Mil) CerDIP D22
MIL–STD–1835 D–15 Config. A



7

Ceramic Pin Grid Arrays

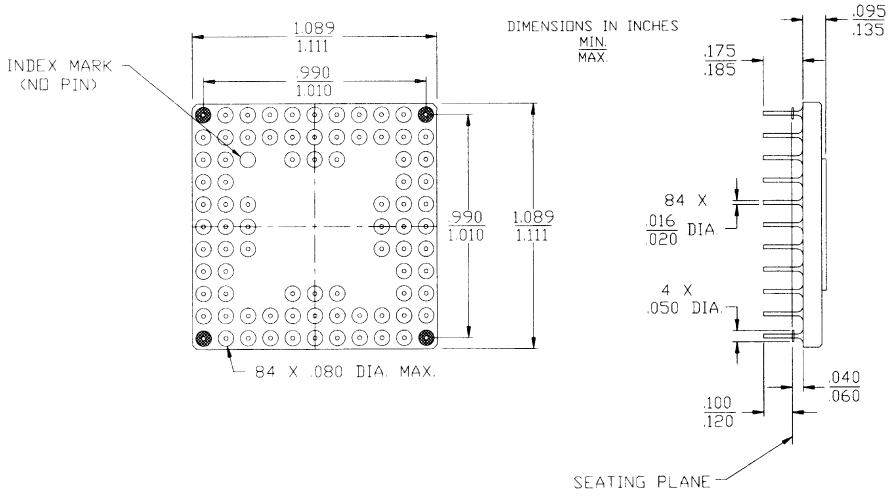
69-Pin Grid Array (Cavity Up) G69



DIM D / DIM E	MIN.	MAX.
LARGE OUTLINE	1.140	1.180
SMALL OUTLINE	1.090	1.135

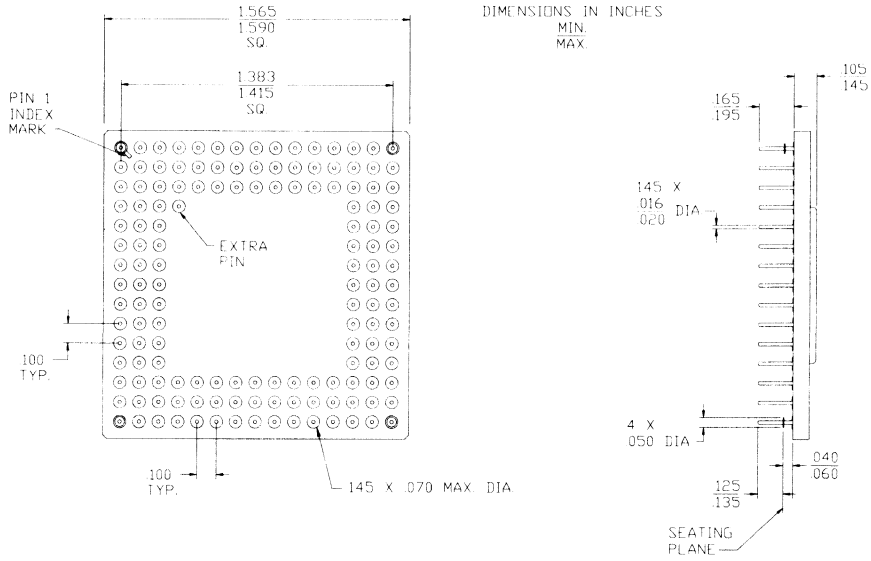
DIMENSIONS IN INCHES
MIN.
MAX.

84-Pin Grid Array (Cavity Up) G84



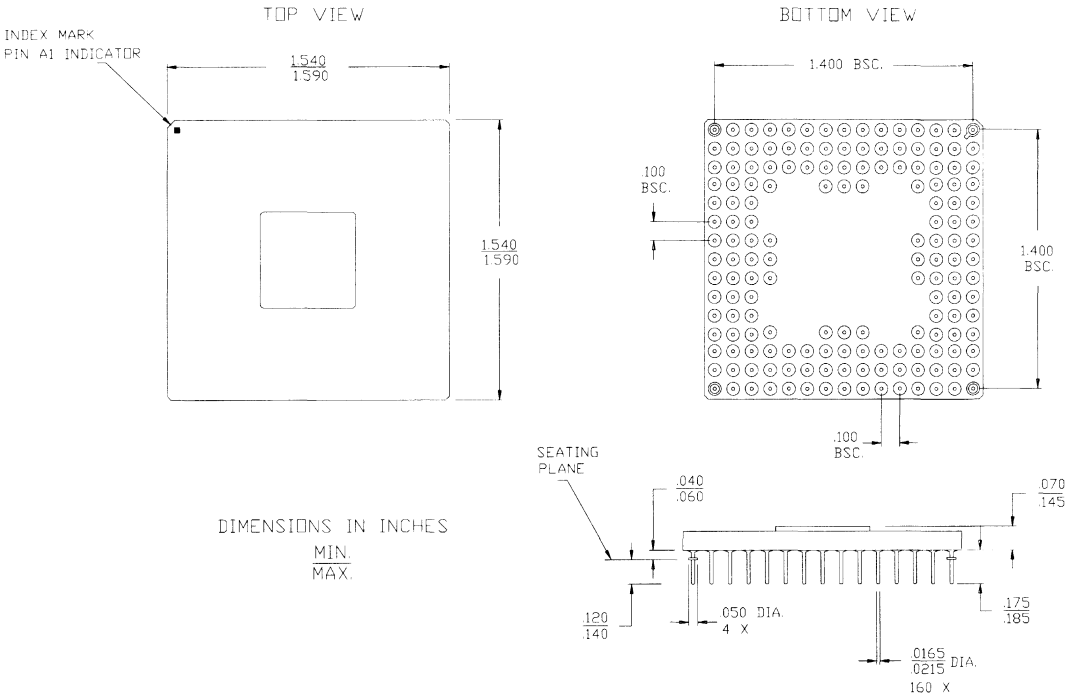
Ceramic Pin Grid Arrays (continued)

145-Pin Grid Array (Cavity Up) G145



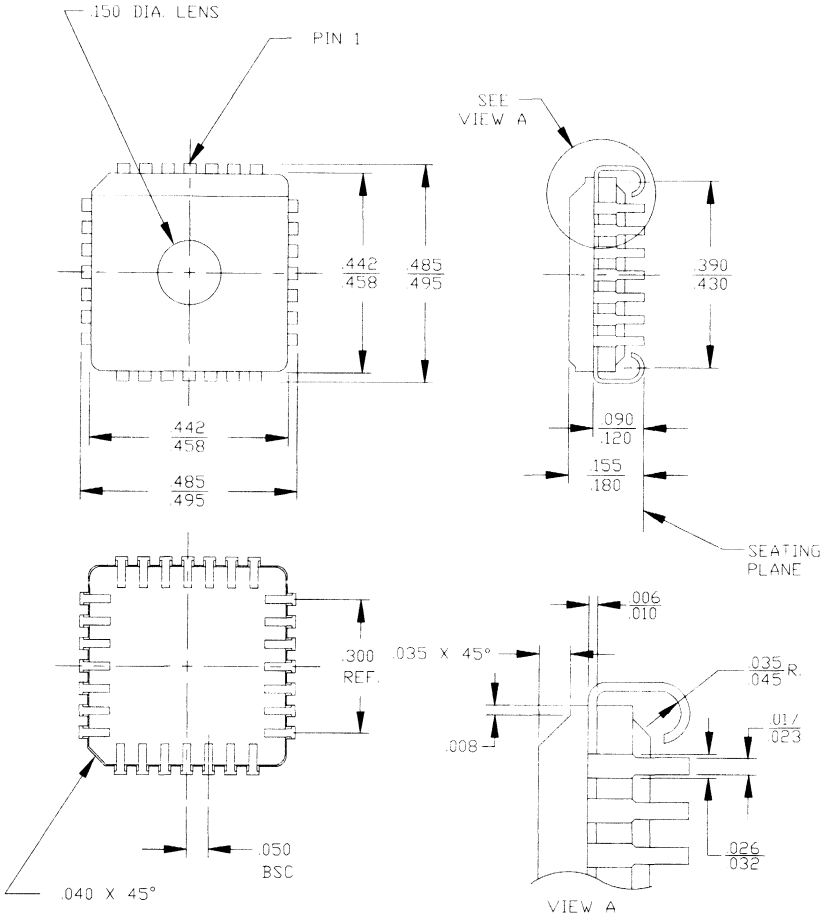
Ceramic Pin Grid Arrays (continued)

160-Pin PGA G160



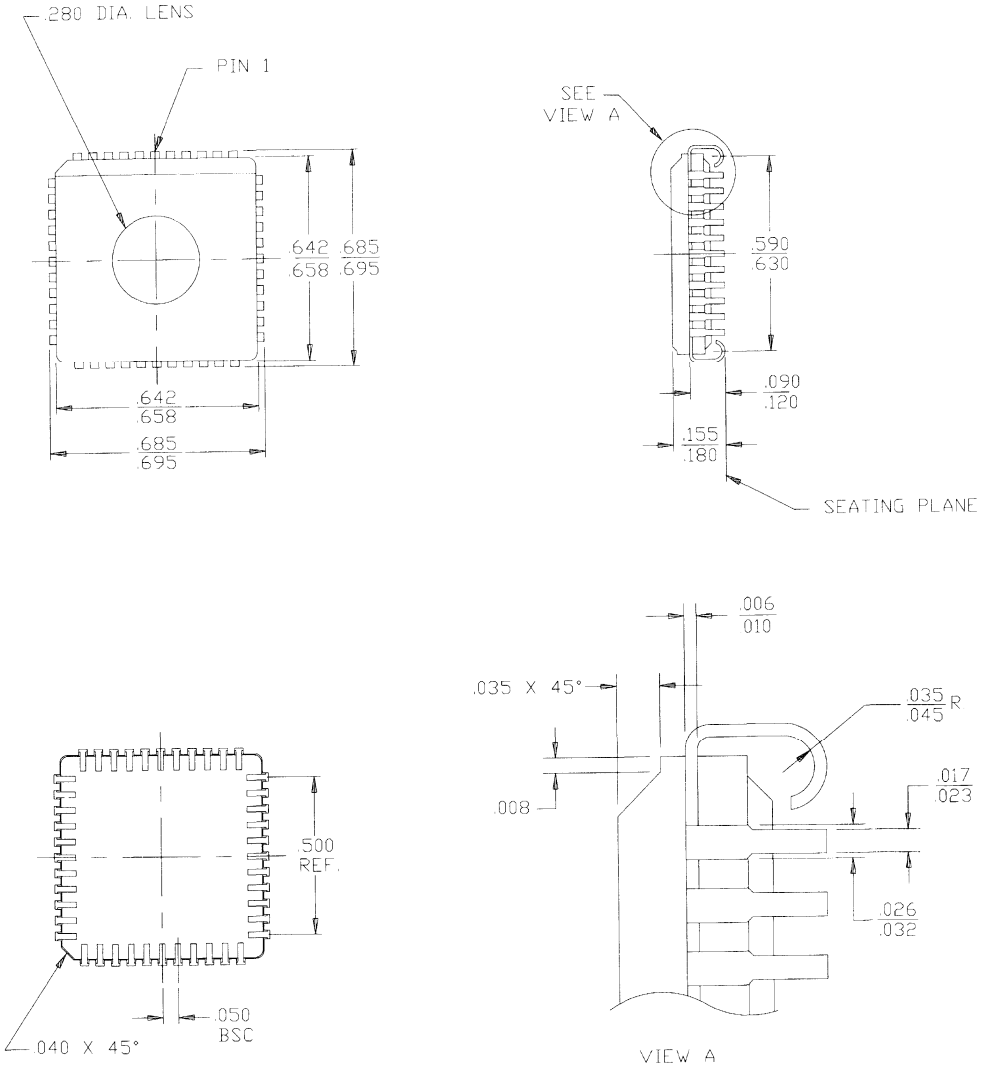
Ceramic Windowed J-Leaded Chip Carriers

28-Pin Windowed Leaded Chip Carrier H64



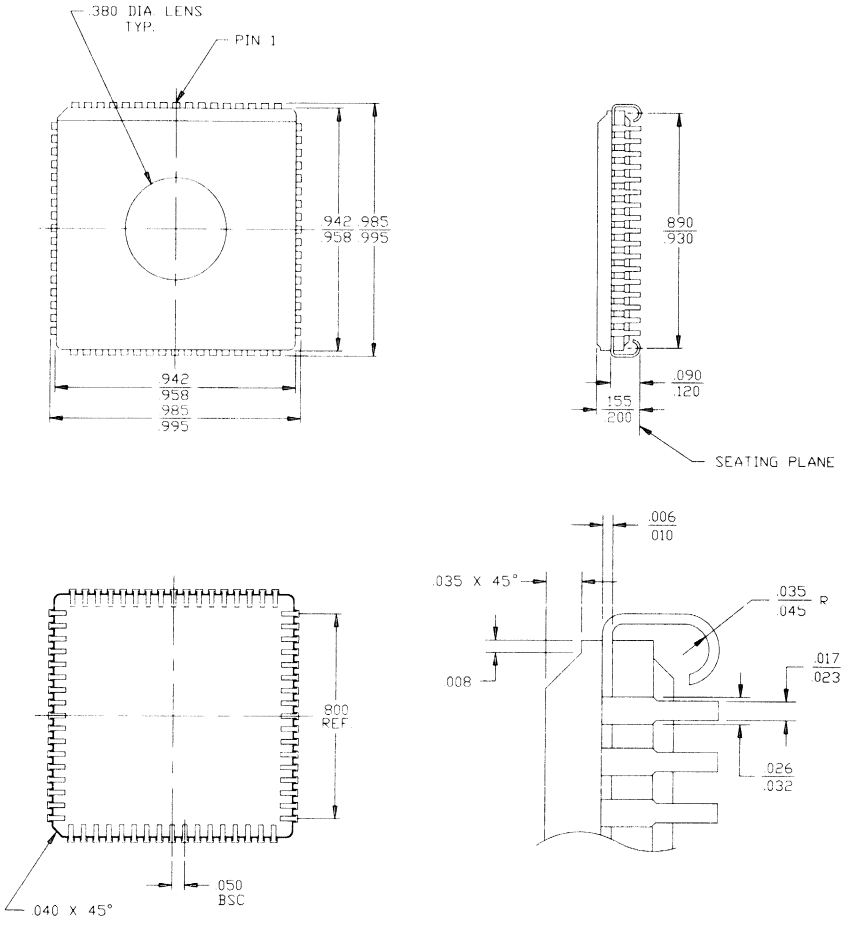
Ceramic Windowed J-Leaded Chip Carriers (continued)

44-Pin Windowed Leaded Chip Carrier H67



Ceramic Windowed J-Leaded Chip Carriers (continued)

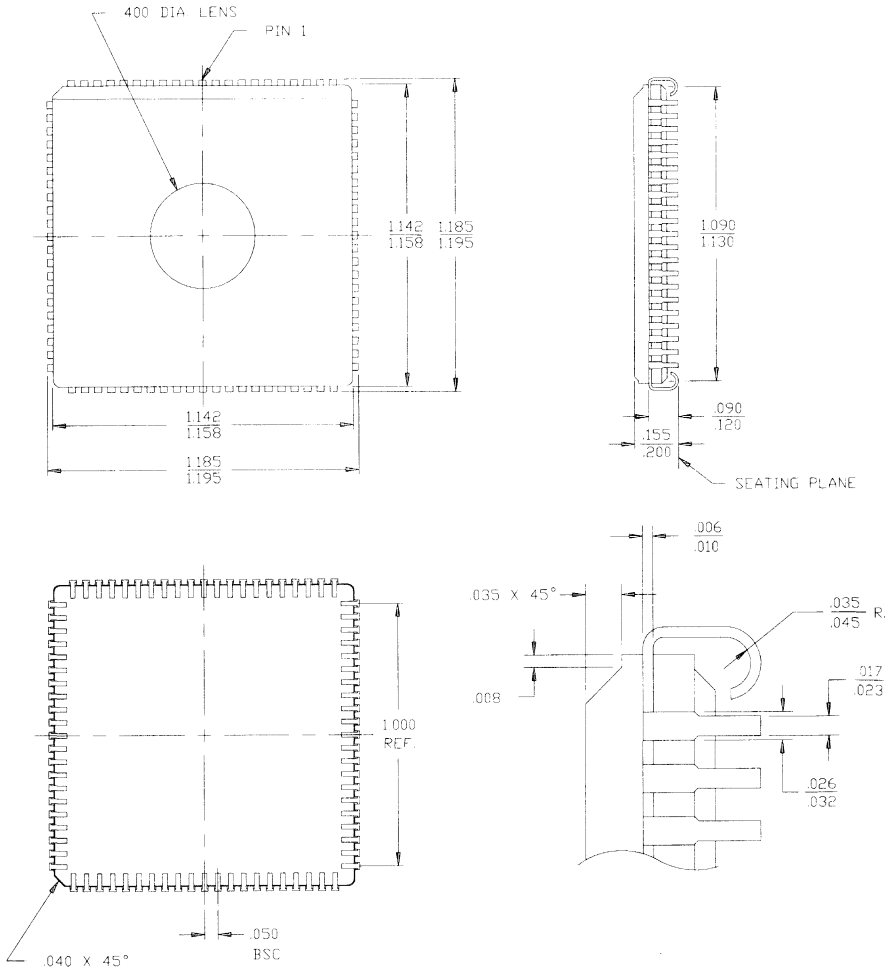
68-Pin Windowed Leaded Chip Carrier H81



7

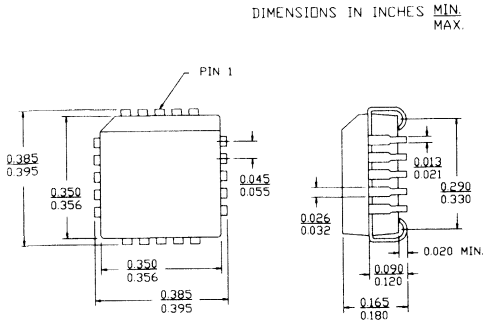
Ceramic Windowed J-Leaded Chip Carriers (continued)

84-Lead Windowed Leaded Chip Carrier H84

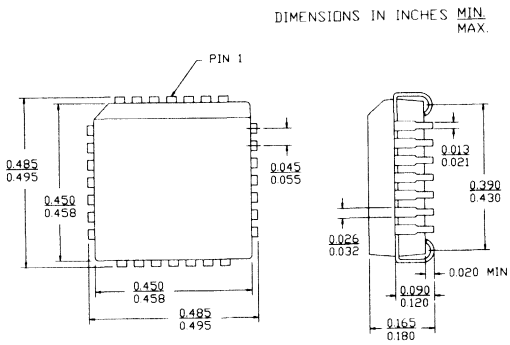


Plastic Leaded Chip Carriers

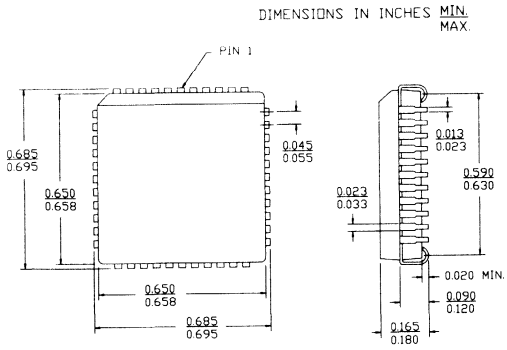
20-Lead Plastic Leaded Chip Carrier J61



28-Lead Plastic Leaded Chip Carrier J64

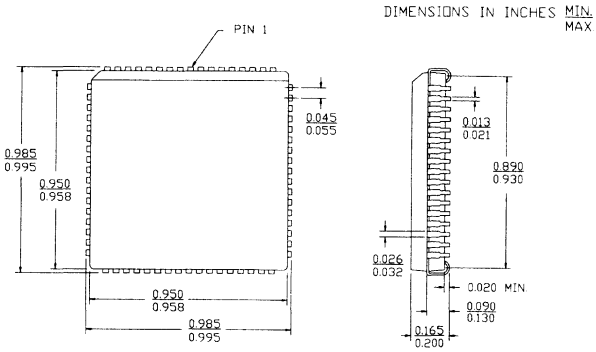


44-Lead Plastic Leaded Chip Carrier J67

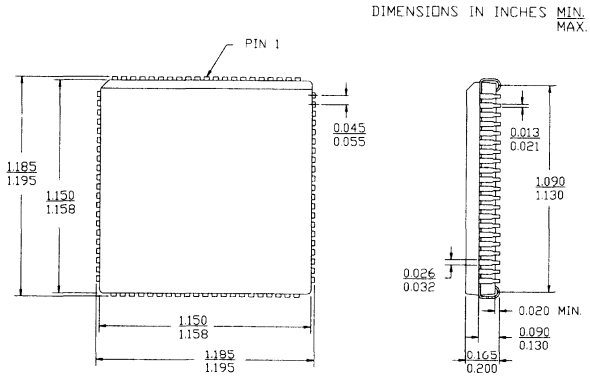


Plastic Leaded Chip Carriers (continued)

68-Lead Plastic Leaded Chip Carrier J81

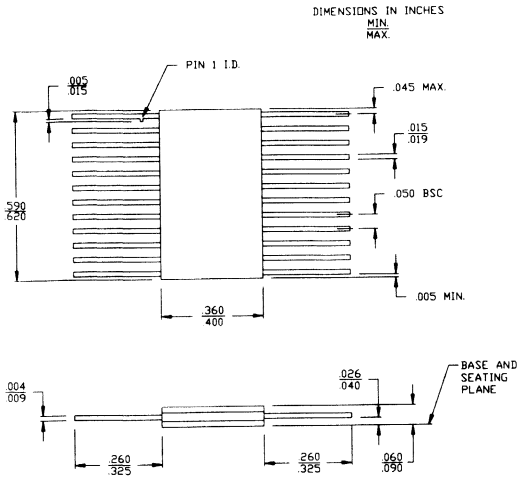


84-Lead Plastic Leaded Chip Carrier J83



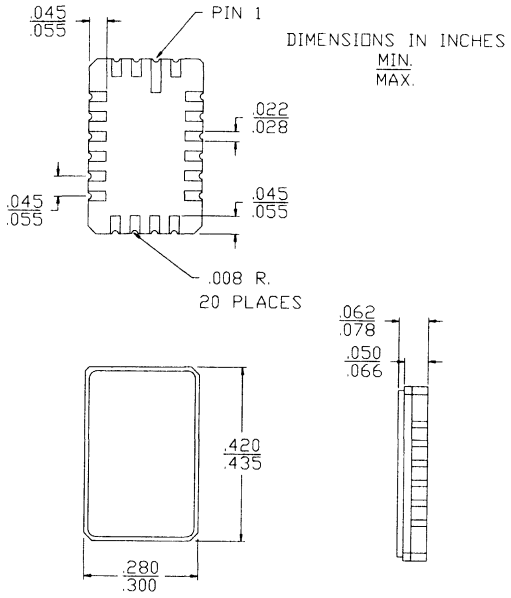
Cerpacks

24-Lead Rectangular Cerpack K73
MIL-STD-1835 F-6 Config. A

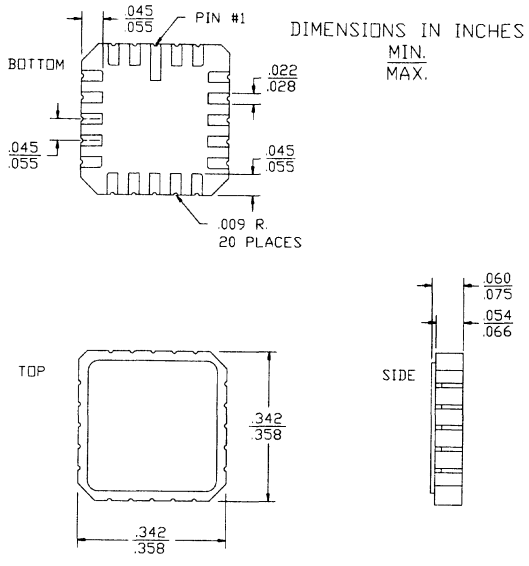


Ceramic Leadless Chip Carriers

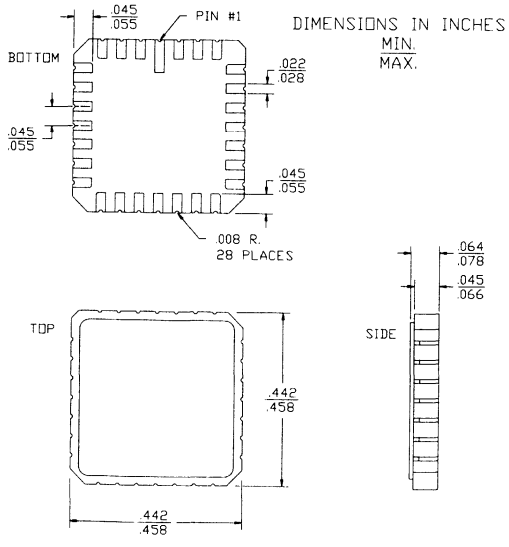
20-Pin Rectangular Leadless Chip Carrier L51
MIL-STD-1835 C-13



20-Pin Square Leadless Chip Carrier L61
MIL-STD-1835 C-2A

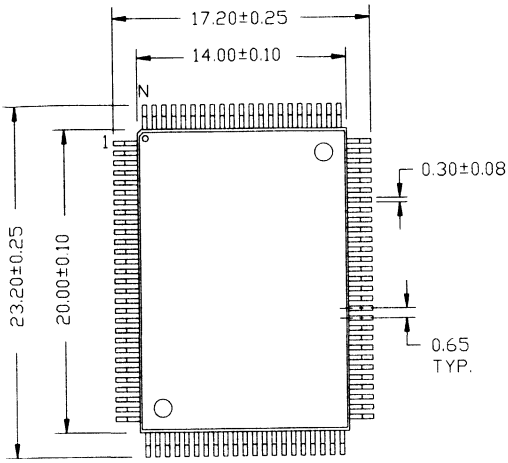


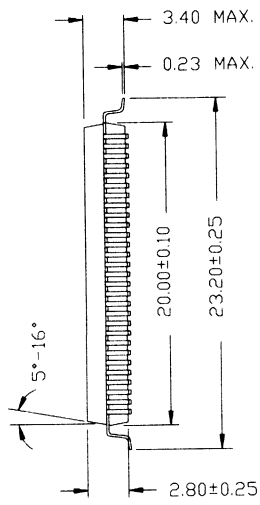
28-Square Leadless Chip Carrier L64
MIL-STD-1835 C-4

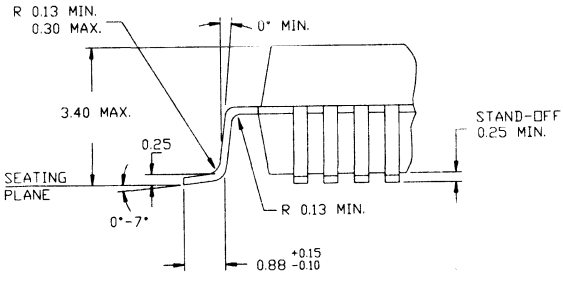


Plastic Quad Flatpacks

100-Lead Plastic Quad Flatpack N100







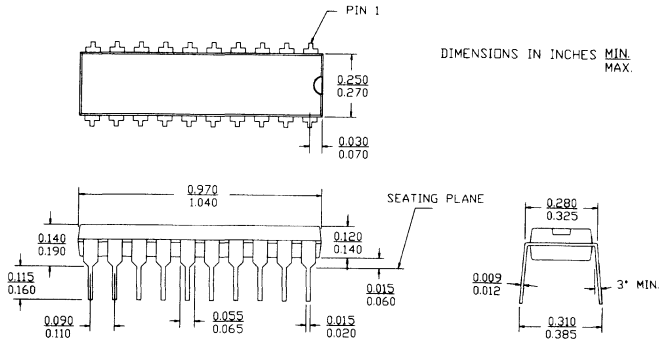
NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. LEAD COPLANARITY 0.100 MAX.
3. PACKAGE WIDTH (14.00±0.10) AND LENGTH (20.00±0.10) DOES NOT INCLUDE MOLD PROTRUSION. MAX. ALLOWABLE PROTRUSION IS 0.25 MM.
4. LEAD WIDTH DOES NOT INCLUDE DAMBAR PROTRUSION. MAX. ALLOWABLE DAMBAR PROTRUSION ABOVE LOWER RADIUS IS 0.08 MM.

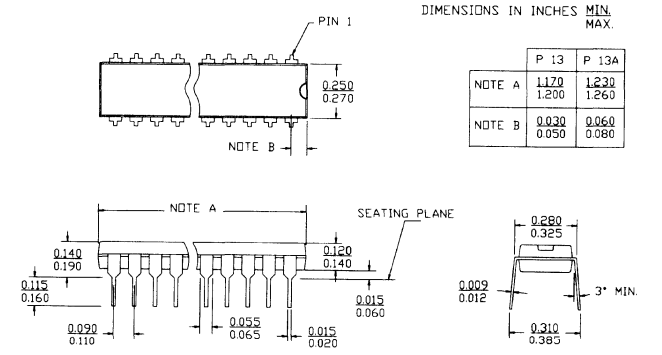
7

Plastic Dual-In-Line Packages

20-Lead (300-Mil) Molded DIP P5

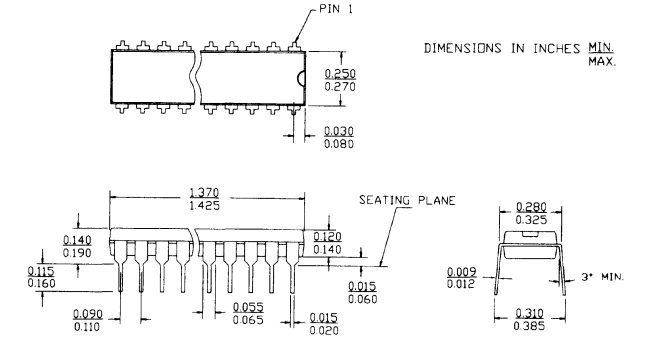


24-Lead (300-Mil) Molded DIP P13/P13A



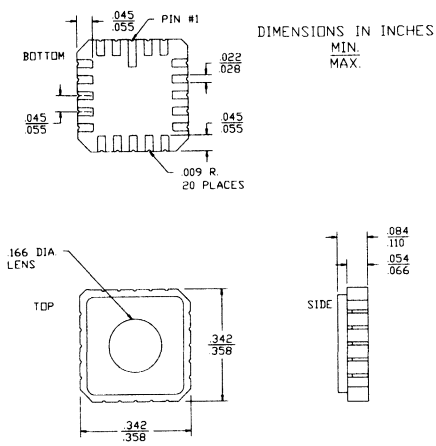
	P 13	P 13A
NOTE A	1.170 1.200	1.230 1.260
NOTE B	0.030 0.050	0.060 0.080

28-Lead (300-Mil) Molded DIP P21

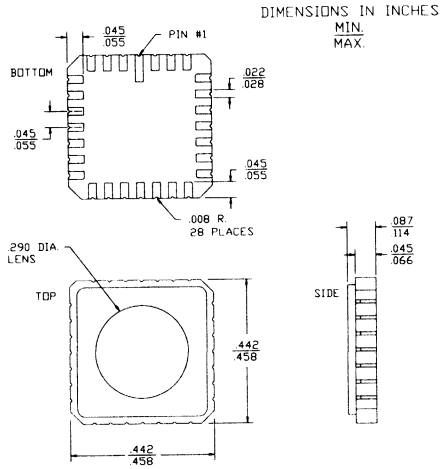


Ceramic Windowed Leadless Chip Carriers

20-Pin Windowed Square Leadless Chip Carrier Q61
MIL-STD-1835 C-2A

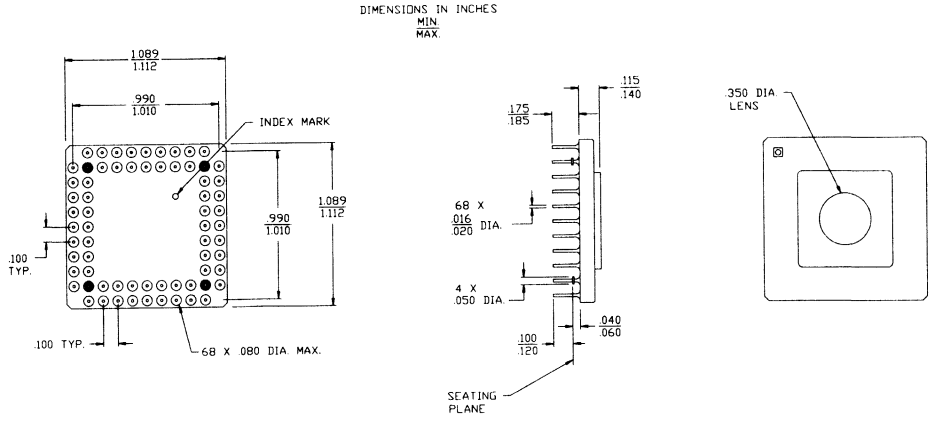


28-Pin Windowed Leadless Chip Carrier Q64
MIL-STD-1835 C-4



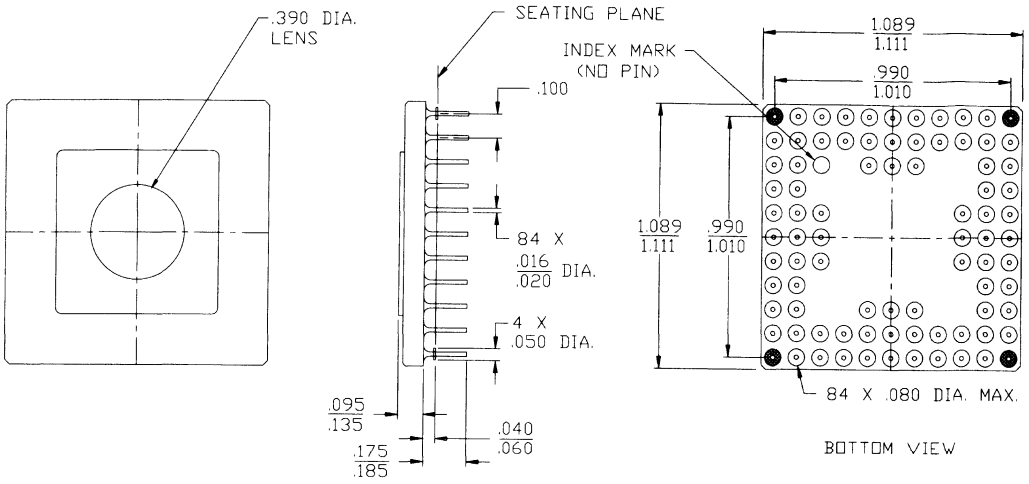
Ceramic Windowed Pin Grid Arrays

68-Pin Windowed PGA Ceramic R68

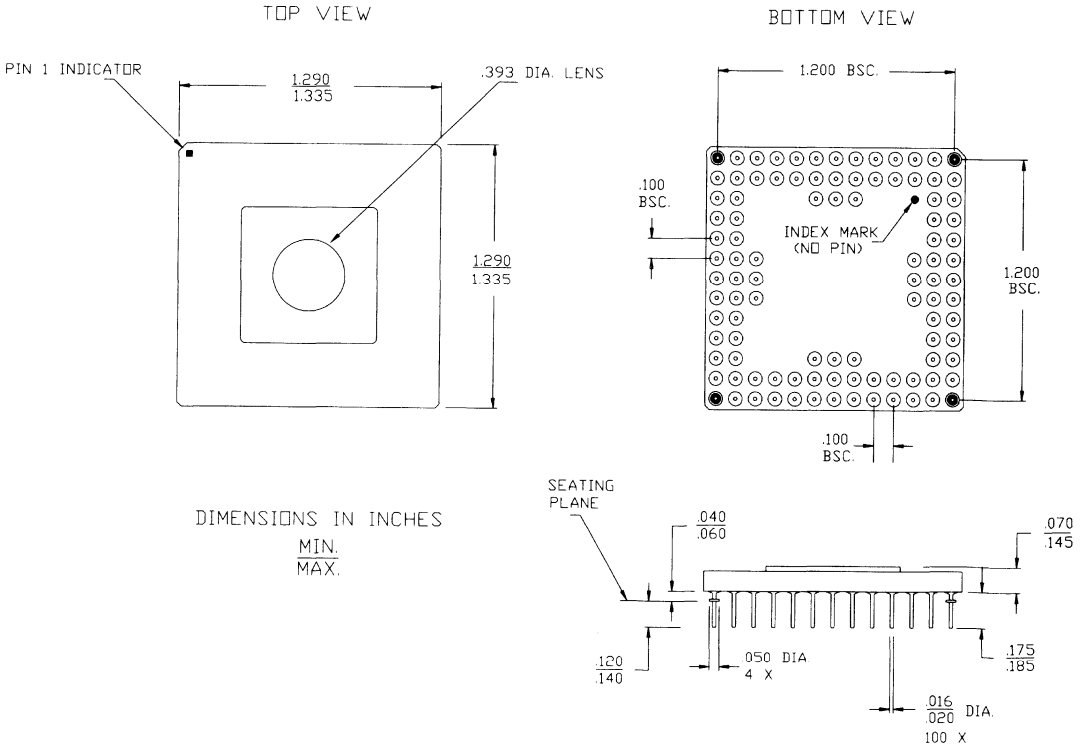


Ceramic Windowed Pin Grid Arrays (continued)

84-Lead Windowed Pin Grid Array R84

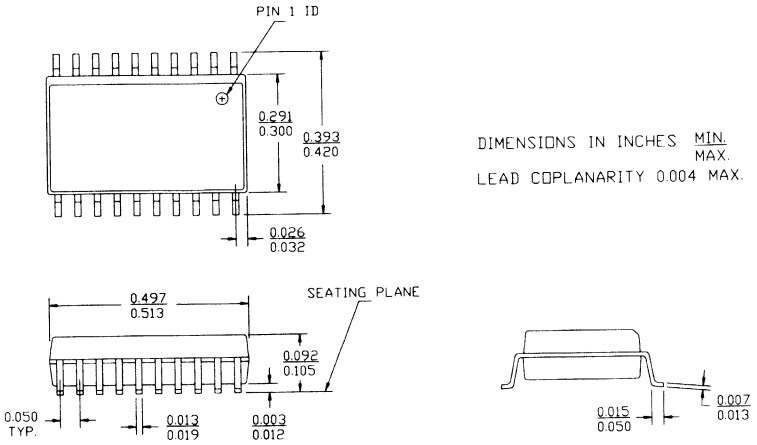


100-Pin Windowed Ceramic Pin Grid Array R100



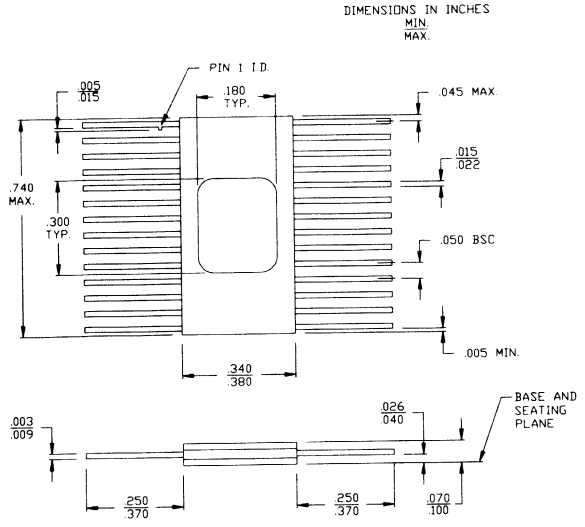
Plastic Small Outline ICs

20-Lead (300-Mil) Molded SOIC S5



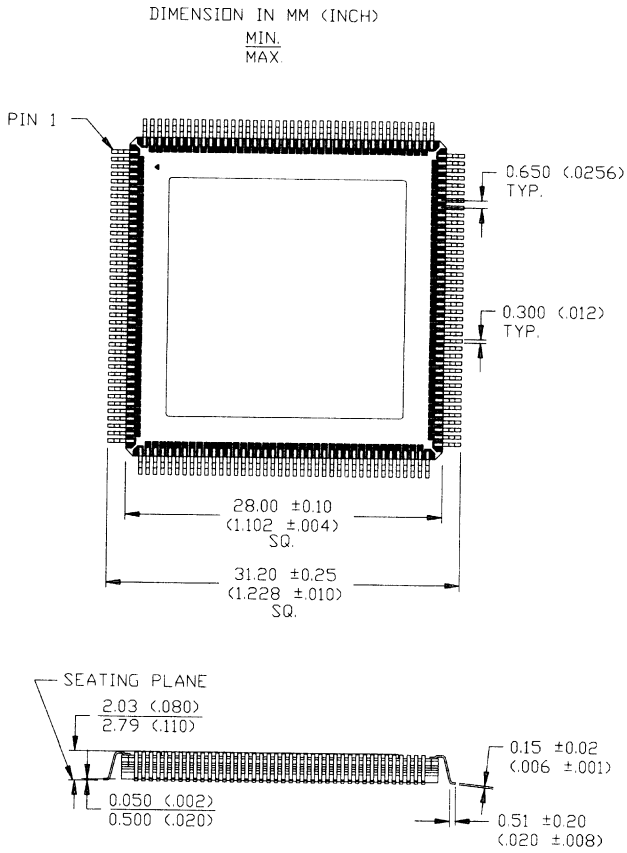
Windowed Cerpacks

28-Lead Windowed Cerpack T74



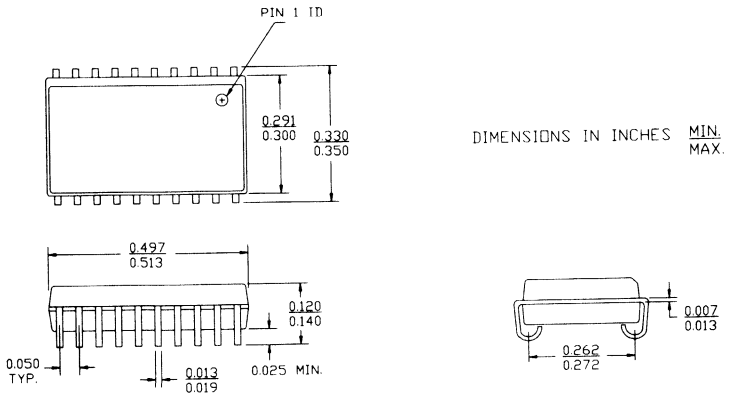
Ceramic Quad Flatpacks

160-Lead Ceramic Quad Flatpack (Cavity Up) U162



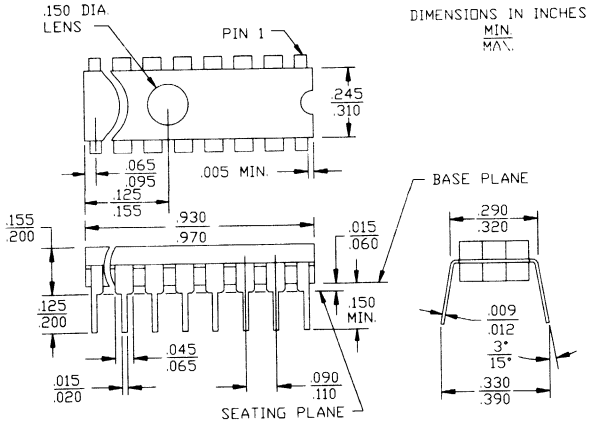
Plastic Small Outline J–Bend

20-Lead (300-Mil) Molded SOJ V5



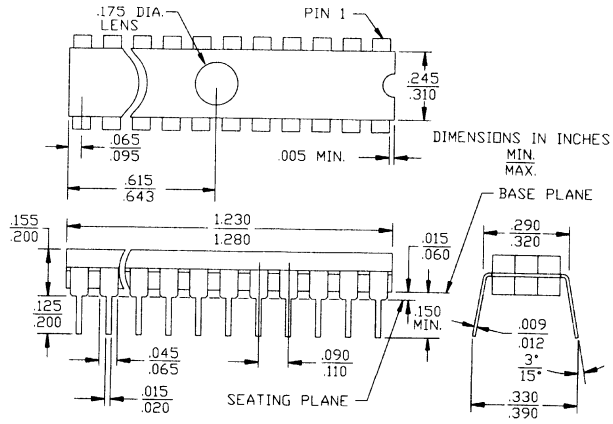
Ceramic Windowed Dual-In-Line Packages

20-Lead (300-Mil) Windowed CerDIP W6
MIL–STD–1835 D–8 Config. A

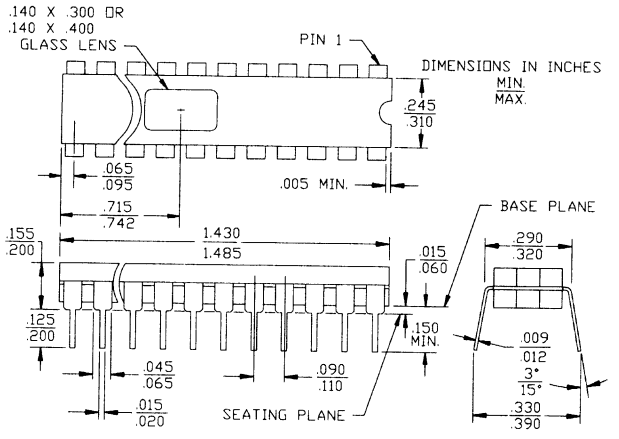


Ceramic Windowed Dual-In-Line Packages (continued)

24-Lead (300-Mil) Windowed CerDIP W14
MIL-STD-1835 D-9 Config. A

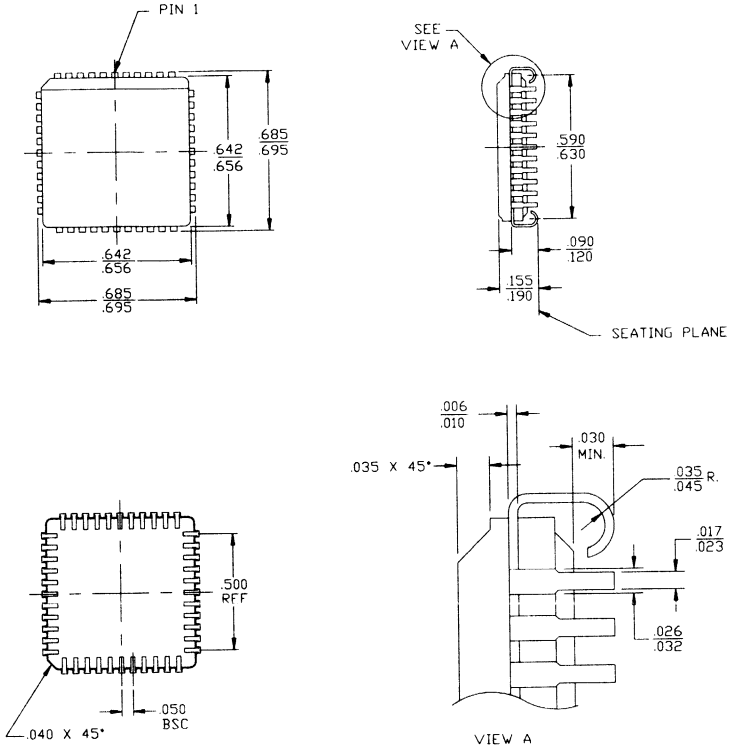


28-Lead (300-Mil) Windowed CerDIP W22
MIL-STD-1835 D-15 Config. A



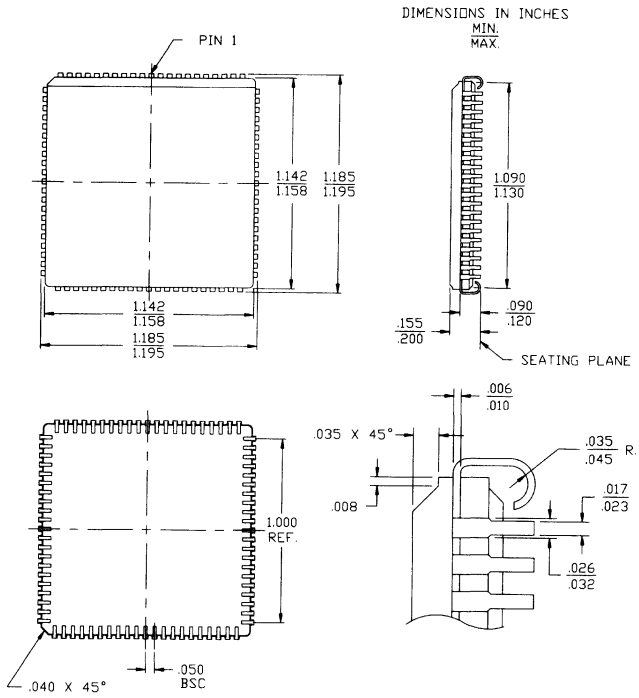
Ceramic J-Leaded Chip Carriers

44-Pin Ceramic Leaded Chip Carrier Y67

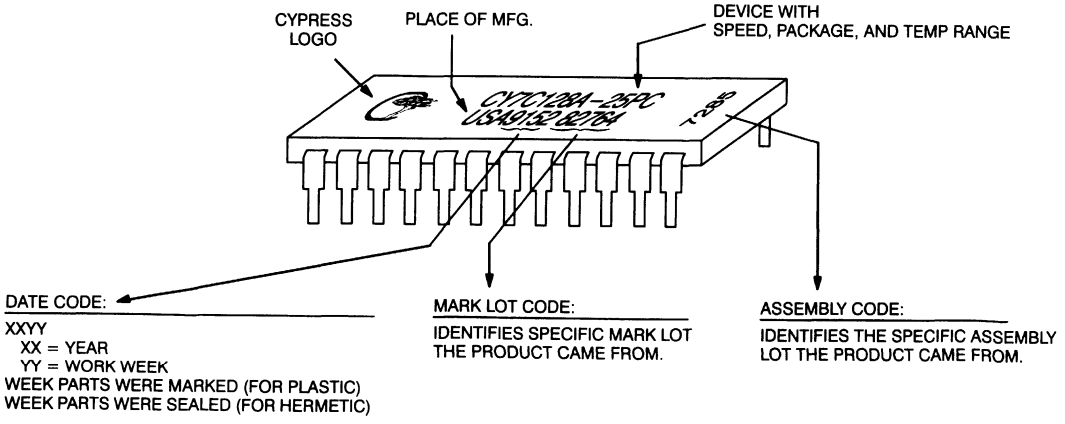


Ceramic J-Leaded Chip Carriers (continued)

84-Pin Ceramic Leaded Chip Carrier Y84



Typical Marking for DIP Packages (P and D Type)



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